ECE 255, Differential Amplifiers, Cont.

3 April 2018

1 Introduction

In this lecture, we will continue from the previous lecture with studying differential amplifiers starting with input differential resistance.

1.1 Small-Signal Operation

1.1.1 Input Differential Resistance

As in other BJTs, the incremental base current i_b and i_e are related by

$$i_b = \frac{i_e}{\beta + 1} = \frac{v_{id}/(2r_e)}{\beta + 1} \tag{1.1}$$

Hence, the differential input resistance is

$$R_{id} = \frac{v_{id}}{i_b} = (\beta + 1)2r_e = 2r_\pi \tag{1.2}$$

The above is the familiar resistance-reflection rule: for every unit of current flowing in the base, there is $\beta + 1$ unit of current flowing in the emitter, and hence the amplification factor of $\beta + 1$ for the emitter resistance into the base. When emitter resistors are added to the emitters, as shown in Figure **??**, the corresponding input resistance is

$$R_{id} = (\beta + 1)(2r_e + 2R_e) \tag{1.3}$$

In the above formulas, for differential amplifiers, the input voltage v_{id} sees the resistors of both transistors, and hence, the resistors r_e and R_e are doubled compared to the ordinary amplifiers.

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1.1.2 Differential Voltage Gain

In the small signal regime when $v_{id} \ll V_T$, the total collector currents are

$$i_{C1} = I_C + g_m \frac{v_{id}}{2}, \qquad i_{C2} = I_C - g_m \frac{v_{id}}{2} \tag{1.4}$$

with $I_C = \alpha I/2$. The total voltage at the collectors are

$$v_{C1} = (V_{CC} - I_C R_C) - g_m R_C \frac{v_{id}}{2}, \qquad v_{C2} = (V_{CC} - I_C R_C) + g_m R_C \frac{v_{id}}{2} \tag{1.5}$$

Consequently, the differential voltage gain is

$$A_d = \frac{v_{od}}{v_{id}} = g_m R_C \tag{1.6}$$

With emitter resistors in place, this becomes

$$A_d = \frac{\alpha(2R_C)}{2r_e + 2R_e} \approx \frac{R_C}{r_e + R_e} \approx \frac{g_m R_C}{1 + g_m R_e} \tag{1.7}$$

The last form is good for mnemonics.

1.1.3 Differential Half-Circuits

The differential amplifier can be broken into differential half-circuits. Depending on if the amplifier is symmetrically or anti-symmetrically driven, the half circuits are different.

Differential-Mode Case As before, due to symmetry, when the input voltage is completely complementary, there is a virtual ground between the two transistors, such that the differential circuit can be divided into two half-circuits. This is illustrated in Figure 1(a) and Figure 1(b).

When the differential amplifier is asymmetrically driven as shown in Figure 2, if the input signal is small, one can still assume that a virtual ground exists at the emitters of the transistors, and proceed with a half-circuit analysis. Hence, the differential voltage gain is

$$A_d = g_m(R_C \parallel r_o) \tag{1.8}$$

using the small-signal hybrid-π model shown in Figure 3. An output resistance r_o is include to model the Early effect.

Common-Mode Case For this case, we will take some examples from Jaeger and Blalock's text.

The important note is that the emitter resistance for differential amplifiers R_{EE} can be split into two emitter resistance connected in parallel each with a value of $2R_{EE}$ as shown in Figure 4.

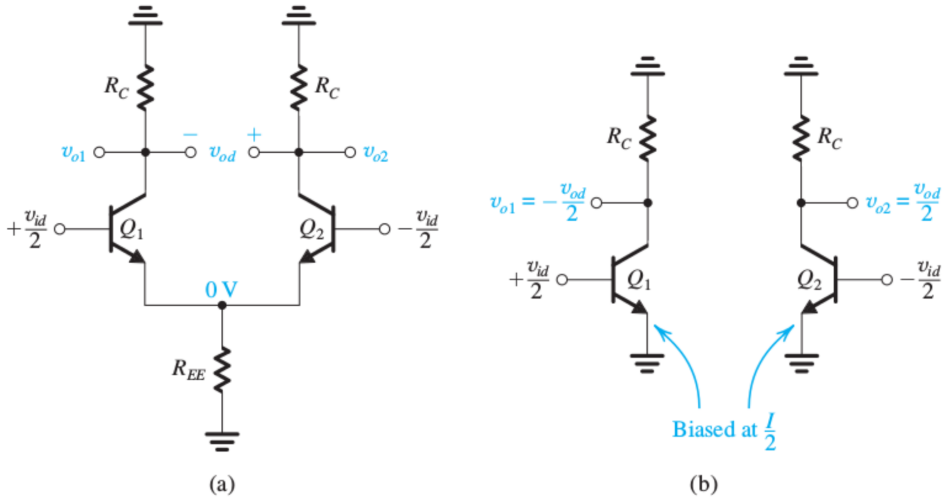

Figure 1: The symmetry of the circuit and the input signal means that there is a virtual ground between the two transistors at the emitters. The emitter voltage should be zero as in (a), and it can be replaced by a ground as shown in (b) (Courtesy of Sedra and Smith).

When the amplifier is differentially driven, then the line of central symmetry can be replaced by a virtual ground as shown in Figure 5(a). Then the analysis proceeds as have been shown in the lecture from Sedra and Smith in yhr preceeding section, as shown in Figure 5(b).

When the differential amplifier is driven in common mode, then no current flows through the central line of symmetry, and the points along this line can be replaced by open circuits as shown in Figure 6.

This analogy is true for both DC and AC signals. Hence, this half-circuit can be used for Q-point (quiescent-point) analysis, as well as DC and AC common mode inputs as shown in Figure 7.

As has been shown, for common mode input, the DC input can range over positive and negative values. Without loss of generality, it can be set to zero as shown in Figure 7(a). But a general DC common mode input is shown in Figure 7(b). Figure 7(c) shows the model for small-signal analysis. It is seen that the half-circuit represented by Figure 7(c) is the common-emitter amplifier with emitter resistance which has been studied before.

2 Common-Mode Rejection

In this section, we will focus on the common-mode rejection of differential amplifiers. For a perfectly matched differential amplifier, the common-mode signals are exactly canceled out. We will study the case when the design of the amplifier is not completely symmetrical or matched, and how the imperfections will

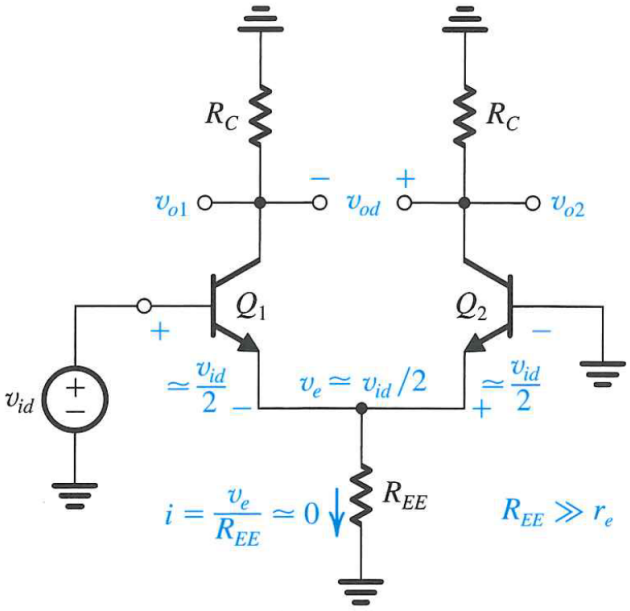

Figure 2: An asymmetrically driven differential amplifier, but with a very large R_{EE}. For small v_{id}, an approximate virtual ground can be assumed at the emitter terminals (Courtesy of Sedra and Smith).

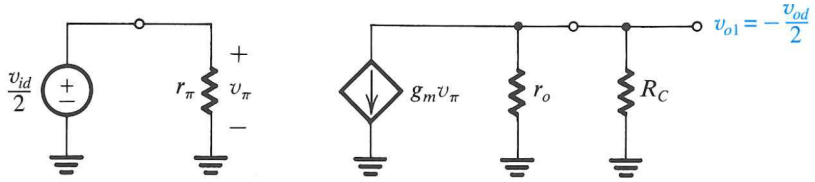

Figure 3: A hybrid-π model of the half-circuit of a differential amplifier for differential gain analysis. The transistor is assumed to have an output resistor r_o (Courtesy of Sedra and Smith).

influence the common-mode rejection.

2.1 The MOS Case

As shown in Figure 8, for small signal analysis, we can replace the voltage source with short circuits in the analysis, and assume a small v_{icm} on top the the background common-mode voltage V_{CM}. Using the equivalent circuit model, it is seen that

$$v_{icm} = \frac{i}{g_m} + 2iR_{SS}, \text{ or } i = \frac{v_{icm}}{1/g_m + 2R_{SS}} \tag{2.1}$$

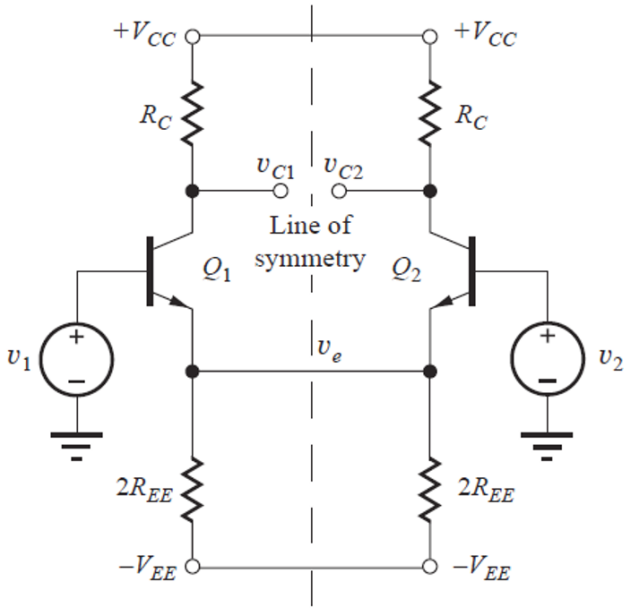

Figure 4: Circuit emphasizing symmetry of the differential amplifier (Courtesy of Jaeger and Blalock).

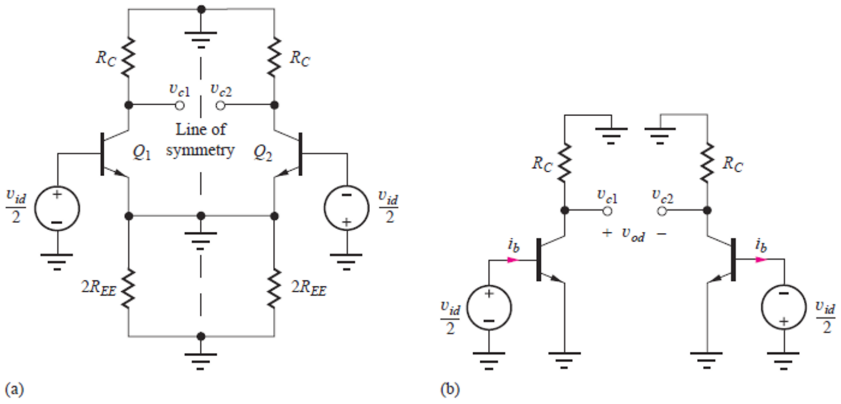

Figure 5: (a) AC grounds for differential-mode input. (b) Differential half-circuits (Courtesy of Jaeger and Blalock).

We can next find that

$$v_{o1} = v_{o2} = -R_D i = -\frac{R_D}{1/g_m + 2R_{SS}} v_{icm} \approx -\frac{R_D}{2R_{SS}} v_{icm} \tag{2.2}$$

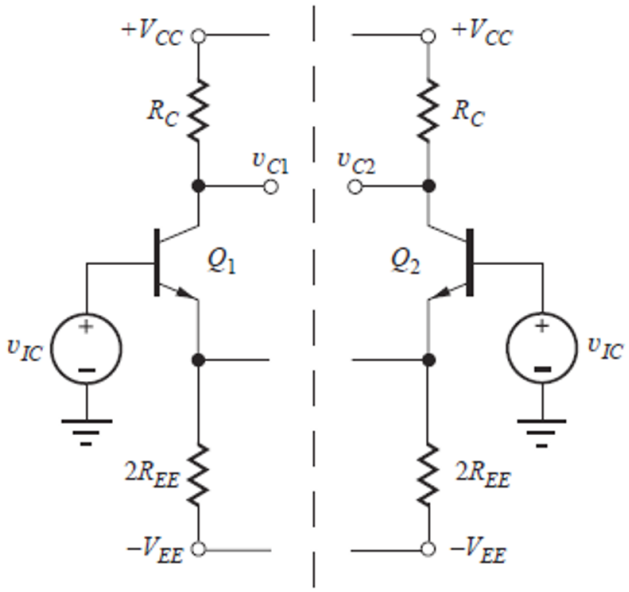

Figure 6: Construction of the common-mode half-circuit (Courtesy of Jaeger and Blalock).

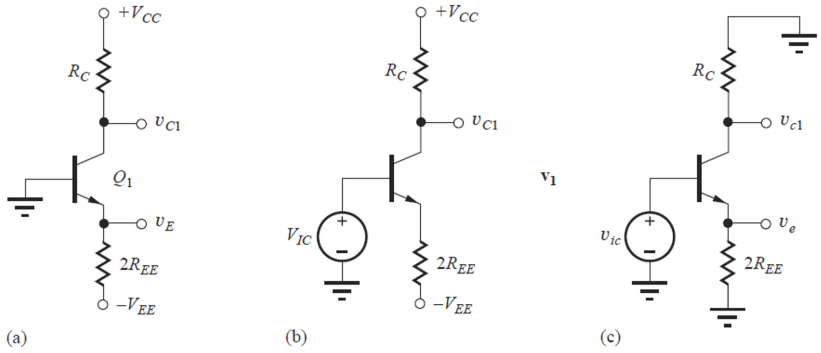

Figure 7: Common-mode half-circuits for (a) Q-point analysis, (b) DC common-mode input, and (c) common-mode signal analysis (Courtesy of Jaeger and Blalock).

where $2R_{SS} \gg 1/g_m$ has been assumed.

2.1.1 Effect of Mismatch

The critical thing to study here is that if the two R_D's are mismatched, namely, the load of Q_1 is R_D while that of Q_2 is $R_D + \Delta R_D$. Then following the above

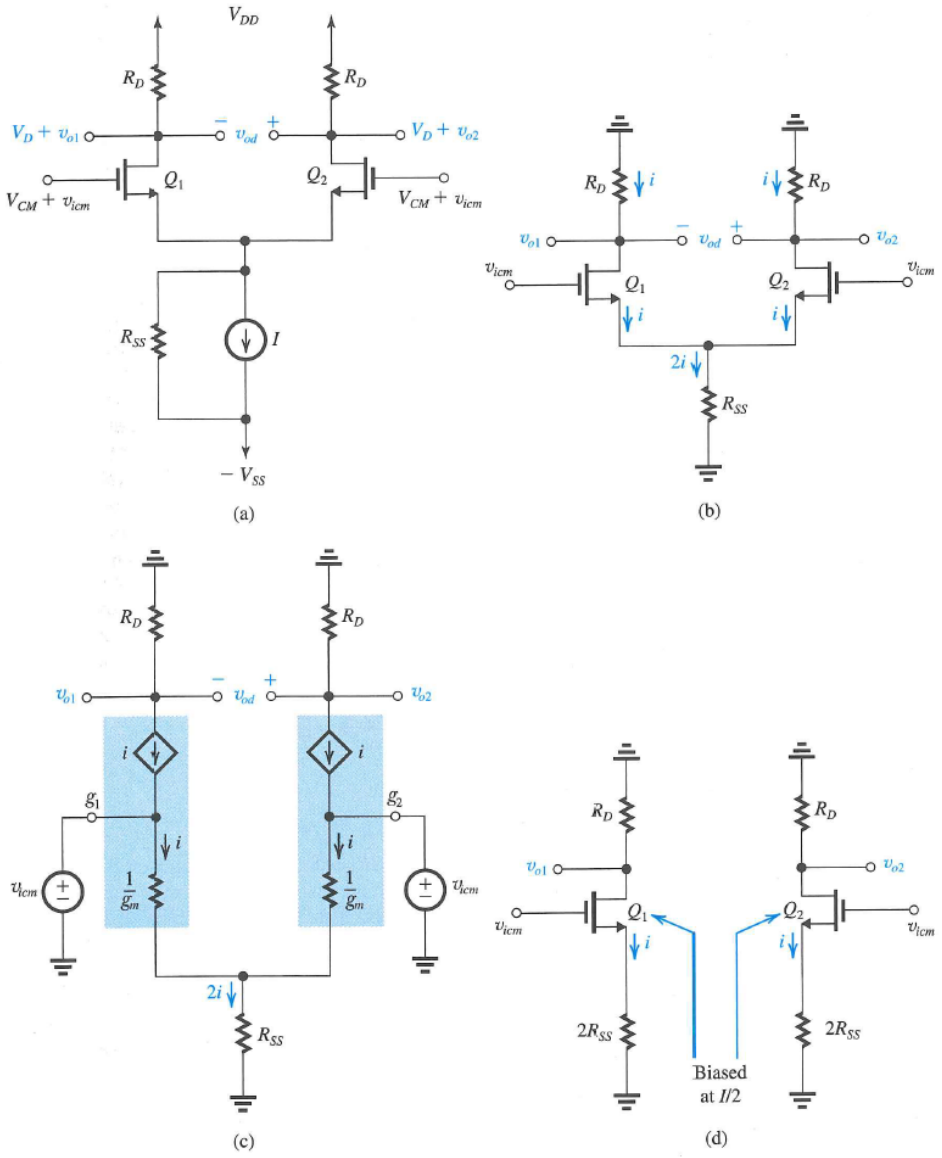

Figure 8: Small-signl analysis of the MOS differential amplifier: (a) The circuit with DC biases in place. (b) The small-signal circuit of the differential amplifier with DC biased removed. (c) The T-model equivalent circuit of the differential amplifier (Courtesy of Sedra and Smith).

analysis,

$$v_{o1} \approx -\frac{R_D}{2R_{SS}} v_{icm}, \text{ and } v_{o2} \approx -\frac{R_D + \Delta R_D}{2R_{SS}} v_{icm} \tag{2.3}$$

Thus the differential voltage output now, due to a small common mode signal, v_{icm}, is

$$v_{od} = v_{o2} - v_{o1} = -\frac{\Delta R_D}{2R_{SS}} v_{icm} \tag{2.4}$$

The **common-mode gain** due to this imperfection is then

$$A_{cm} = \frac{v_{od}}{v_{icm}} = -\frac{\Delta R_D}{2R_{SS}} = -\left(\frac{R_D}{2R_{SS}}\right)\left(\frac{\Delta R_D}{R_D}\right) \tag{2.5}$$

The desirable signal is the output of the differential signal, while the undesirable signal is the output of the common-mode disturbance. The term **common-mode rejection ratio (CMRR)** is defined as

$$\text{CMRR} = \frac{|A_d|}{|A_{cm}|} \tag{2.6}$$

and when expressed in decibel, it is

$$\text{CMRR(dB)} = 20 \log_{10} \frac{|A_d|}{|A_{cm}|} \tag{2.7}$$

Recall that the differential mode voltage gain is $g_m R_D$, then the common-mode rejection ratio can be written as

$$\text{CMRR} = (2g_m R_{SS}) \Big/ \left(\frac{\Delta R_D}{R_D}\right) \tag{2.8}$$

It is seen that a source with large R_{SS} will increase this ratio, as well as a design with small ΔR_D or small mismatched.

2.1.2 Effect of g_m Mismatch on CMRR

If the transconductance of the two transistors are not matched, it can be shown that the gain for the common-mode disturbance is

$$A_{cm} \approx \left(\frac{R_D}{2R_{SS}}\right)\left(\frac{\Delta g_m}{g_m}\right) \tag{2.9}$$

and the corresponding CMRR will be

$$\text{CMRR} = (2g_m R_{SS}) \Big/ \left(\frac{\Delta g_m}{g_m}\right) \tag{2.10}$$

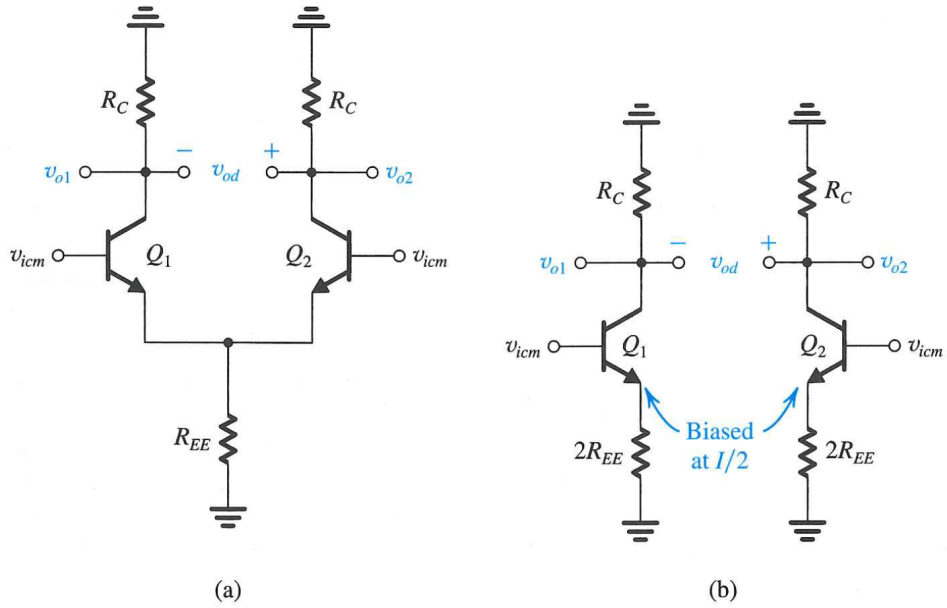

Figure 9: (a) The differential amplifier fed by a common-mode input signal v_{icm}. (b) Equivalent "half-circuits" for common-mode analysis (Courtesy of Sedra and Smith).

2.2 The BJT Case

The BJT differential amplifier is shown in Figure 9. It can be shown that

$$v_{o1} = v_{o2} = -\frac{\alpha R_C}{r_e + 2R_{EE}} v_{icm} \tag{2.11}$$

Hence, the common mode signal is completely rejected when a differential signal is taken at the output. However, when the two circuits are not perfectly matched, for instance, having a slightly mismatched R_C, then the differential output is not zero, and one gets

$$A_{cm} = \frac{v_{od}}{v_{icm}} = -\frac{\alpha \Delta R_C}{2R_{EE} + r_e} \tag{2.12}$$

With $\alpha \approx 1$, the above becomes

$$A_{cm} \approx -\left(\frac{R_C}{2R_{EE}}\right)\left(\frac{\Delta R_C}{R_C}\right) \tag{2.13}$$

Using the fact that the differential gain is

$$A_d = \frac{\alpha(2R_C)}{2r_e + 2R_{EE}} \approx \frac{R_C}{R_{EE}} \tag{2.14}$$

then the CMRR is[1]

$$\text{CMRR} = 2 \Big/ \left(\frac{\Delta R_C}{R_C}\right) \tag{2.15}$$

[1] There seems to be an error with the textbook formula (9.95).