ECE 255, Differential Amplifiers, Cont.

29 March 2018

In this lecture, we continue to study differential amplifiers, with emphasis on small signal analysis followed by BJT differential amplifiers.

1 MOS Differential Amplifier, Cont.

1.1 Small-Signal Analysis

To operate the differential amplifier in the linear regime, it has to operate with small signal input. Figure 1(a) is the differential amplifer with a small signal superimposed on top of at DC common-mode signal V_{CM}. The input signals are

$$v_{G1} = V_{CM} + \frac{1}{2}v_{id}, \qquad v_{G2} = V_{CM} - \frac{1}{2}v_{id} \tag{1.1}$$

Then without loss of generality, one can set $V_{CM} = 0$, and get the small signal model shown in Figure 1(b). The transistor circuit can be further simplified with T-model equivalent circuit to arrive at Figure 1(c).

The differential input signal is applied in an **anti-symmetric** or **complementary** manner as shown. Also, by symmetry, because of the way the amplifier is driven by anti-symmetric signals, the voltage midway between the two amplifiers must be zero making a **virtual ground**.

From (7.42) of Sedra and Smith, or from the previous supplementary notes,

$$g_m = \frac{2I_D}{V_{OV}} = \frac{2(I/2)}{V_{OV}} = \frac{I}{V_{OV}} \tag{1.2}$$

Notice that due to symmetry, a virtual ground is established at the location of the original current source. Finally, using the transconductance, one obtains that

$$v_{o1} = -g_m\frac{v_{id}}{2}R_D, \qquad v_{o2} = +g_m\frac{v_{id}}{2}R_D \tag{1.3}$$

$$\frac{v_{o1}}{v_{id}} = -\frac{1}{2}g_m R_D, \qquad \frac{v_{o2}}{v_{id}} = +\frac{1}{2}g_m R_D \tag{1.4}$$

Or when the differential output is taken, the differential voltage gain proper is

$$A_d = \frac{v_{od}}{v_{id}} = \frac{v_{o2} - v_{o1}}{v_{id}} = g_m R_D \tag{1.5}$$

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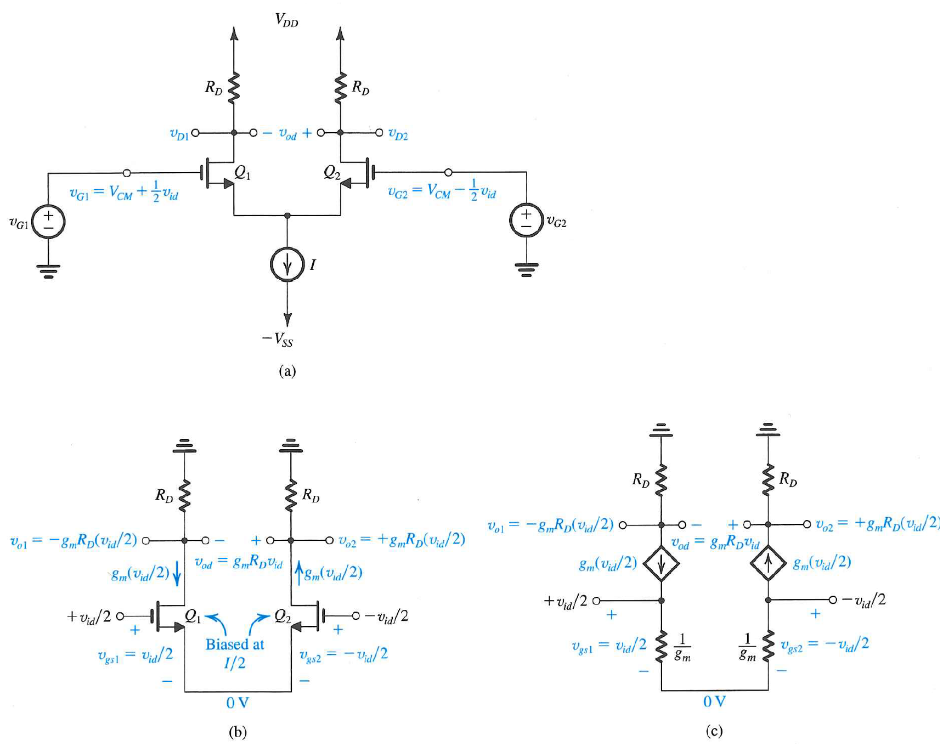

Figure 1: Small-signl analysis of the MOS differential amplifier: (a) The circuit with DC biases in place. (b) The small-signal circuit of the differential amplifier with DC biases removed. (c) The T-model equivalent circuit of the differential amplifier (Courtesy of Sedra and Smith).

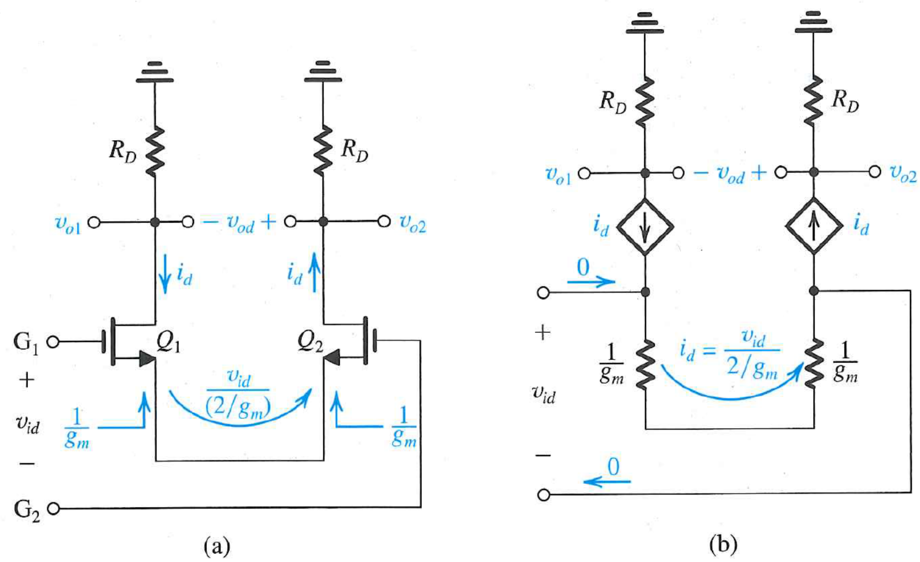

Figure 2: Alternative view of the small-signal analysis where (a) the analysis is done directly on the circuit, (b) the analysis is done on the T-model equivalent circuit (Courtesy of Sedra and Smith).

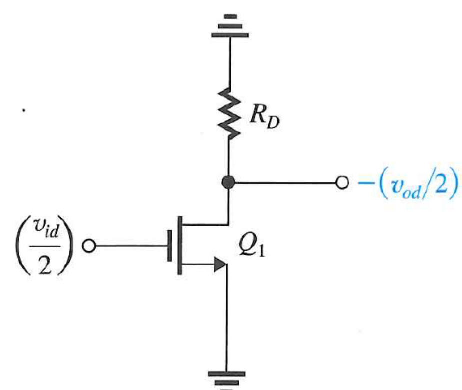

Figure 3: The equivalent differential half-circuit of the model shown in Figure 2(a) (Courtesy of Sedra and Smith).

An alternative way of viewing the above analysis is to use the model shown in Figure 2. When a total voltage v_{id} is applied between gates G_1 and G_2, then the impedance seen by this voltage is $2/g_m$. And the current produced is $(g_m/2)v_{id}$, and the voltage $v_{o1} = -g_m R_D/2$, giving the same result as seen before.

1.1.1 The Differential Half-Circuit

Due to the symmetry of the differential amplifier, a virtual ground can be inserted right in between the two transistors: hence, only a half circuit needs to be analyzed as shown in Figure 3. Then the differential gain is given by

$$A_d = g_m(R_D \parallel r_o) \tag{1.6}$$

where we have assumed the presence of an output resistor r_o to account for the Early effect.

1.1.2 Differential Amplifier with Current-Source Loads

A MOSFET without the Early effect behaves like a current source because changes in V_{DS} does not change I_D. Hence, an appropriately biased MOSFET with the correct gate voltage can be used as a current source. Thus, the load of the differential amplifier can be replaced with a current source which ideally has an infinite internal impedance. Figure 4(a) shows the realization of such current sources with PMOS Q_3 and Q_4.[1] The bias voltage V_G is chosen to ensure a drain current equal to $I/2$. Due to the symmetry of the design, the half-circuit is shown in Figre 4(b). Therefore, the differential gain is given by

$$A_d = \frac{v_{od}}{v_{id}} = g_{m1}(r_{o1} \parallel r_{o3}) \tag{1.7}$$

where the R_D in (1.6) is now replaced by r_{o3}.

2 BJT Differential Pair

The basic configuration of the BJT differential pair is shown in Figure 5, which is very similar to the MOSFET differential pair. Here it is assumed that the transistors are in active mode and not in saturation mode[2]

2.1 Basic Operation

Again, the basic operation of the differential pair is divided into the common mode operation plus a differential mode operation. In other words,

$$v_{B1} = \frac{1}{2}(v_{B1} + v_{B2}) + \frac{1}{2}(v_{B1} - v_{B2}), \qquad v_{B2} = \frac{1}{2}(v_{B1} + v_{B2}) - \frac{1}{2}(v_{B1} - v_{B2}) \tag{2.1}$$

[1] They could equally have been realized with NMOS.

[2] Please note that saturation for BJT is very different in meaning from saturation for MOSFET.

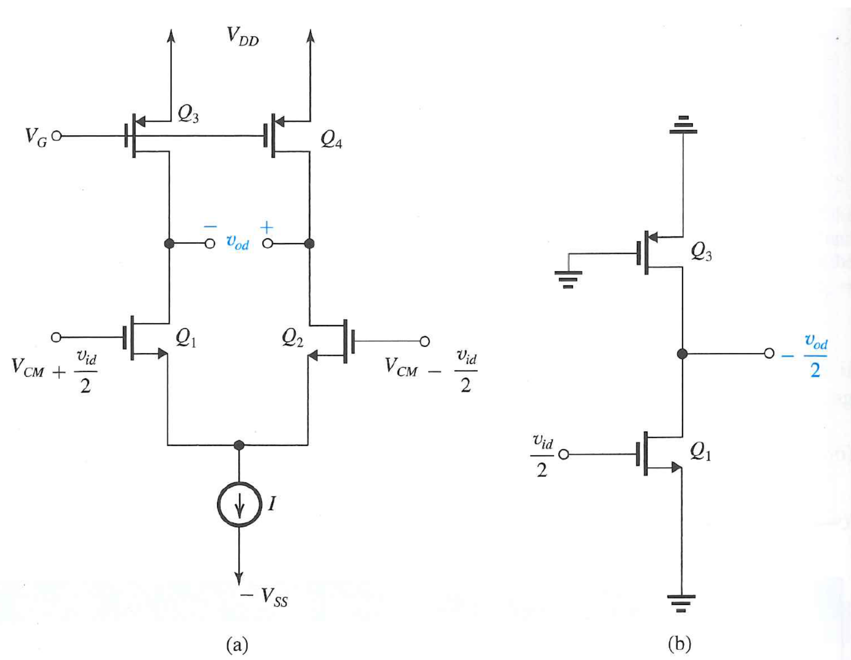

Figure 4: (a) Differential amplifier where the load is replaced by a current source approximated by MOSFETs Q_3 and Q_4. (b) The differential half circuit of (a) (Courtesy of Sedra and Smith).

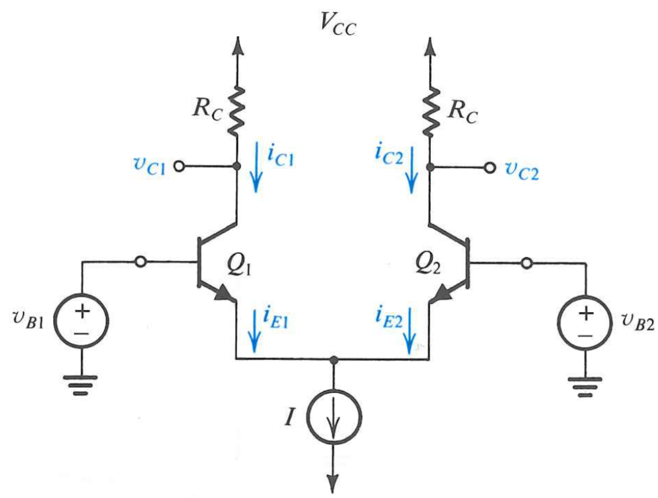

Figure 5: The basic BJT differential-pair configuration (Courtesy of Sedra and Smith).

The above can be rewritten as

$$v_{B1} = V_{CM} + \frac{1}{2}v_{id}, \qquad v_{B2} = V_{CM} - \frac{1}{2}v_{id} \tag{2.2}$$

or that the inputs at the bases can be written as a sum and difference of the two inputs at the two bases, the sum of which is twice the common-mode voltage V_{CM}, and the difference of which is the differential input voltage.

When the transistors are matched, then $i_{E1} = i_{E2} = I/2$. Then the currents through the emitters are $\alpha I/2$ for each branch and the voltage at the collector is then by KVL,

$$V_C = V_{CC} - \frac{1}{2}\alpha I R_C$$

The difference voltage at the collectors is zero due to symmetry.

Figure 6 shows the different operation of the BJT differential amplifier. Figure 6(a) shows the common-mode operation of the amplifier. Figure 6(b) shows that when a large positive base voltage of +1 V is applied at transistor Q_1, it is turned on when transistor Q_2 is turned off. On the other hand, when large negative base voltage of −1 V is applied at transistor Q_1, Q_1 is turned off while Q_2 is turned on as shown in Figure 6(c). Figure 6(d) shows a small signal operation of the BJT differential amplifier.

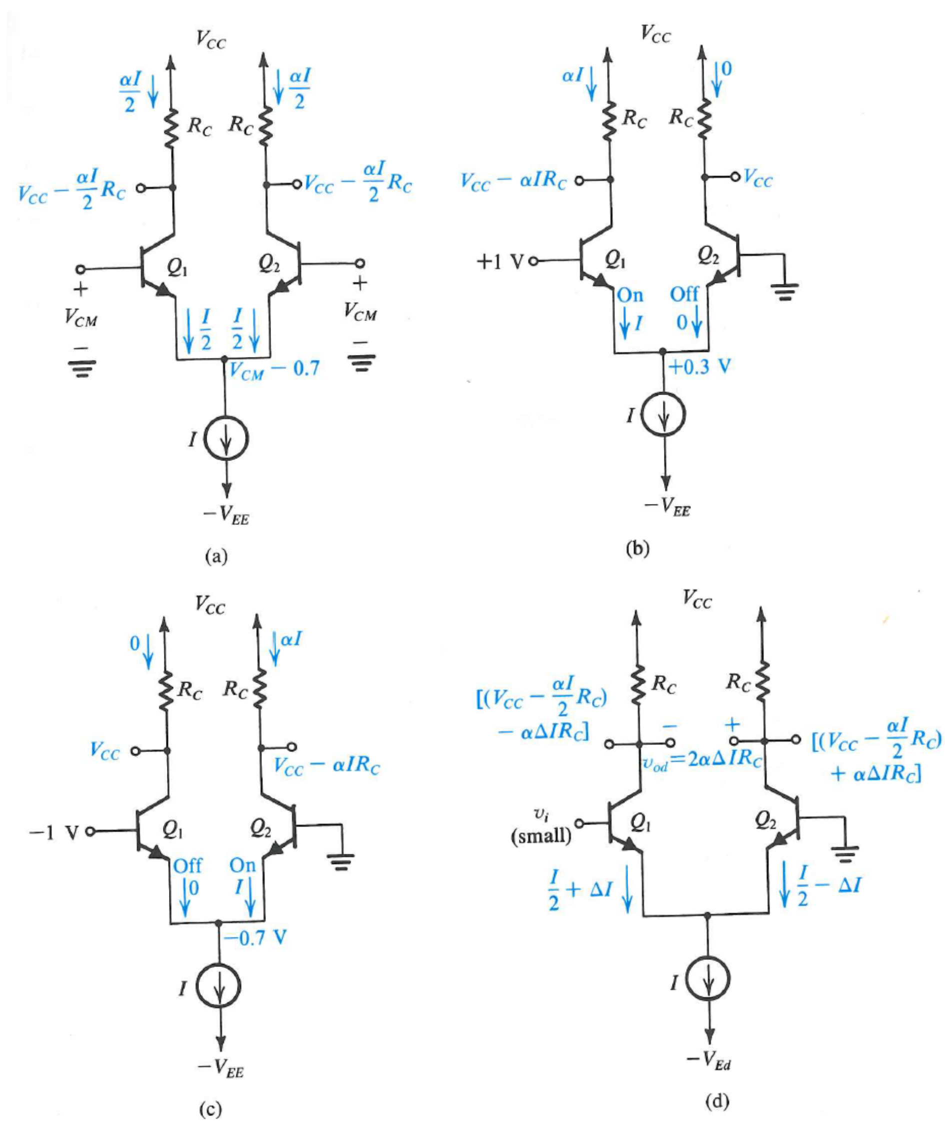

Figure 6: Different operational modes of the BJT differential amplifier: (a) The common-mode operation. (b) The differential mode wih Q_2 off and Q_1 on with $V_{CM} = 0$. (c) The differential mode wih Q_1 off and Q_2 on with $V_{CM} = 0$. (d) The small-signal differential mode operation with $V_{CM} = 0$ (Courtesy of Sedra and Smith).

2.2 Input Common-Mode Range

To investigate the range over which the transistors remain in the active mode, we remind ourselves of the following figure, as shown in Figure 7 (from previous lecture notes, or Figure 6.8 of Sedra and Smith). In order to remain in the active mode, the CBJ should not be forward biased but in reverse biased. So the collector-base voltage should not be more negative than -0.4 V for an *npn* transistor. Thus, one gets

$$V_{CM\max} \approx V_C + 0.4 = V_{CC} - \alpha\frac{I}{2}R_C + 0.4 \tag{2.3}$$

in order for the CBJ not to become forward biased.

On the other hand, the current source I in the circuit needs a certain minimum V_{CS} to ensure its proper operation. Thus,

$$V_{CM\min} = -V_{EE} + V_{CS} + V_{BE} \tag{2.4}$$

It is noted that with large values for V_{EE} and V_{CC}, then V_{CM} can have a large range of values from a large negative number to a large positive number.

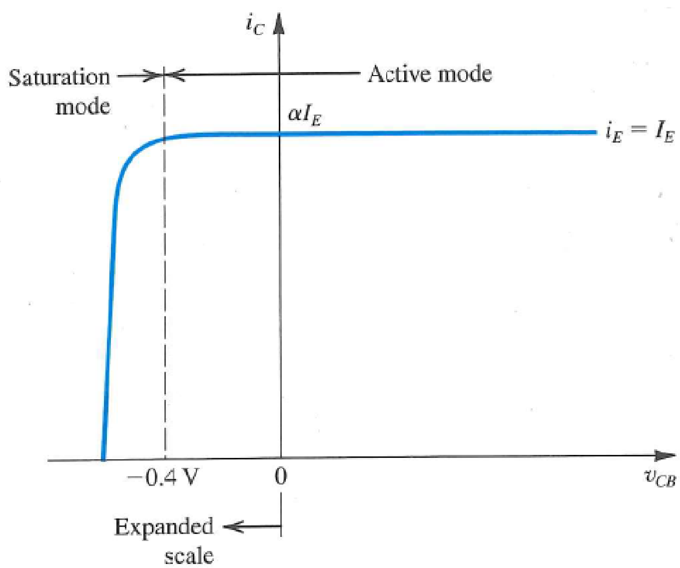

Figure 7: The *i*-*v* characteristic of the CBJ (collector-base junction) showing when the transistor enters a saturation mode (Courtesy of Sedra and Smith).

2.3 Large-Signal Operation

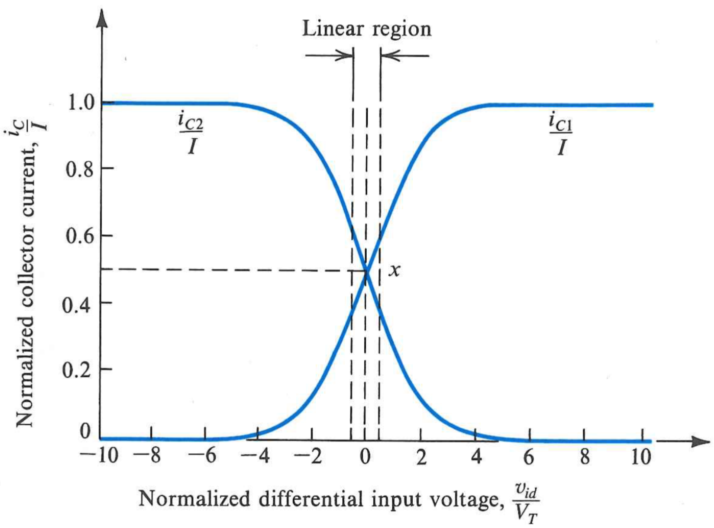

Figure 8: The transfer characteristics of the BJT differential amplifier with $\alpha \approx 1$ (Courtesy of Sedra and Smith).

Recall that in a BJT, the collector current is given by $i_C = I_S e^{v_{BE}/V_T}$, and that the emitter and collector currents are related by the ratio α, i.e., $\alpha i_E = i_C$. Then the emitter currents, applied specifically to the differential amplifier, are

$$i_{E1} = \frac{I_S}{\alpha} e^{(v_{B1} - v_E)/V_T}, \qquad i_{E2} = \frac{I_S}{\alpha} e^{(v_{B2} - v_E)/V_T} \tag{2.5}$$

which implies that

$$\frac{i_{E1}}{i_{E2}} = e^{(v_{B1} - v_{B2})/V_T} \tag{2.6}$$

From it, one gets

$$\frac{i_{E1}}{i_{E1} + i_{E2}} = \frac{1}{1 + e^{(v_{B2} - v_{B1})/V_T}}, \qquad \frac{i_{E2}}{i_{E1} + i_{E2}} = \frac{1}{1 + e^{(v_{B1} - v_{B2})/V_T}} \tag{2.7}$$

Since $i_{E1} + i_{E2} = I$, it follows that

$$i_{E1} = \frac{I}{1 + e^{-v_{id}/V_T}}, \qquad i_{E2} = \frac{I}{1 + e^{+v_{id}/V_T}} \tag{2.8}$$

where $v_{id} = v_{B1} - v_{B2}$.

Because of the exponential relation between the collector current i_C and the base-emitter voltage, the current switches rapidly between the two transistors as shown in Figure 8: A small differential voltage v_{id} of several V_T can enable the switching.

Furthermore, because of the exponential relation of the collector current, the BJT differential pair is very sensitive to the change in the base-emitter voltage of the input voltage. This sensitivity can be reduced by adding emitter resistors R_e to the circuit as shown in Figure 9(a). Figure 9(b)shows the improved linearity of the collector current to the input voltage v_{id} with increasing R_e.

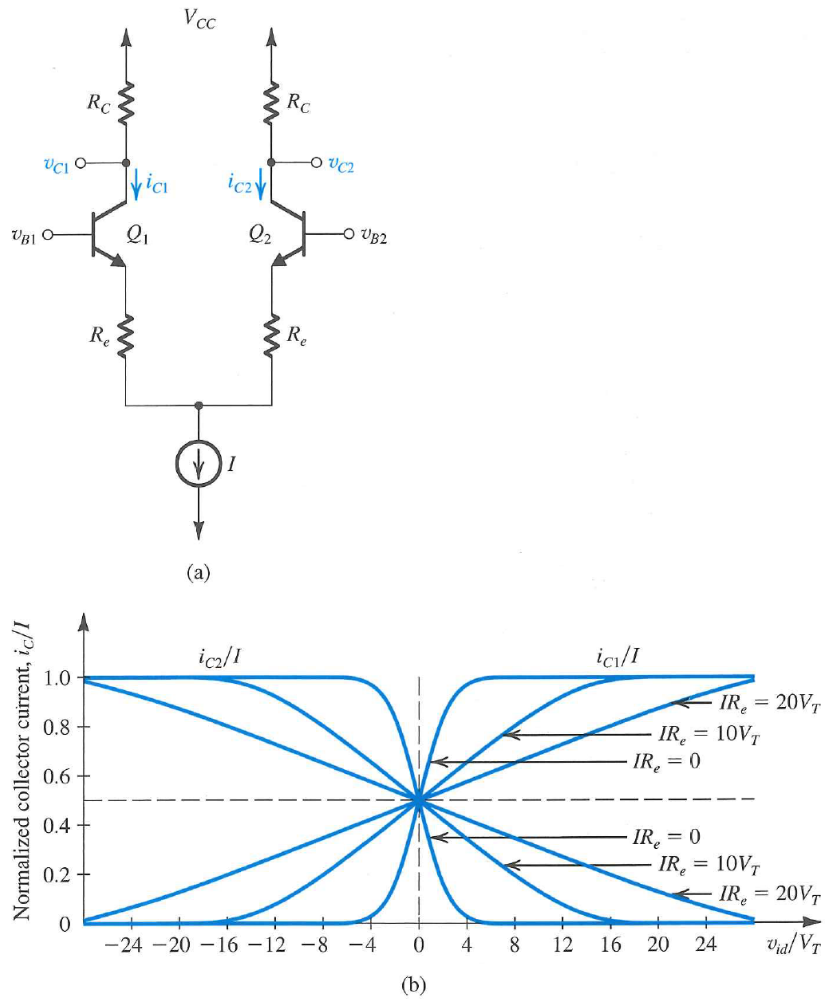

Figure 9: The transfer characteristics of the BJT differential amplifier (b) can be made more linear by adding emitter resistors R_e in the differential pair as shown in (a) (Courtesy of Sedra and Smith).

For the MOSFET case, the linearity can be improved by increasing V_{OV} which is dependent on the geometry of the gate, and it can be changed by altering its geometry. But this cannot be done for BJT; however, the linearity is improved by adding external resistors R_e.

2.4 Small-Signal Operation

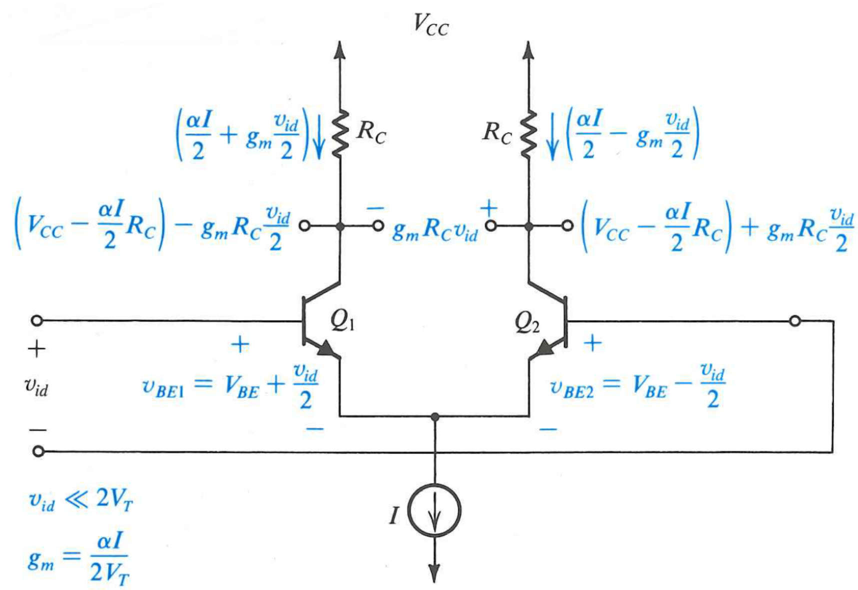

Figure 10: The differential amplifier with the DC bias voltages plus the small differential input signals v_{id} (Courtesy of Sedra and Smith).

Figure 10 shows the small signal model of the BJT differential amplifier. One can show that

$$i_{C1} = \frac{\alpha I}{1 + e^{-v_{id}/V_T}}, \qquad i_{C2} = \frac{\alpha I}{1 + e^{+v_{id}/V_T}} \tag{2.9}$$

The above can be manipulated to become

$$i_{C1} = \frac{\alpha I e^{v_{id}/(2V_T)}}{e^{v_{id}/(2V_T)} + e^{-v_{id}/(2V_T)}}, \qquad i_{C2} = \frac{\alpha I e^{-v_{id}/(2V_T)}}{e^{v_{id}/(2V_T)} + e^{-v_{id}/(2V_T)}} \tag{2.10}$$

Assuming that $v_{id} \ll 2V_T$, and using that $e^x \approx 1 + x$ when x is small, then

$$i_{C1} \approx \frac{\alpha I[1 + v_{id}/(2V_T)]}{1 + v_{id}/(2V_T) + 1 - v_{id}/(2V_T)}, \qquad i_{C2} \approx \frac{\alpha I[1 - v_{id}/(2V_T)]}{1 + v_{id}/(2V_T) + 1 - v_{id}/(2V_T)} \tag{2.11}$$

or

$$i_{C1} \approx \frac{\alpha I}{2} + \frac{\alpha I}{2V_T}\frac{v_{id}}{2}, \text{ and similarly, } i_{C2} \approx \frac{\alpha I}{2} - \frac{\alpha I}{2V_T}\frac{v_{id}}{2} \tag{2.12}$$

In other words, the small signal i_c is

$$i_c \approx \frac{\alpha I}{2V_T}\frac{v_{id}}{2} \tag{2.13}$$

Since $g_m = I_C/V_T = \alpha I/(2V_T)$, the above is just

$$i_c = g_m \frac{v_{id}}{2} \tag{2.14}$$

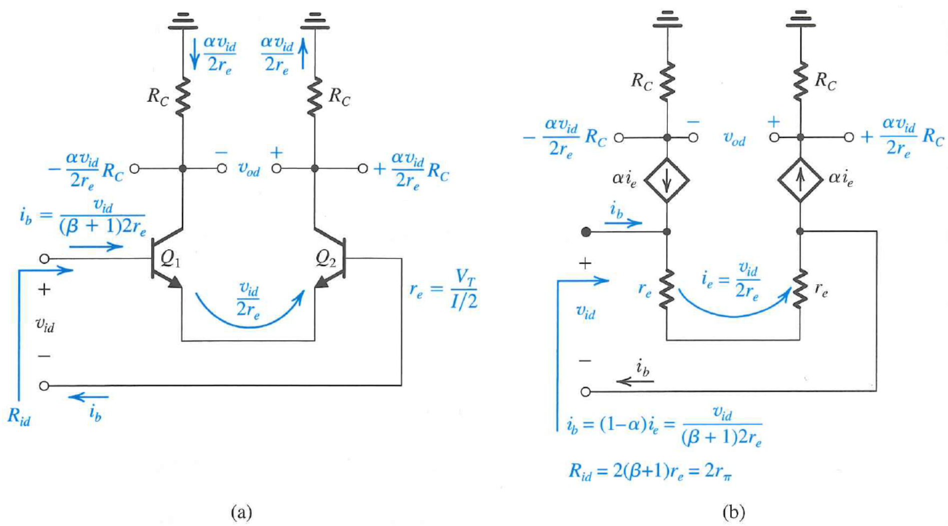

Figure 11: (a) The small signal model of the BJT differential amplifier with the DC bias voltages removed. (b) The T-model equivalent circuit of the small-signal model (Courtesy of Sedra and Smith).

Alternatively, one can look at Figure 11 and see that

$$i_e = \frac{v_{id}}{2r_e} \tag{2.15}$$

Consequently,

$$i_c = \alpha i_e = \frac{\alpha v_{id}}{2r_e} = g_m \frac{v_{id}}{2} \tag{2.16}$$

where $g_m = \alpha/r_e$ have been used.

In the case of Figure 12 when an emitter resistor R_e is added, then

$$i_e = \frac{v_{id}}{2r_e + 2R_e} \tag{2.17}$$

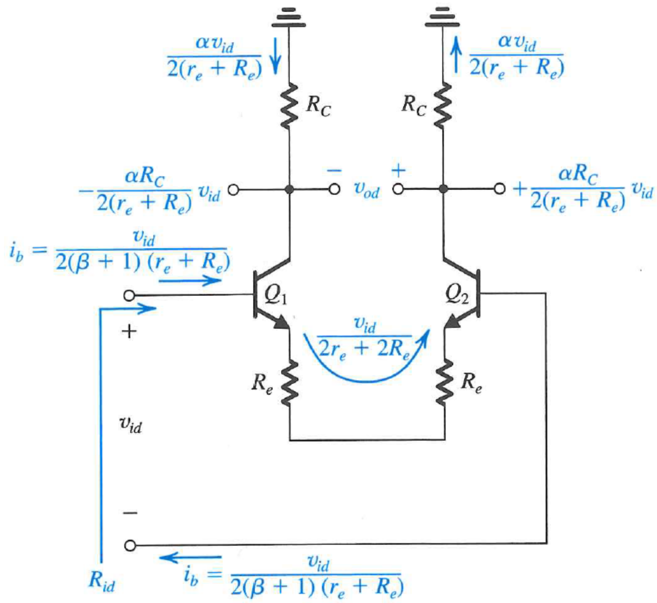

Figure 12: The small signal model of the BJT differential amplifier with the DC bias voltages removed and emitter resistors added (Courtesy of Sedra and Smith).