ECE 255, Differential Amplifiers

27 March 2018

In this lecture, we study differential amplifiers. Because of the cancelation nature of the amplifier, it rejects unwanted noise, called common-mode noise, from the amplifier circuit. For instance, in the previous lecture, we have studied discrete amplifiers where the input has only one terminal. As long as an input voltage is induced at the input terminal, there will be an output voltage at the amplifier output. But there are many remnant electric fields in our environment. These remnant electric fields are generated by other electronic/electrical devices not grounded or shielded properly. These undesirable electric fields appear as noise in the amplifier circuits.

One way to overcome this kind of environmental noise (also called electromagnetic interference (EMI) noise) is to operate amplifiers in pair. One amplifier is to receive only a positive signal, while the other amplifier is to receive only a negative signal. If these two amplifiers are balanced, then the environment noise can be canceled. These are called differential amplifiers as shall be studied.

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1 The MOS Differential Pair

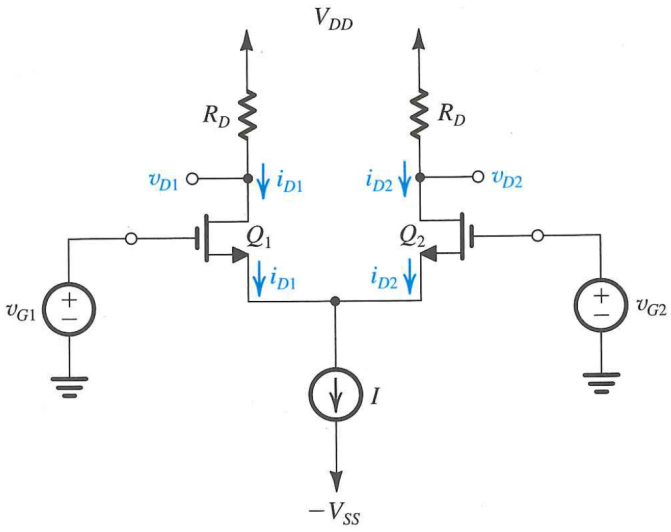

Figure 1: The basic MOSFET differential-pair amplifier configuration (Courtesy of Sedra and Smith).

Figure 1 shows a basic MOS differential amplifier. The two transistor Q_1 and Q_2 are made to be as similar to each other as possible. The current source is assumed ideal with an infinite internal impedance. Two identical resistors R_D are connected to the drain terminals of the MOSFETs, and they are in the saturation regime of operation.

1.1 Common-Mode Input Voltage

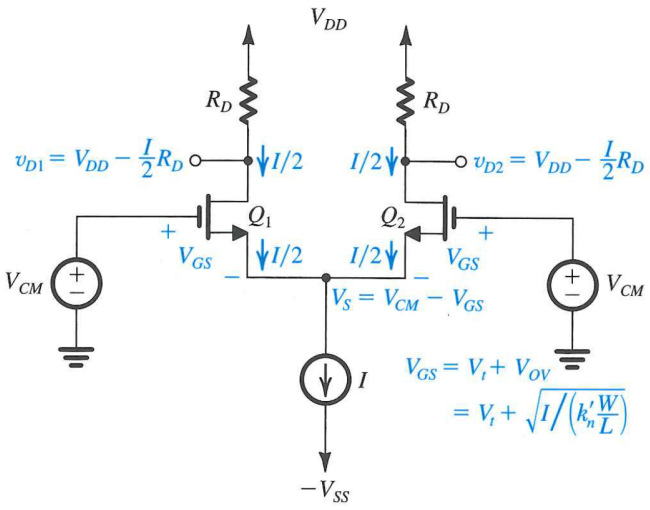

Figure 2: The common-mode operation of the MOSFET differential-pair amplifier configuration (Courtesy of Sedra and Smith).

In this mode, it is assumed that the input voltages to the MOSFETs are equal, namely, that the two gate voltages, $v_{G1} = v_{G2} = V_{CM}$, where V_{CM} is the **common-mode voltage** as shown in Figure 2. Since this circuit is completely symmetrical (an assumption), then $i_{D1} = i_{D2} = I/2$. Then the voltage at the source terminal, which is assumed to be identical for both transistors, is

$$V_S = V_{CM} - V_{GS} \tag{1.1}$$

Neglecting the channel-length modulation effect (Early effect), and that the transistors are in the saturation region, then

$$\frac{I}{2} = \frac{1}{2}k_n'\frac{W}{L}(V_{GS} - V_t)^2 = \frac{1}{2}k_n'\frac{W}{L}V_{OV}^2 \tag{1.2}$$

where the overdrive voltage is V_{OV} is also given by

$$V_{OV} = \sqrt{I/(k_n'(W/L))} \tag{1.3}$$

The voltages at the drain terminals will be identical, namely,

$$v_{D1} = v_{D2} = V_{DD} - \frac{I}{2}R_D \tag{1.4}$$

Hence, there is no difference in the two voltages, and **the differential voltage** is zero. If the common-mode voltage V_{CM} is changed, by symmetry, the differential voltage output is always zero. Therefore, the differential amplifier rejects common-mode voltages.

To keep the transistors in saturation mode, we want $V_{DS} > V_{OV}$. But

$$V_{DS} = V_D - V_S = V_D - (V_{CM} - V_{GS}) = V_{DD} - \frac{I}{2}R_D - (V_{CM} - V_{GS}) > V_{OV} \quad (1.5)$$

Substituting that $V_{OV} = V_{GS} - V_t$, and moving V_{CM} to the right-hand side of the inequality, and V_t to the left-hand side, one gets

$$V_t + V_{DD} - \frac{I}{2}R_D > V_{CM} \quad (1.6)$$

Consequently, to keep the transistors in saturation mode,

$$V_{CM\max} = V_t + V_{DD} - \frac{I}{2}R_D \quad (1.7)$$

Next, if one assumes that a minimum voltage of V_{CS} is needed across the current source for its proper function, then the voltage across the current source, which is $V_S + V_{SS}$ is such that

$$V_S + V_{SS} > V_{CS}, \text{ or } V_S > -V_{SS} + V_{CS} \quad (1.8)$$

From the above, one gets the inequality that

$$V_{CM} = V_G = V_S + V_{GS} \rightarrow V_{CM} > -V_{SS} + V_{CS} + V_{GS} \quad (1.9)$$

Then one gets the bound, after using that $V_{GS} = V_{OV} + V_t$, that

$$V_{CM} \geq V_{CM\min} = -V_{SS} + V_{CS} + V_t + V_{OV} \quad (1.10)$$

Note that the value of $V_{CM\min}$ can be a negative number because $-V_{SS}$ can be a large negative number. Therefore, the common-mode range of operation is given by

$$V_{CM\min} \leq V_{CM} \leq V_{CM\max} \quad (1.11)$$

1.2 Differential Input Voltage

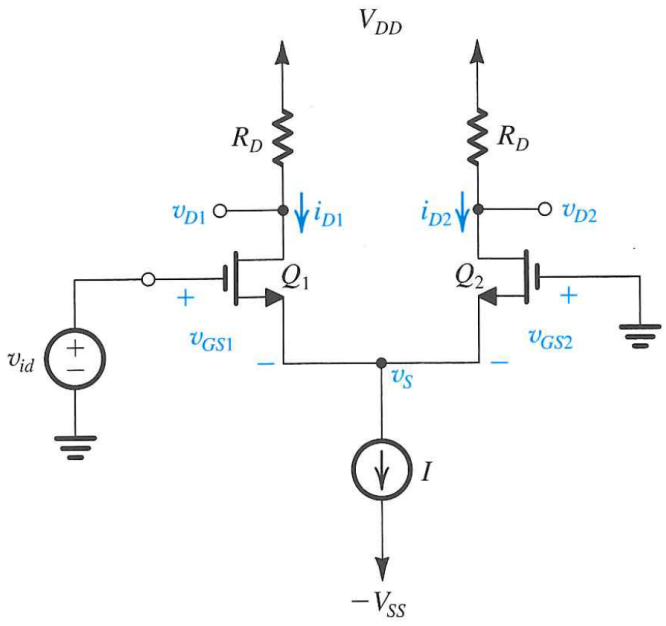

Figure 3: The MOSFET differential-pair amplifier with a differential input signal v_{id}. Without loss of generality, one can assume that the gate of Q_2 is grounded (Courtesy of Sedra and Smith).

Given the inputs v_{G1} and v_{G2}, they can always be expressed in terms of common-mode and differential-mode inputs, viz.,

$$v_{G1} = v_{CM} + v_{DM}, \qquad v_{G2} = v_{CM} - v_{DM} \tag{1.12}$$

For differential amplifier, the output is insensitive to the value of v_{CM} in the ideal case. Hence, it can always be picked that $v_{CM} = v_{DM}$ so that $v_{G2} = 0$ and that $v_{G1} = 2v_{DM}$ without loss of generality. Hence, we can do small-signal analysis by applying a small voltage v_{id} to the gate of Q_1, as shown in Figure 3 and then grounding the gate of Q_2.

Hence, any voltage output at this point is due to the imbalance of the amplifier, or the non-zero value of v_{id}. Here, v_{id} is the **differential input signal**, and it invokes the **differential mode** of the differential amplifier.

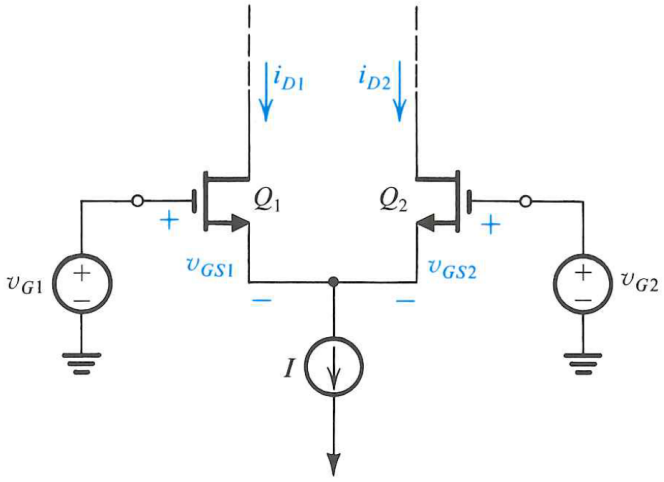

Figure 4: A simplified picture of MOSFET differential-pair amplifier for deriving transfer characteristics (Courtesy of Sedra and Smith).

A simplified picture of the differential pair amplifier is shown in Figure 4. The differential pair is driven by a current source with current $I = I_{D1} + I_{D2}$ such that as v_{id} is increased, one see that the imbalance will increase reaching a point where all the drain current I will flow through Q_1. At this juncture, then

$$I = \frac{1}{2} k_n' \frac{W}{L} (v_{GS1} - V_t)^2 \tag{1.13}$$

Thus

$$v_{GS1} = V_t + \sqrt{2I/k_n'(W/L)} = V_t + \sqrt{2} V_{OV} \tag{1.14}$$

The above V_{OV} is the overdrive voltage corresponding to when the transistor has a drain current of $I/2$ as shown in (1.2). The entire current will be steered into Q_1 when

$$v_{id\max} = v_{GS1} + v_S = V_t + \sqrt{2} V_{OV} - V_t = \sqrt{2} V_{OV} \tag{1.15}$$

In the above, we assume that the transistor Q_2 is completely turned off so that $v_S = -V_t$, with $v_{G2} = 0$. If v_{id} is further increase, then transistor Q_2 is turned off even more, and v_{GS1} remains to be $V_t + \sqrt{2} V_{OV}$ in order to produce the necessary drain current I, but with the additional voltage absorbed by Q_2.

The same thing happens when one sets v_{id} to be negative turning off Q_1 and turning on Q_2. Alternatively, we can shift the common-mode voltage V_{CM} such that gate of Q_1 is grounded and a small signal $|v_{id}|$ is sent to the gate of Q_2. Therefore,

$$-\sqrt{2} V_{OV} \leq v_{id} \leq \sqrt{2} V_{OV} \tag{1.16}$$

where at the extreme ends, the drain current is flowing entirely in one transistor or the other one. The above defines the range for the differential mode operation of the differential amplifier. The transistors are assume to be in saturation mode.

1.3 Large Signal Operation

Next, one derives the large signal operation of the differential amplifier for two different drain current i_{D1} and i_{D2} when a differential voltage is applied at the gates, namely $v_{id} = v_{G1} - v_{G2}$.

To begin, assuming saturation-region operation, the drain currents for Q_1 and Q_2 are

$$i_{D1} = \frac{1}{2}k'_n \frac{W}{L}(v_{GS1} - V_t)^2, \qquad i_{D2} = \frac{1}{2}k'_n \frac{W}{L}(v_{GS2} - V_t)^2 \tag{1.17}$$

Taking the square roots of these equations, one obtains

$$\sqrt{i_{D1}} = \sqrt{\frac{1}{2}k'_n \frac{W}{L}}(v_{GS1} - V_t), \qquad \sqrt{i_{D2}} = \sqrt{\frac{1}{2}k'_n \frac{W}{L}}(v_{GS2} - V_t) \tag{1.18}$$

Taking the difference of these equations, and letting

$$v_{GS1} - v_{GS2} = v_{G1} - v_{G2} = v_{id}$$

squaring the sum of the above equations, and assuming that

$$i_{D1} + i_{D2} = I$$

one arrives at the following equation that

$$2\sqrt{i_{D1} i_{D2}} = I - \frac{1}{2}k'_n \frac{W}{L} v_{id}^2 \tag{1.19}$$

One can let $i_{D2} = I - i_{D1}$ in the above, square the above equation, solve the ensuing quadratic equation to get

$$i_{D1} = \frac{I}{2} \pm \sqrt{k'_n \frac{W}{L} I}\left(\frac{v_{id}}{2}\right)\sqrt{1 - \frac{(v_{id}/2)^2}{I/(k'_n \frac{W}{L})}} \tag{1.20}$$

One can have a sanity check to decide on which of the $\pm$ should be taken in the above equation. For small-signal analysis, incrementing v_{id} will only increase i_{D1}; hence, only the + sign is acceptable above. The physical answer is

$$i_{D1} = \frac{I}{2} + \sqrt{k'_n \frac{W}{L} I}\left(\frac{v_{id}}{2}\right)\sqrt{1 - \frac{(v_{id}/2)^2}{I/(k'_n \frac{W}{L})}} \tag{1.21}$$

The corresponding value of $i_{D2} = I - i_{D1}$ yielding

$$i_{D2} = \frac{I}{2} - \sqrt{k'_n \frac{W}{L} I}\left(\frac{v_{id}}{2}\right)\sqrt{1 - \frac{(v_{id}/2)^2}{I/(k'_n \frac{W}{L})}} \tag{1.22}$$

Again, as a check, the common-mode result should be obtained when $v_{id} = 0$, leading to

$$i_{D1} = i_{D2} = \frac{I}{2}, \qquad v_{GS1} = v_{GS2} = V_{GS} \tag{1.23}$$

where this particular $I/2$ is the common-mode $I/2$ given by

$$\frac{I}{2} = \frac{1}{2}k'_n \frac{W}{L}(V_{GS} - V_t)^2 = \frac{1}{2}k'_n \frac{W}{L}V_{OV}^2 \tag{1.24}$$

From the above, one notes that I/V_{OV}^2 can be used to eliminate $k'_n(W/L)$, and the above equations in (1.21) and (1.22) can be rewritten as

$$i_{D1} = \frac{I}{2} + \left(\frac{I}{V_{OV}}\right)\left(\frac{v_{id}}{2}\right)\sqrt{1 - \left(\frac{v_{id}/2}{V_{OV}}\right)^2} \tag{1.25}$$

$$i_{D2} = \frac{I}{2} - \left(\frac{I}{V_{OV}}\right)\left(\frac{v_{id}}{2}\right)\sqrt{1 - \left(\frac{v_{id}/2}{V_{OV}}\right)^2} \tag{1.26}$$

Notice that in the above, the relationship between the drain current and the differential voltage input is nonlinear. The normalized plots of i_{Di}/I, $i = 1, 2$, versus v_{id}/V_{OV} are shown in Figure 5. These plots express the salient feature of a differential pair MOS amplifiers. When the differential input signal is small, the differential amplifier displays linear behavior but not when the input signal is large.

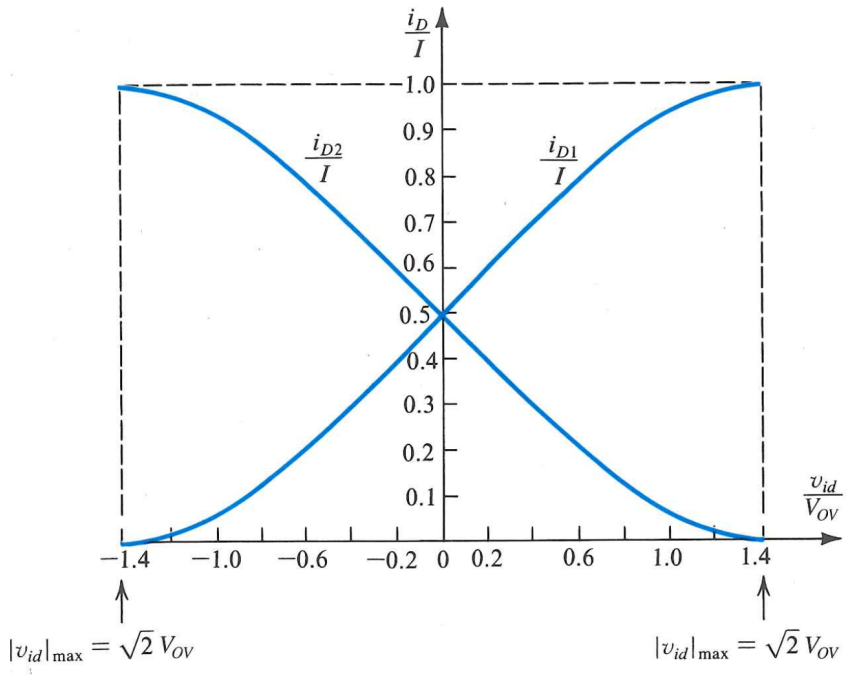

Figure 5: Normalized plots of the currents in a MOSFET differential-pair amplifier. The V_{OV} here is the overdrive voltage when the drain current is $I/2$ (Courtesy of Sedra and Smith).

Assuming small signals, one can arrive at the following linearization approximations, namely,

$$i_{D1} \approx \frac{I}{2} + \frac{I}{V_{OV}} \frac{v_{id}}{2}, \qquad i_{D2} \approx \frac{I}{2} - \frac{I}{V_{OV}} \frac{v_{id}}{2} \tag{1.27}$$

In other words, there is a small differential current that is proportional to the differential voltage input v_{id}, i.e.,

$$i_d = \frac{I}{V_{OV}} \frac{v_{id}}{2} \tag{1.28}$$

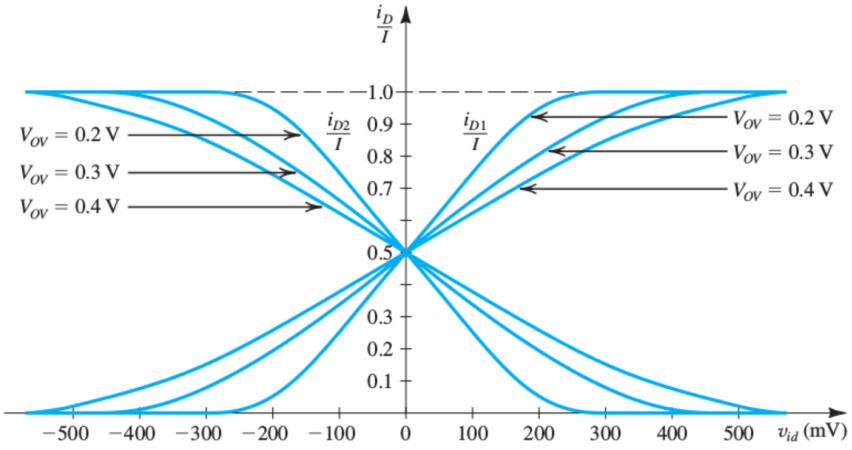

Figure 6: Similar plots to Figure 5 showing their dependence on V_{OV}. Enlarging V_{OV} makes the problem more linear (Courtesy of Sedra and Smith).

Figure 6 shows the dependence of the i-v plots of the differential amplifier for different V_{OV}. A larger V_{OV} is seen to improve the linearity of the amplifier at the expense of reducing the gain. When the transistor is in saturation mode, the drain current is related to the overdrive voltage by

$$I_D = \frac{1}{2} k'_n \frac{W}{L} V_{OV}^2 \tag{1.29}$$

To maintain the same drain current, the overdrive voltage V_{OV} can be increased by decreasing W/L. Since the transconductance is given by

$$g_m = \sqrt{2k'_n (W/L) I_D} \tag{1.30}$$

decreasing W/L will decrease the transconductance lowering the gain of the amplifier.