

# ECE 255

14 September 2017

In this lecture, the DC analysis of BJT will be discussed.

## 1 BJT Circuits at DC

It is important that circuit designers gain physical insight into the working of the circuit with speedy analysis. Later, if needed, more elaborate analysis can be done with commercial software such as SPICE. For DC analysis of circuits, the following assumptions are made:

- The  $|V_{BE}|$  of a transistor is 0.7 V, and the  $|V_{CE}|$  of a saturated transistor is 0.2 V.
- The Early effect is ignored.

Next, a designer has to decide:

- Which mode is the transistor operating in? Cut-off, active, or saturation (conducting)?
- Is  $V_{CB}$  of an *npn* transistor  $> -0.4$  V, or  $V_{CB}$  of a *pn*p transistor  $< 0.4$  V? This decides if the transistor is in active or saturation mode. Then the model in Figure 1 is used accordingly.

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### Example 1.<sup>1</sup>

For the circuit shown in Figure 2(a), with Figure 2(b) indicating what the actual rig-up is, one wishes to find all the node voltages and branch currents. Here,  $\beta$  is assumed to be 100.

#### Solution

As seen, the base-emitter junction is forward biased. Assuming a turn-on voltage of 0.7 V, then the emitter voltage is

$$V_E = 4 - V_{BE} \approx 4 - 0.7 = 3.3 \text{ V} \quad (1.1)$$

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<sup>1</sup>Example 6.4 of textbook.

Table 6.3 Simplified Models for the Operation of the BJT in DC Circuits		
	<i>nnp</i>	<i>ppp</i>
Active EBJ: Forward Biased		
CBJ: Reverse Biased		
Saturation EBJ: Forward Biased		
CBJ: Forward Biased		

Figure 1: Simplified model of a BJT in DC circuits (Courtesy of Sedra and Smith).

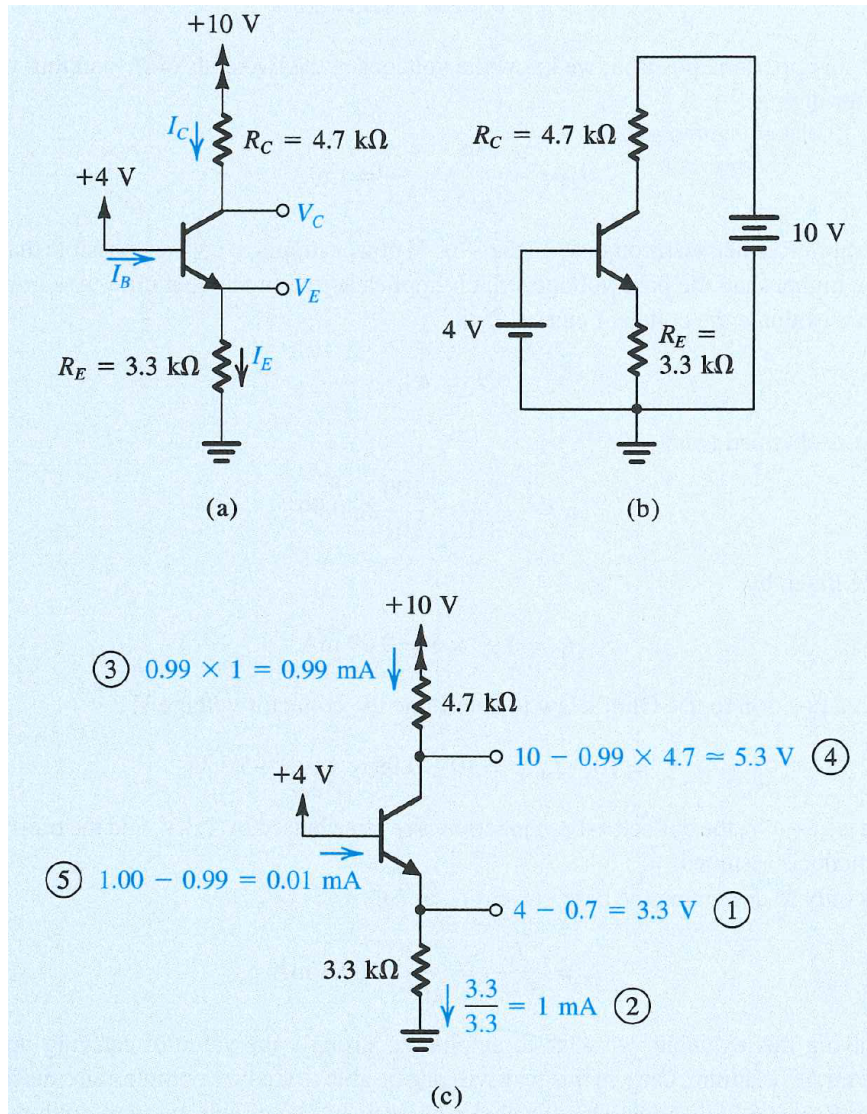


Figure 2: The circuit is shown in (a). A rig up is shown in (b). The steps to solving the problem is shown in (c) (Courtesy of Sedra and Smith).

Then the current through  $R_E$  is

$$I_E = \frac{V_E - 0}{R_E} = \frac{3.3}{3.3} = 1 \text{ mA} \quad (1.2)$$

Assume that the transistor is in active mode, then

$$I_C = \alpha I_E = \frac{\beta}{\beta + 1} I_E = \frac{100}{101} I_E \approx 0.99 \times 1 = 0.99 \text{ mA} \quad (1.3)$$

From Ohm's law,

$$V_C = 10 - I_C R_C = 10 - 0.99 \times 4.7 \approx 5.3 \text{ V} \quad (1.4)$$

This does prove that the transistor is in active mode.

To determine the base current, then

$$I_B = \frac{I_E}{\beta + 1} = \frac{1}{101} \approx 0.01 \text{ mA} \quad (1.5)$$

The analysis steps are emphasized in Figure 2(c).

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**Example 2.**<sup>2</sup>

Next, the circuit shown in Figure 3(a) is analyzed, where the base voltage is zero, or grounded.

**Solution**

Looking at the figure, the EBJ is reverse biased, so is the ECJ. So the transistor is in the cut-off mode. No current is flowing through the transistor.

Since no current flows through the transistor, there is no voltage drop through  $R_E$  and  $R_C$ , and the voltages are as shown in Figure 3(b).

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**Example 3.**<sup>3</sup>

The example shown in Figure 4 is analyzed here with  $\beta = 100$ .

**Solution**

The base-emitter junction is clearly forward biased, yielding

$$I_B = \frac{+5 - V_{BE}}{R_B} \approx \frac{5 - 0.7}{100} = 0.043 \text{ mA} \quad (1.6)$$

Assume that the transistor is in active mode, then

$$I_C = \beta I_B = 100 \times 0.043 = 4.3 \text{ mA} \quad (1.7)$$

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<sup>2</sup>Example 6.6 of textbook.

<sup>3</sup>Example 6.8 of textbook.

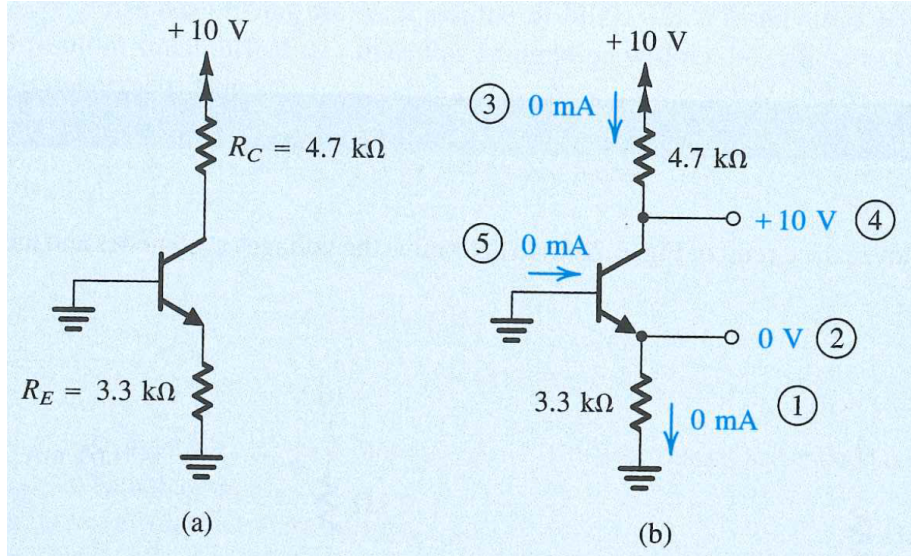


Figure 3: The circuit for Example 2, where (a) is the circuit, and (b) is the analysis steps (Courtesy of Sedra and Smith).

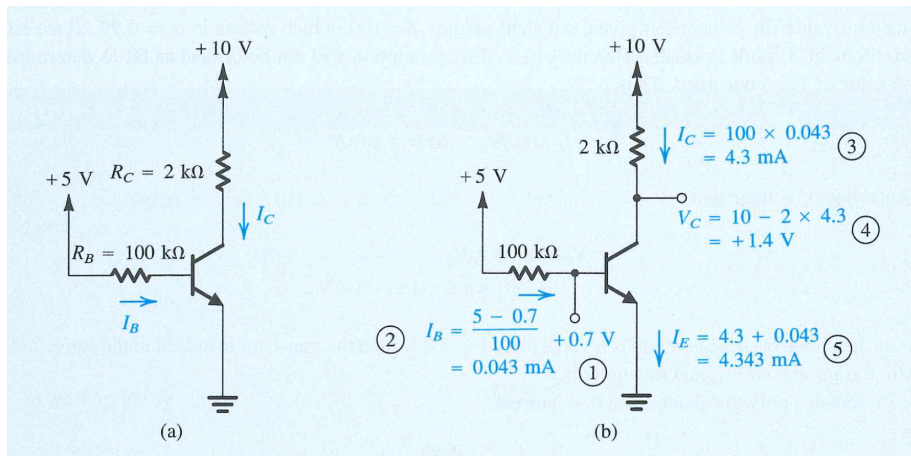


Figure 4: The circuit for Example 3, where (a) is the circuit, and (b) is the analysis steps (Courtesy of Sedra and Smith).

The collector voltage is then

$$V_C = 10 - I_C R_C = 10 - 4.3 \times 2 = +1.4 \text{ V} \quad (1.8)$$

Here,  $V_B$  is

$$V_B = V_{BE} \approx +0.7 \text{ V} \quad (1.9)$$

Then CBJ is reverse biased by  $+1.4 - 0.7 = 0.7 \text{ V}$  and the transistor is indeed in active mode. Hence, the emitter current is

$$I_E = (\beta + 1)I_B = 101 \times 0.043 \approx 4.3 \text{ mA} \quad (1.10)$$

Notice that if  $\beta$  higher, then  $I_C$  is larger, leading to a larger voltage drop across  $R_C$ . This will cause  $V_C$  to drop lower, reaching into the saturation regime of the transistor. Hence, this is a *bad* design.

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**Example 4.**<sup>4</sup>

We refer to Figure 5(a) to determine the node voltages and branch currents, with  $\beta = 100$ .

**Solution**

First, one finds the Thevenin equivalent source that is driving the base. The Thevenin voltage can be found by open-circuiting the output port, as the  $V_{\text{Thevenin}} = V_{oc}$ , the open-circuit voltage. Moreover, the two circuits should have the same short-circuit current. This process is shown next in the box.

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<sup>4</sup>Example 6.10 of textbook.

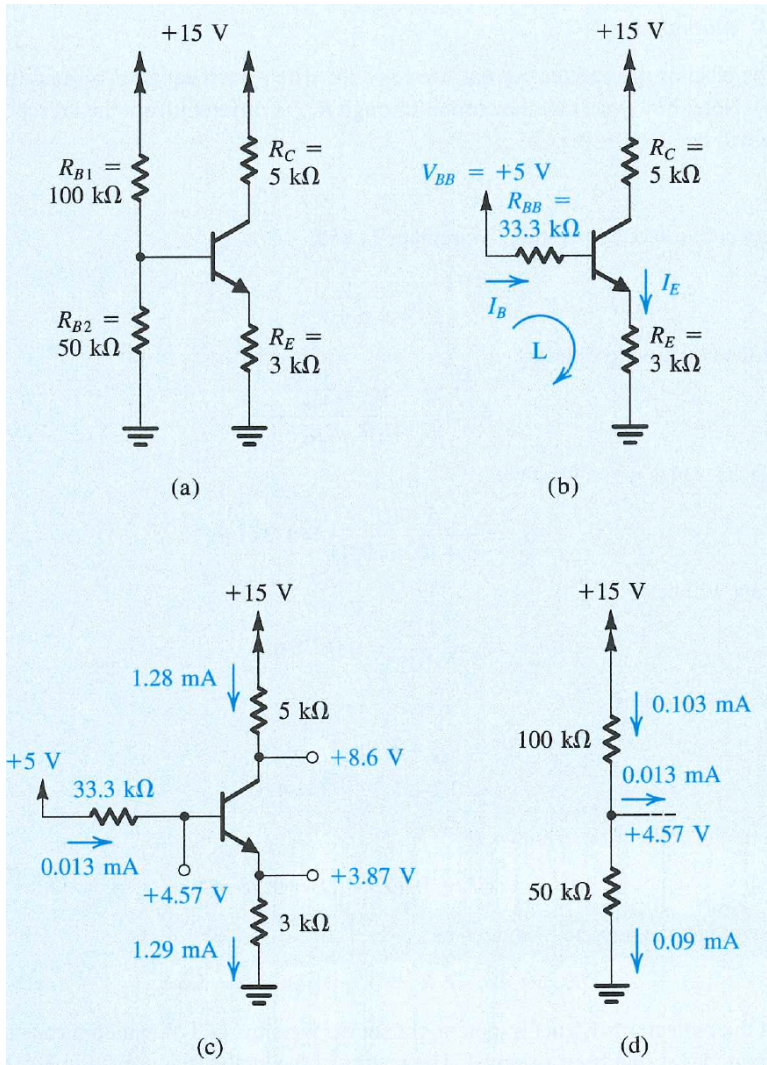
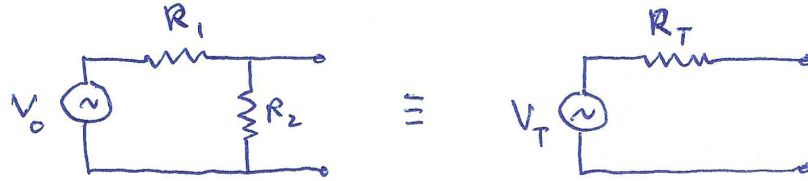


Figure 5: The circuit for Example 4, where (a) is the circuit, and (b) shows the Thevenin equivalent for the base current, (c) is the circuit to be analyzed, (d) shows the currents in the original circuit after retrieval (Courtesy of Sedra and Smith).

### Finding the Thevenin Equivalent Circuit



To find  $V_T$ , the Thevenin equivalent circuit should have the same open-circuit voltage  $V_{OC}$  as the original circuit. So one finds that

$$V_{OC} = V_T = \frac{R_2}{R_1 + R_2} V_0 \quad (1.11)$$

The two circuits should have the same short circuit current  $I_{SC}$ , and

$$I_{SC} = \frac{V_0}{R_1} = \frac{V_T}{R_T} = \frac{V_0}{R_T} \frac{R_2}{R_1 + R_2} \quad (1.12)$$

Solving for  $R_T$  from above gives

$$R_T = \frac{R_1 R_2}{R_1 + R_2} = R_1 || R_2 \quad (1.13)$$

The Thevenin equivalent resistance can also be found by the test-current method, where in the limit when the voltage sources are turned off, the source impedance of the two circuits should look the same.

Using these methods, then the Thevenin equivalent voltage is

$$V_{BB} = +15 \frac{R_{B2}}{R_{B1} + R_{B2}} = 15 \frac{50}{100 + 50} = +5 \text{ V} \quad (1.14)$$

The Thevenin equivalent impedance is

$$R_{BB} = R_{B1} || R_{B2} = 100 || 50 = 33.3 \text{ k}\Omega \quad (1.15)$$

Writing KVL or the loop equation around loop L, then

$$V_{BB} = I_B R_{BB} + V_{BE} + I_E R_E \quad (1.16)$$

Assuming

$$I_B = \frac{I_E}{\beta + 1} \quad (1.17)$$

Then substituting (1.16) into (1.15), solving for  $I_E$  gives

$$I_E = \frac{V_{BB} - V_{BE}}{R_E + R_{BB}/(\beta + 1)} = \frac{5 - 0.7}{3 + 33.3/101} = 1.29 \text{ mA} \quad (1.18)$$



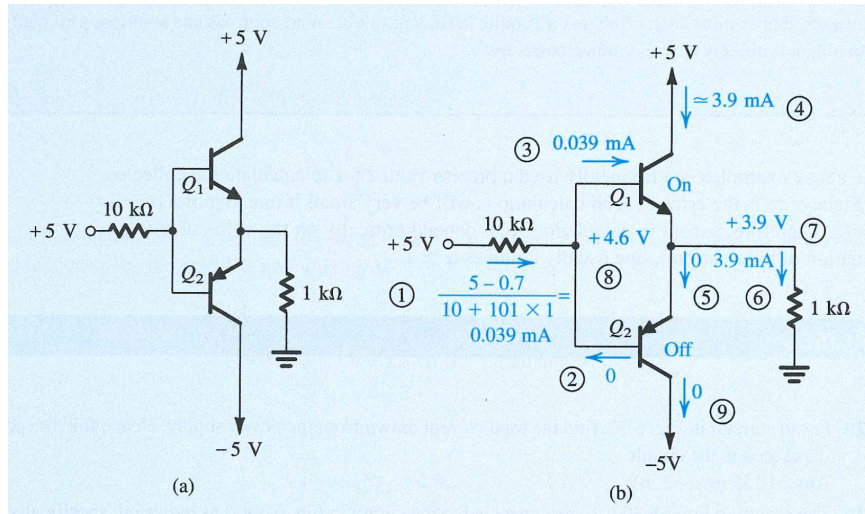


Figure 6: The circuit for Example 5, where (a) is the circuit, and (b) shows the steps in the analysis (Courtesy of Sedra and Smith).

The base current is then

$$I_B = \frac{1.29}{101} = 0.0128 \text{ mA} \quad (1.19)$$

And the base voltage is

$$V_B = V_{BE} + I_E R_E = 0.7 + 1.29 \times 3 = 4.57 \text{ V} \quad (1.20)$$

The collector current is

$$I_C = \alpha I_E = 0.99 \times 1.29 = 1.28 \text{ mA} \quad (1.21)$$

And the collector voltage is

$$V_C = +15 - I_C R_C = 15 - 1.28 \times 5 = 8.6 \text{ V} \quad (1.22)$$

Since  $V_C$  is higher than  $V_B$ , CBJ is reverse biased and the transistor is in active mode.

**Example 5.**<sup>5</sup>

The voltages and currents in Figure 6(a) can be found, assuming that  $\beta = 100$ .

<sup>5</sup>Example 6.12 of textbook.

First, note that both transistors cannot be simultaneously turned on or in the active mode because their bases are at the same voltage, so are their emitters. So when one is on, the other one has to be off.

Assume that  $Q_2$  is on, then the emitter current has to come via the  $1\text{ k}\Omega$  resistor by drawing current from the ground. This will make the emitter and base of  $Q_2$  be at negative potential, implying that a current will flow into the base. This is not possible for an *npn* transistor.

Next, assume that  $Q_1$  is on instead. When the base current flows into  $Q_1$  via the  $10\text{ k}\Omega$  resistor, the base voltage will be lower than  $5\text{ V}$ , and the CBJ of  $Q_1$  is reverse biased. Hence, it is in active mode.

Next, the node voltages and branch currents can be derived. First, one writes KVL around the loop formed by (1), (3), and (7) of the Figure 6(b). One gets that (using the notation of the previous example)

$$V_{BB} = I_B R_{BB} + V_{BE} + I_E R_E \quad (1.23)$$

Using

$$I_E = (\beta + 1)I_B \quad (1.24)$$

Substituting the above into the previous equation, and solving for  $I_B$ , one gets

$$I_B = \frac{V_{BB} - V_{BE}}{R_{BB} + (\beta + 1)R_E} = \frac{5 - 0.7}{10 + 101 \times 1} = 0.039\text{ mA} \quad (1.25)$$

Then the collector current

$$I_C = \beta I_B = 100 \times 0.039 = 3.9\text{ mA} \quad (1.26)$$

With the above, one can find the emitter voltage

$$V_E = I_E R_E = 3.9 \times 1 = 3.9\text{ V} \quad (1.27)$$

With the emitter voltage, one can find the base voltage

$$V_B = V_{BE} + I_E R_E = V_{BE} + V_E = 0.7 + 3.9 = 4.6\text{ V} \quad (1.28)$$