ECE 255

3 October 2017

In this lecture, we will study examples from Section 5.3 of Sedra and Smith.

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1 MOSFET Circuits at DC with Examples

Example 5.3

Design the circuit of Fig. 5.21: that is, determine the values of R_D and R_S so that the transistor operates at $I_D = 0.4$ mA and $V_D = +0.5$ V. The NMOS transistor has $V_t = 0.7$ V, $\mu_n C_{ox} = 100\ \mu\text{A/V}^2$, $L = 1\ \mu$m, and $W = 32\ \mu$m. Neglect the channel-length modulation effect (i.e., assume that $\lambda = 0$).

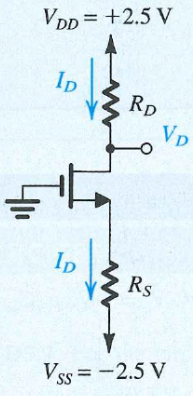

Figure 5.21 Circuit for Example 5.3.

Solution

To establish a dc voltage of +0.5 V at the drain, we must select R_D as follows:

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{2.5 - 0.5}{0.4} = 5\ \text{k}\Omega$$

To determine the value required for R_S, we need to know the voltage at the source, which can be easily found if we know V_{GS}. This in turn can be determined from V_{OV}. Toward that end, we note that since $V_D = 0.5$ V is greater than V_G, the NMOS transistor is operating in the saturation region, and we can use the saturation-region expression of i_D to determine the required value of V_{OV},

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}V_{OV}^2$$

Then substituting $I_D = 0.4$ mA $= 400\ \mu$A, $\mu_n C_{ox} = 100\ \mu\text{A/V}^2$, and $W/L = 32/1$ gives

$$400 = \frac{1}{2} \times 100 \times \frac{32}{1} V_{OV}^2$$

Example 5.3 *continued*

which results in

$$V_{OV} = 0.5 \text{ V}$$

Thus,

$$V_{GS} = V_t + V_{OV} = 0.7 + 0.5 = 1.2 \text{ V}$$

Referring to Fig. 5.21, we note that the gate is at ground potential. Thus, the source must be at –1.2 V, a the required value of R_S can be determined from

$$R_S = \frac{V_S - V_{SS}}{I_D} = \frac{-1.2 - (-2.5)}{0.4} = 3.25 \text{ k}\Omega$$

Example 5.4

Figure 5.22 shows an NMOS transistor with its drain and gate terminals connected together. Find the i–v relationship of the resulting two-terminal device in terms of the MOSFET parameters $k_n = k_n'(W/L)$ and V_{tn}. Neglect channel-length modulation (i.e., $\lambda = 0$). Note that this two-terminal device is known as a **diode-connected transistor**.

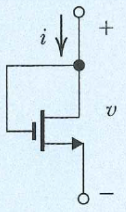

Figure 5.22

Solution

Since $v_D = v_G$ implies operation in the saturation mode,

$$i_D = \frac{1}{2} k_n' \left(\frac{W}{L} \right) (v_{GS} - V_{tn})^2$$

Now, $i = i_D$ and $v = v_{GS}$, thus

$$i = \frac{1}{2} k_n' \left(\frac{W}{L} \right) (v - V_{tn})^2$$

Replacing $k_n' \left(\frac{W}{L} \right)$ by k_n results in

$$i = \frac{1}{2} k_n (v - V_{tn})^2$$

Example 5.5

Design the circuit in Fig. 5.23 to establish a drain voltage of 0.1 V. What is the effective resistance between drain and source at this operating point? Let $V_{tn} = 1$ V and $k_n'(W/L) = 1$ mA/ V^2.

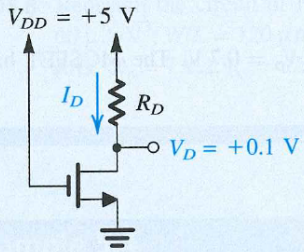

Figure 5.23 Circuit for Example 5.5.

Solution

Since the drain voltage is lower than the gate voltage by 4.9 V and $V_{tn} = 1$ V, the MOSFET is operating in the triode region. Thus the current I_D is given by

$$I_D = k_n' \frac{W}{L}\left[(V_{GS} - V_{tn})V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

$$I_D = 1 \times \left[(5-1) \times 0.1 - \frac{1}{2} \times 0.01\right]$$

$$= 0.395 \text{ mA}$$

The required value for R_D can be found as follows:

$$R_D = \frac{V_{DD} - V_D}{I_D}$$
$$= \frac{5 - 0.1}{0.395} = 12.4\ \text{k}\Omega$$

In a practical discrete-circuit design problem, one selects the closest standard value available for, say, 5% resistors—in this case, 12 kΩ; see Appendix J. Since the transistor is operating in the triode region with a small V_{DS}, the effective drain-to-source resistance can be determined as follows:

$$r_{DS} = \frac{V_{DS}}{I_D}$$
$$= \frac{0.1}{0.395} = 253\ \Omega$$

Alternatively, we can determine r_{DS} by using the formula

$$r_{DS} = \frac{1}{k_n V_{OV}}$$

to obtain

$$r_{DS} = \frac{1}{1 \times (5 - 1)} = 0.25\ \text{k}\Omega = 250\ \Omega$$

which is close to the value found above.

Example 5.6

Analyze the circuit shown in Fig. 5.24(a) to determine the voltages at all nodes and the currents through all branches. Let $V_{tn} = 1$ V and $k_n'(W/L) = 1$ mA/V^2. Neglect the channel-length modulation effect (i.e., assume $\lambda = 0$).

Example 5.6 *continued*

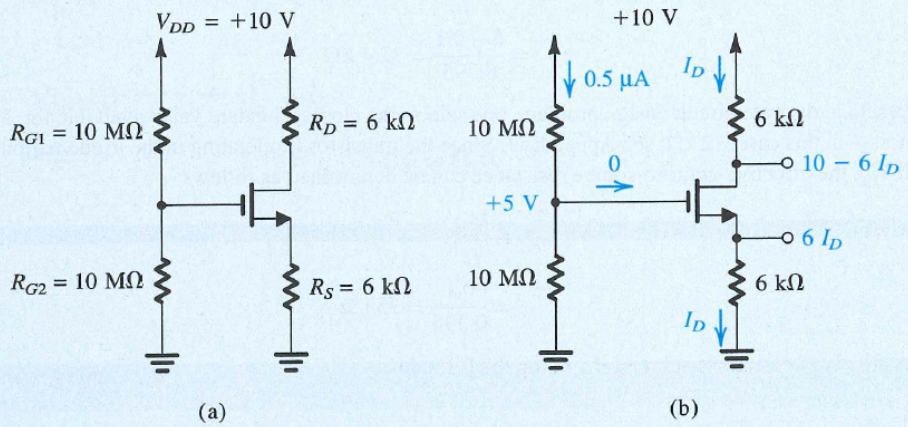

Figure 5.24 **(a)** Circuit for Example 5.6. **(b)** The circuit with some of the analysis details shown.

Solution

Since the gate current is zero, the voltage at the gate is simply determined by the voltage divider formed by the two 10-MΩ resistors,

$$V_G = V_{DD}\frac{R_{G2}}{R_{G2}+R_{G1}} = 10 \times \frac{10}{10+10} = +5 \text{ V}$$

With this positive voltage at the gate, the NMOS transistor will be turned on. We do not know, however, whether the transistor will be operating in the saturation region or in the triode region. We shall assume saturation-region operation, solve the problem, and then check the validity of our assumption. Obviously, if our assumption turns out not to be valid, we will have to solve the problem again for triode-region operation.

Refer to Fig. 5.24(b). Since the voltage at the gate is 5 V and the voltage at the source is I_D (mA) × 6 (kΩ) = $6I_D$ (V), we have

$$V_{GS} = 5 - 6I_D$$

Thus I_D is given by

$$I_D = \frac{1}{2}k_n'\frac{W}{L}(V_{GS} - V_{tn})^2$$

$$= \frac{1}{2} \times 1 \times (5 - 6I_D - 1)^2$$

which results in the following quadratic equation in I_D:

$$18I_D^2 - 25I_D + 8 = 0$$

This equation yields two values for I_D: 0.89 mA and 0.5 mA. The first value results in a source voltage of $6 \times 0.89 = 5.34$ V, which is greater than the gate voltage and does not make physical sense as it would imply that the NMOS transistor is cut off. Thus,

$$I_D = 0.5 \text{ mA}$$
$$V_S = 0.5 \times 6 = +3 \text{ V}$$
$$V_{GS} = 5 - 3 = 2 \text{ V}$$
$$V_D = 10 - 6 \times 0.5 = +7 \text{ V}$$

Since $V_D > V_G - V_m$, the transistor is operating in saturation, as initially assumed.

Example 5.7

Design the circuit of Fig. 5.25 so that the transistor operates in saturation with $I_D = 0.5$ mA and $V_D = +3$ V. Let the PMOS transistor have $V_{tp} = -1$ V and $k_p'(W/L) = 1$ mA/V^2. Assume $\lambda = 0$. What is the largest value that R_D can have while maintaining saturation-region operation?

Example 5.7 *continued*

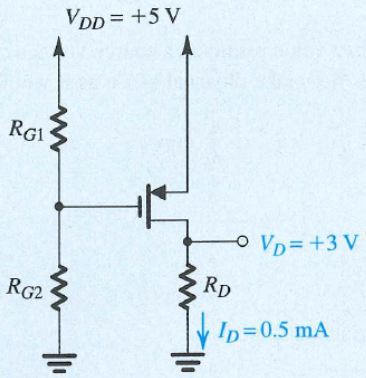

Figure 5.25 Circuit for Example 5.7.

Solution

Since the MOSFET is to be in saturation, we can write

$$I_D = \frac{1}{2} k_p' \frac{W}{L} |V_{ov}|^2$$

Substituting $I_D = 0.5$ mA and $k_p' W/L = 1$ mA/V^2, we obtain

$$|V_{ov}| = 1 \text{ V}$$

and

$$V_{SG} = |V_{tp}| + |V_{ov}| = 1 + 1 = 2 \text{ V}$$

Since the source is at +5 V, the gate voltage must be set to +3 V. This can be achieved by the appropriate selection of the values of R_{G1} and R_{G2}. A possible selection is $R_{G1} = 2$ MΩ and $R_{G2} = 3$ MΩ.

The value of R_D can be found from

$$R_D = \frac{V_D}{I_D} = \frac{3}{0.5} = 6 \text{ kΩ}$$

Saturation-mode operation will be maintained up to the point that V_D exceeds V_G by $|V_{tp}|$; that is, until

$$V_{D\max} = 3 + 1 = 4 \text{ V}$$

This value of drain voltage is obtained with R_D given by

$$R_D = \frac{4}{0.5} = 8 \text{ kΩ}$$

Example 5.8

The NMOS and PMOS transistors in the circuit of Fig. 5.26(a) are matched, with $k_n'(W_n/L_n) = k_p'(W_p/L_p) = 1$ mA/V^2 and $V_{tn} = -V_{tp} = 1$ V. Assuming $\lambda = 0$ for both devices, find the drain currents i_{DN} and i_{DP}, as well as the voltage v_O, for $v_I = 0$ V, +2.5 V, and −2.5 V.

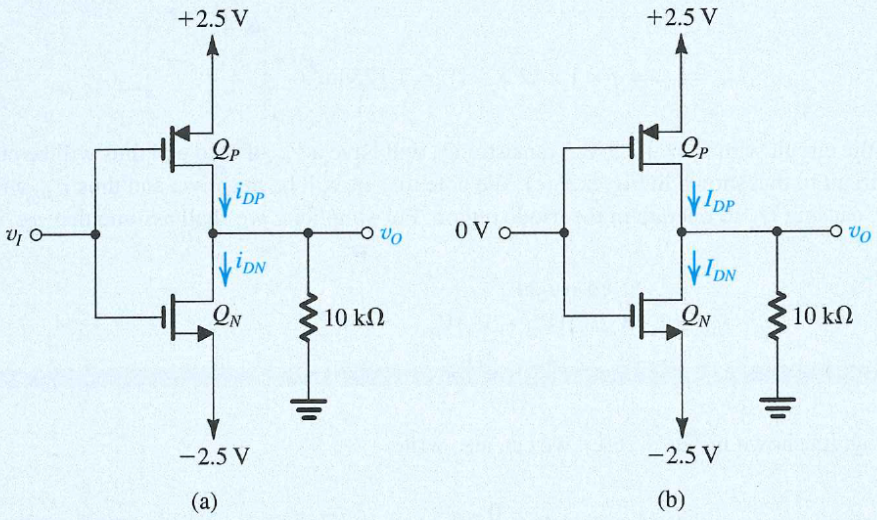

Figure 5.26 Circuits for Example 5.8.

Example 5.8 *continued*

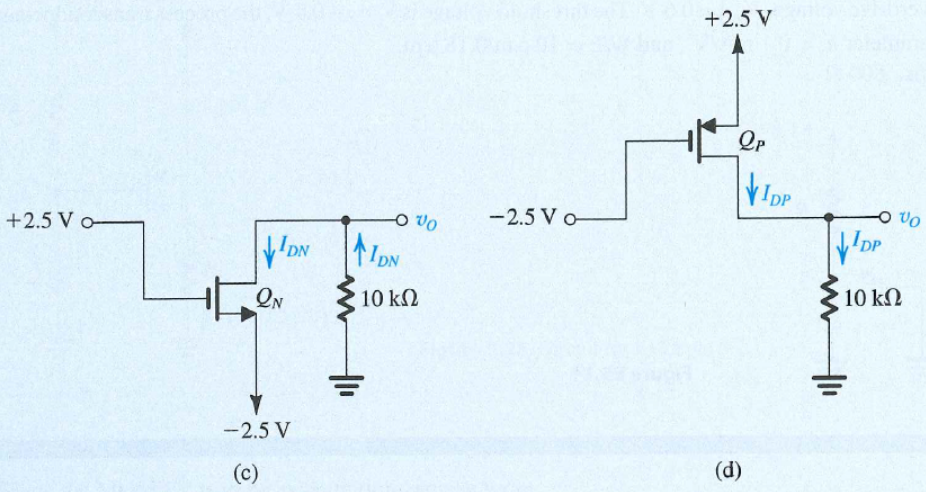

Figure 5.26 *continued*

Solution

Figure 5.26(b) shows the circuit for the case $v_I = 0$ V. We note that since Q_N and Q_P are perfectly matched and are operating at equal values of $|V_{GS}| = 2.5$ V, the circuit is symmetrical, which dictates that $v_O = 0$ V. Thus both Q_N and Q_P are operating with $|V_{DG}| = 0$ and, hence, in saturation. The drain currents can now be found from

$$I_{DP} = I_{DN} = \tfrac{1}{2} \times 1 \times (2.5 - 1)^2 = 1.125 \text{ mA}$$

Next, we consider the circuit with $v_I = +2.5$ V. Transistor Q_P will have a V_{SG} of zero and thus will be cut off, reducing the circuit to that shown in Fig. 5.26(c). We note that v_O will be negative, and thus v_{GD} will be greater than V_{tn}, causing Q_N to operate in the triode region. For simplicity we shall assume that v_{DS} is small and thus use

$$\begin{aligned} I_{DN} &\simeq k_n'(W_n/L_n)(V_{GS} - V_{tn})V_{DS} \\ &= 1[2.5 - (-2.5) - 1][v_O - (-2.5)] \end{aligned}$$

From the circuit diagram shown in Fig. 5.26(c), we can also write

$$I_{DN}(\text{mA}) = \frac{0 - v_O}{10(\text{k}\Omega)}$$

These two equations can be solved simultaneously to yield

$$I_{DN} = 0.244 \text{ mA} \qquad v_O = -2.44 \text{ V}$$

Note that $V_{DS} = -2.44 - (-2.5) = 0.06$ V, which is small as assumed.

Finally, the situation for the case $v_I = -2.5$ V [Fig. 5.26(d)] will be the exact complement of the case $v_I = +2.5$ V: Transistor Q_N will be off. Thus $I_{DN} = 0$, Q_P will be operating in the triode region with $I_{DP} = 0.244$ mA and $v_O = +2.44$ V.