Semiconductors@Purdue

FALL 2023

PURDUE UNIVERSITY

For more information on Semiconductors at Purdue, please visit our website at:
https://engineering.purdue.edu/semiconductors

or email Cristina Farmus at:
cfarmus@purdue.edu or semiconductors@purdue.edu

Cover photo:

From left: Purdue University President **Mung Chiang**, U.S. Secretary of Commerce **Gina Raimondo**, and U.S. Senator **Todd Young** participate in a fireside chat at the CHIPS for America: Execute for Success 2023 Policy and Strategy Summit hosted in Washington, D.C. on April 18th, 2023.

(Purdue University Photo/Purdue Marketing and Communications)

OCTOBER 2023

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Semiconductors@Purdue

Purdue University is uniquely positioned to offer a full range of options for partners interested in semiconductors and microelectronics: research and innovation, workforce and talent, and business growth. As a top 10 public university in the U.S. that moves fast and gets things done, Purdue pursues excellence at scale, with the largest engineering college (over 16,000 engineering students) ever ranked among the top 5 in the U.S and top 5 university in the world in receiving U.S. patents.

Purdue University is home to large scale, impactful, interdisciplinary research and learning in semiconductors. A strong, critical mass of researchers sets Purdue apart by spanning the full stack of semiconductors R&D from materials and devices, to circuits, systems, architecture, and advanced packaging integration. Purdue currently leads three and participates in two Semiconductor Research Corporation funded multi-university research programs. Strong connections to industry, such as DoD, Commerce/NIST, and NSF, support one of the nation's largest and best semiconductors research programs.

Purdue's reputation as an R&D trailblazer is matched by its leadership in workforce development. In May 2022, we launched the Semiconductor Degrees Program, a full suite of degrees and credentials options for semiconductors education, ranging from on-campus courses to a new set of degrees, competitive internships, innovative Learning While Working program, flexible online courses, and virtual lab. Purdue leads the Scalable Asymmetric Life Cycle Engagement (SCALE), a five-year, DoD sponsored national coalition of 19 universities aimed at addressing the urgent need to develop a highly skilled U.S. microelectronics workforce to bolster national security.

In summer 2022, Purdue announced a partnership with SkyWater Technologies to build a $1.8B fab on campus, and another partnership with MediaTek to build company's first semiconductor chip design center in the Midwest, to be housed on Purdue's campus. Together with IEDC and Navy Crane, Indiana is building a strong semiconductor ecosystem as the heart of the Silicon Heartland.

In May and June 2023, Purdue has announced four like-minded global partnerships in semiconductor workforce and innovation. On May 3rd, Purdue University and the State of Indiana announced an R&D partnership with imec during the SelectUSA Investment Summit,. The following week, Purdue signed an agreement to become the flagship academic partner and collaborator with the government of India, establishing Purdue as a key collaborator with the India Semiconductor Mission (ISM). At G7 on May 21st, in Hiroshima, Japan, Purdue signed another landmark international agreement, partnering with Micron, Tokyo Electron, and other educational institutions in the U.S. and Japan to establish the "UPWARDS Network" for workforce advancement and research and development in semiconductors. On June 19, Purdue and TSMC renewed the partnership in the Center for Secure Microelectronics Ecosystems.

As part of Purdue@DC, the full-day CHIPS for America: Execute for Success 2023 Policy and Strategy Summit, held at the Russell Senate Office Building on April 18th, 2023, convened hundreds of attendees representing over 175 entities from over 23 states, and focused on strategies to execute the vision outlined in CHIPS for America: Vision for Success. Featuring a fireside keynote with Secretary Gina Raimondo and Senator Todd Young, the Summit highlighted the implementation of federal investments and future policy actions and facilitated the creation of government, industry, and academic partnerships

“Semiconductor excellence at scale runs deep within the DNA of Purdue. From the invention of MOSFET by Mohamed Atalla, a proud Boilermaker engineer, to the creation of the Silicon Valley by Fred Terman who hailed from the Hoosier soil. Today, Purdue is America’s semiconductor university, where cutting-edge research, workforce development, and “lab-to-fab” collaboration with industry converge. With over 50 esteemed faculty in the nation’s top 4 engineering college, we have launched the first comprehensive Semiconductor Degrees Program, welcomed the Skywater fab to campus, formed an R&D partnership with imec, established Purdue as a key collaborator with India Semiconductor Mission, and signed the U.S.-Japan semiconductor agreement at the G7 summit. Together with the state of Indiana and Navy Crane, and leading with actions on national policies in Washington D.C., Purdue is at the heart of the Silicon Heartland.”

Mung Chiang

President

Roscoe H. George Distinguished Professor,
Elmore Family School of Electrical and Computer Engineering

Purdue University

Mark Lundstrom

Senior Advisor to the President and Chief Semiconductor Officer

Don and Carol Scifres Distinguished Professor,
Elmore Family School of Electrical and Computer Engineering

Purdue University

Purdue President's Semiconductor Taskforce

A new Purdue University taskforce devoted to semiconductors and microelectronics has reasserted the university's focus on helping the U.S. regain preeminence in the industry.

The President's Semiconductor Taskforce will coordinate and lead Purdue's efforts toward innovative research and development through the CHIPS for America and Science Act, approved last year in Washington, D.C. The taskforce will consist of faculty experts from several areas of Purdue microelectronics. Purdue expanding semiconductor research and development already runs the gamut of disciplines in the field, from materials and devices to circuits, systems, architecture, and advanced packaging integration. Strong connections in industry, defense, and the National Science Foundation further support Purdue's research.

Leading the new taskforce is Mark Lundstrom, who steps into a new role as Chief Semiconductor Officer for Purdue and Senior Advisor to President Mung Chiang. Lundstrom most recently served as Interim Dean for the College of Engineering.

Mark Lundstrom
Taskforce Leader

Senior Advisor to the President and Chief Semiconductor Officer; Don and Carol Scifres Distinguished Professor, Elmore Family School of Electrical and Computer Engineering

Ganesh Subbarayan
Fellow

Co-director, SRC Center for Heterogeneous Integration Research in Packaging; James G. Dwyer Professor of Mechanical Engineering, School of Mechanical Engineering

Carol Handwerker
Senior Fellow

Reinhardt Schuhmann, Jr. Distinguished Professor in the School of Materials Engineering

Zhihong Chen

Mary Jo and Robert L. Kirk Director of Birck Nanotechnology Center; Professor, Elmore Family School of Electrical and Computer Engineering

Joerg Appenzeller
Senior Fellow

Scientific Director of Nanoelectronics in the Birck Nanotechnology Center; Barry M. and Patricia L. Epstein Professor, Elmore Family School of Electrical and Computer Engineering

Peter Bermel

Director of SCALE; Associate Director of Graduate Admissions; Elmore Professor, Elmore Family School of Electrical and Computer Engineering

Vijay Raghunathan
Fellow

Associate Head of ECE; Director of Semiconductor Education; Professor, Elmore Family School of Electrical and Computer Engineering

Cristina Farmus

Vice President for Special Projects

Silicon Crossroads Hub:
Purdue's Semiconductor Innovation Ecosystem Grows with CHIPS-Funded, Indiana-Led Semiconductor Hub

PURDUE UNIVERSITY

Submitted through the Applied Research Institute, the Indiana-led proposal "Silicon Crossroads" was announced September 20 by the Department of Defense as one of eight Microelectronics Commons Hubs selected out of over 80 proposals across the U.S. The Naval Surface Warfare Center, Crane Division (NSWC Crane), in Indiana will manage the program.

The hubs are the first major program funded through the CHIPS and Science Act 2022, co-sponsored by U.S. Sen. Todd Young of Indiana. The total five-year budget is around $2 billion; FY23 is year 1 and has a budget of $238 million. The Indiana-led consortium, with participation from Illinois and Michigan, received $33 million as part of the year 1 budget and is the largest hub in the Midwest.

"As we collectively work to grow the nation's microelectronics base, Indiana will play a key role in the development of these critical national security technologies and capabilities," Young said. "More broadly, this announcement shows how the CHIPS and Science Act will connect more of America, including the industrial Midwest, to the innovation economy."

Indiana leads the Silicon Crossroads Hub, and as its leading university Purdue will collaborate with many members of the consortium in the coming years. Purdue is a national leader in microelectronics materials, devices, chip design, tool development, manufacturing, packaging and sustainability, spanning the semiconductor ecosystem in software and hardware with long-standing faculty excellence.

> *"Located in America's heartland, Silicon Crossroads builds on the Midwest's strengths in research and development as well as workforce training at all levels to build a domestic semiconductor industry—a national security imperative to keep our nation ahead of our adversaries."*
>
> **Eric Holcomb,** Indiana Governor

U.S. Secretary of State Antony J. Blinken and Secretary of Commerce Gina Raimondo Visit Purdue University

U.S. Secretary of State Antony J. Blinken and Secretary of Commerce Gina Raimondo visited Purdue University on September 13, 2022 to tour university research facilities and meet students as they embark on their mission to bolster the U.S. semiconductor industry.

Senator Todd Young (R-Ind.) and Indiana Governor Eric J. Holcomb joined Blinken and Raimondo on a tour of Purdue's Birck Nanotechnology Center, highlighting the leading-edge research and workforce development efforts at Purdue that can help the United States restore domestic semiconductor manufacturing and competitiveness abroad. A fireside chat followed.

From left: *Indiana Governor Eric J. Holcomb, U.S. Secretary of State Antony Blinken, Purdue President (2013-2022) Mitch Daniels, U.S. Secretary of Commerce Gina Raimondo, and U.S. Senator Todd Young participate in a fireside chat following a tour of Purdue's microelectronics facilities.*

(Photo: Charles Jischke, Purdue University)

> *"This is, I think, the most exciting human fab that I have ever seen."*
>
> **Antony Blinken,** U.S. Secretary of State

> *"I was blown away by what I saw when I visited Purdue, in so far as, in my assessment, it is exactly what the United States needs to be doing."*
>
> **Gina Raimondo,** U.S. Secretary of Commerce

Speaking to the crowd at Birck, Raimondo announced that the Commerce Department's National Institute of Standards and Technology signed a cooperative research and development agreement to develop and produce chips for nanotech and semiconductor devices. SkyWater Technology will manufacture the chips at an existing semiconductor foundry in Minnesota. This summer, Purdue announced partnerships with SkyWater to build a $1.8 billion fabrication facility in West Lafayette.

"Purdue's cutting-edge research and workforce development programs are at the forefront of helping us shape the future of innovation in America's semiconductor manufacturing industry. I'm excited to learn about the workforce pipelines Purdue is creating, including opportunities at all levels of the industry," Raimondo said. "I'm excited to have met the students who are future leaders of America's semiconductor industry. The graduates from these programs—from Ph.D.s to associate degree holders—will be at the forefront of innovation as we revitalize American manufacturing."

From left:

U.S. Sen. Todd Young, Indiana Governor Eric J. Holcomb, U.S. Secretary of Commerce Gina Raimondo, and U.S. Secretary of State Antony Blinken during a tour of Purdue's microelectronics facilities.

(Photo: Charles Jischke, Purdue University)

U.S. Secretary of Commerce Gina Raimondo and Purdue President (as of January 1, 2023) Mung Chiang at the Industrial Round Table career fair.

CHIPS for America:
Execute for Success 2023 Policy Strategy Summit

The CHIPS for America: Execute for Success 2023 Policy and Strategy Summit, held on April 18, 2023 in Washington, D.C., was co-hosted by Purdue University and U.S. Senator Todd Young. The Krach Center for Tech Diplomacy at Purdue, SEMI, and the Semiconductor Industry Association (SIA) were partners in organizing this summit. The event was attended in person by over 280 participants from 175 distinct entities (government, industry, academia, think tanks, law firms, and professional associations) from over 23 states and Washington, D.C.

The theme of this summit was "Executing for Success" with a focus on executing the vision for the CHIPS Act. Three panel discussions offered perspectives from government, industry, and academia, thoughts on the challenges ahead, and ways to sustain the effort over the long term. A fireside chat with The Honorable Gina Raimondo, Secretary of Commerce, and Senator Todd Young was moderated by Purdue President, Mung Chiang, followed by remarks from Barbara Snyder, President of the Association of American Universities.

CHIPS for America Summit: *University Panel*

From left: **Max Mirgoli,** *Executive Vice President of Worldwide Strategic Partnerships, imec*
Dr. Todd Younkin, *President and CEO, Semiconductor Research Corporation*
Dr. Mark Lundstrom, *Don and Carol Scifres Distinguished Professor of Electrical and Computer Engineering, Chief Semiconductor Officer, Purdue University*
Dr. Tsu-Jae King Liu, *Dean and Roy W. Carlson Professor, College of Engineering, University of California, Berkeley*
Dr. Matt Kay, *T&AM Program Manager, Office of Deputy CTO for Critical Technologies, Department of Defense*

Other speakers at the summit included Ramin Toloui, Assistant Secretary of State for the Bureau of Economic and Business Affairs at the U.S. Department of State; Dr. Dev Shenoy, Principal Director of Microelectronics with the U.S. Department of Defense; Dr. Eric Lin, Interim Director, CHIPS Research and Development, U.S. Department of Commerce; and Dr. Erwin Gianchandani, Assistant Director of the Technology, Innovation, and Partnerships at the National Science Foundation, as well as leaders from Applied Materials, Everspin Technologies, Information Technology and Innovation Foundation, Intel, Micron, SEMI, the Semiconductor Industry Association, Semiconductor Research Corporation, and SkyWater. They shared their perspectives on the challenges ahead, ways to measure progress and how to sustain the effort over the long term. Barbara Snyder, President of the Association of American Universities, made concluding remarks about the multiple roles a leading research university like Purdue plays in the success of CHIPS Act.

Some key points from the panel discussions were:

- To ensure sustained U.S. technology leadership—the focus must be on enhancing interagency and public-private collaboration, supporting comprehensive workforce development, and developing viable manufacturing capacity and supply chains.
- The CHIPS Act provides unprecedented support to address these priorities, but will require a sustained effort from government and industry, universities, community colleges, and K-12 educators, as well as key international partners.

Chips for America Summit: *Industry Perspectives Panel*

From left: **Dr. Rob Atkinson,** *President, Information Technology and Innovation Foundation*
Ajit Manocha, *President and Chief Executive Officer, SEMI*
Manish Bhatia, *Executive Vice President, Global Operations, Micron*
Keyvan Esfarjani, *Chief Global Operations Officer, Intel*
Satheesh Kuppurao, *Group VP for Business Development and Growth, Applied Materials*

(Photo: Purdue University Marketing and Communications)

- To boost competitiveness, incentives like the CHIPS program are key, but many countries around the world have announced and started to implement similar programs. The U.S. microelectronics industry must take a long-term view and recognize that it faces intense competition for global semiconductor Foreign Direct Investment especially as other nations dramatically ramp up their subsidies.
- The need for new talent and upskilling of the current workforce is critical. A waterfall model was proposed: identify a few major university workforce development hubs around the nation, charge them to scale-up programs to have impact within three to five years, then expand the impact to more universities, and establish a national network to coordinate activities, assess and share best practices, and share content.

Purdue announced the Sustainability Capability Semiconductors Index (SCSI), which will track a composite of 5 scores for water, power, chemicals, emissions, and construction. This update of industry state-of-the-art progress will be presented quarterly.

What Purdue Offers

#4
BEST ENGINEERING GRADUATE SCHOOL IN THE U.S.
U.S. News & World Report, 2022

#4
IN THE U.S. FOR PATENTS
U.S. Patent and Trademark Office, 2022

- Advanced Research & Development facilities with more than 400 research labs on the West Lafayette campus, including the Scifres Nanotechnology Laboratory, the second largest clean room in academia.
- Advanced Packaging and Heterogeneous Integration, novel approaches to information, emerging memory technologies, reliability, and sustainability of electronics.
- Exceptional faculty with 22 members of the National Academy of Engineering.
- Innovative faculty and staff with 18 National Academy of Inventors Fellows at Purdue, of which 14 are in the College of Engineering.
- A pipeline of globally competitive talent needed to innovate and thrive with over 11,000 engineering undergraduate and 4,000 graduate students.
- A business-minded university with an interwoven business and social ecosystem, backed by Purdue Research Foundation track record of meeting industry partners' needs with space, logistics, and community connections.

NOTABLE PURDUE RANKINGS

RANKING	SOURCE	NATION
Engineering Graduate Program	U.S. News & World Report	#4
Engineering Undergraduate Program	U.S. News & World Report	#9
Online Graduate Engineering Program	U.S. News & World Report	#2
Most Innovative School	U.S. News & World Report	#7
Top Public University	The Wall Street Journal / Times Higher Education	#10
Best Value University	The Wall Street Journal / Times Higher Education	#7
Best University for Engagement	The Wall Street Journal / Times Higher Education	#4
University with Most Utility Patents in the World	U.S. Patent and Trademark Office	#5
Graduating the Most STEM Majors	Forbes	#5
Number of Alumni Working at Top Fortune 500 Companies	Forbes	#19
Best Colleges for Veterans	College Consensus	#8
Safest College Town	SafeWise.com	#15
Best Online Learning School	Newsweek	#3

Indiana and Purdue Semiconductor History

Indiana and Purdue have a long record of impacting semiconductor history, as exemplified by three outstanding individuals: Karl Lark-Horovitz, who pioneered work in solid-state physics that played a role in the invention of the transistor, Frederick E. Terman, the Father of Silicon Valley, and Mohamed M. Atalla, who co-invented the MOSFET metal–oxide–semiconductor field-effect transistor, or MOS transistor.

Karl Lark-Horovitz was a Purdue professor and Head of the Department of Physics. Through his work and that of many others at Purdue, the field of semiconductor research was expanded greatly. In the 1940s he turned his attention to solid state physics, a then new area of theory and research. He was the first to recognize the benefits of using germanium as the material with which to work. Observations of the changing resistance of a semiconductor under an applied voltage helped point the way to the discovery of the transistor. Of equal importance was the research done on materials preparation, as well as the investigation of fundamental properties of semiconductors. The first transistor at Bell Laboratories was actually demonstrated in 1947 using a germanium crystal grown in the Purdue lab and supplied to Bell Laboratories.

Frederick E. Terman was born and spent his childhood in Indiana. As a professor at Stanford, in 1951 he spearheaded the creation of Stanford Industrial Park whereby the University leased portions of its land to high-tech firms. Companies such as Varian Associates, Hewlett-Packard, Eastman Kodak, General Electric, and Lockheed Corporation moved into Stanford Industrial Park and made the mid-Peninsula area into a hotbed of innovation which eventually became known as Silicon Valley.

Mohamed M. Atalla was an Egyptian-American engineer, physical chemist, cryptographer, inventor, and entrepreneur. Born in Egypt, he was educated at Cairo University in Egypt and then Purdue University, before joining Bell Laboratories. He was a semiconductor pioneer who made important contributions to modern electronics. He is best known for co-inventing the MOSFET (metal–oxide–semiconductor field-effect transistor, or MOS transistor) in 1959, with his colleague Dawon Kahng, which along with Atalla's earlier surface passivation and thermal oxidation processes, revolutionized the electronics industry.

SkyWater Technology Plans to Open Fab in West Lafayette

Left to right:

Mitch Daniels,
Purdue University President (2013-2022)

Thomas Sonderman,
SkyWater President and CEO

Ian Steff, *Former Assistant Secretary of Commerce and President and CEO of mySilicon Compass*

Mung Chiang, *Purdue University President (as of January 1, 2023)*

Gary J. Obermiller, *Chairman of the Board, SkyWater Technology*

On July 20, 2022 SkyWater Technology announced plans to open a $1.8 billion state-of-the-art semiconductor manufacturing facility in the Discovery Park District at Purdue, marking a huge step forward for the American semiconductor industry, Purdue's thriving innovation district, and the university's continued emergence as one of the principal drivers of the Indiana economy.

SkyWater, which expects to create 750 new direct jobs within five years after it opens, joins the likes of Saab, Rolls-Royce, major facilities and partnerships in hypersonics, Schweitzer Engineering Laboratories, Wabash, MediaTek, and others who have chosen Discovery Park District as the place to set-up or expand business, as one of the most attractive and innovative environments in the Midwest.

American jobs created will focus on research and design engineering, technology development, operations engineering, maintenance and technical support, and technicians. The new SkyWater facility will accelerate domestic semiconductor capabilities, ensure IP security, and support a more resilient and comprehensive supply chain, providing powerful competitive advantages for its U.S. government and commercial customers. By co-locating the fab at Purdue, SkyWater and its customers will benefit from close collaboration with the university and its pipeline of talent.

SkyWater is a U.S. investor-owned semiconductor manufacturer and a DMEA-accredited Category 1A Trusted Foundry. SkyWater's Technology as a ServiceSM model streamlines the path to production for customers with development services, volume production, and heterogeneous integration solutions in its world-class U.S. facilities. This pioneering model enables innovators to co-create the next wave of technology with diverse categories including mixed-signal CMOS, ROICs, rad-hard ICs, power management, MEMS, superconducting ICs, photonics, carbon nanotubes, and interposers. SkyWater serves growing markets including aerospace and defense, automotive, biomedical, cloud and computing, consumer, industrial, and IoT. For more information, visit: www.skywatertechnology.com.

MediaTek to Open New IC Design Center at Purdue University

On June 28, 2022, Purdue University announced a partnership with MediaTek Inc., a leading global fabless chipmaker, to open the company's first semiconductor chip design center in the Midwest, to be housed on Purdue's campus. MediaTek and Purdue also will partner on new chip design engineering degree programs, research on artificial intelligence, and communications chip design. This collaboration is still in the works.

"This means students and faculty at Purdue will have the opportunity to interact with world class chip design talent right across the street," said Dr. Mung Chiang, President (as of January 1, 2023) of Purdue University. The Purdue team worked with the Indiana Economic Development Corporation to fully leverage Purdue's role as one of the top STEM universities to attract this new semiconductor investment.

"We believe strongly that being in Indiana means we'll have access to some of the best engineering talent in the world," said Dr. Kou-Hung Lawrence Loh, Corporate Senior Vice President of MediaTek Inc. and President of MediaTek USA, Inc. "Not just at Purdue, but West Lafayette is only four hours away from nearly a dozen of the top engineering schools in the country. In the post pandemic world, top candidates tell us they want to be closer to home, near family and they want to have a real house and great schools. Indiana offers all that and more."

The Purdue partnership represents a new U.S. growth model for MediaTek USA—outside the traditional centers of gravity for chip design.

Among those who participated in the announcement were Kou-Hung Lawrence Loh, Corporate Senior Vice President of MediaTek Inc. and President of MediaTek USA (second from left), Eric J. Holcomb, Governor of the State of Indiana (third from left), Brad Chambers, Indiana Secretary of Commerce (fourth from left), and Mung Chiang, President (as of January 1, 2023) of Purdue University (far right).

Industry Partners

Design: AMD, Apple, Cadence, Graphcore, IBM, Intel, MediaTek, Nantero, NVIDIA, Reliable MicroSystems, Samsung, Silvaco, Synopsys, Qualcomm

Tooling: Applied Materials, ASM, ASML, eFabless, KLA, Lam, Tokyo Electron

Manufacturing: Draper, Everspin, GlobalFoundries, IBM, Infineon, Intel, Marvell, NHanced, Samsung, Seagate, SK hynix, SkyWater, Svagos, TSMC, Western Digital

Materials: Air Liquide, Air Products, Corning, Dow, Eastman, Hemlock Semiconductors, MacDermid Alpha, Molex

Customers: Amazon Web Services, Analog Devices, Apple, BAE Systems, Boeing, BorgWarner, Caterpillar, Cisco, Collins Aerospace, Cummins, Daimler, Deere & Co., Fiat Chrysler, Ford, General Dynamics, General Electric, General Motors, Google, Hewlett Packard Enterprise, Hitachi, Honeywell, Juniper Networks, L3Harris, LG Electronics, Lockheed Martin, Medtronic, Microsoft, Nokia, Northrop Grumman, One Network, Raytheon, Robert Bosch, Rolls-Royce, Saab, Siemens, SpaceX, Subaru, Tesla, Texas Instruments, Toyota, United Technologies, ZF Friedrichshafen AG (TRW)

How Industry Can Contribute to Developing the Semiconductors Workforce

Purdue University has already made significant investments in developing the next generation workforce for the semiconductors industry. We are looking forward to working with industry partners to take the initiative to the next level and encourage partners to contribute in many ways. Below are some examples of engagement—pick one option or all—Purdue is ready to work with you to create a customized program that fits your needs and maximizes student success. Contact Cristina Farmus cfarmus@purdue.edu to get more details.

In Kind

1. Commit to summer 2024 internships.
2. Commit to interviewing students with a GPA 3.2 and above.
3. Identify Purdue as a strategic partner university.
4. Participate in the Semiconductor Education Steering Committee to refine curriculum and training offerings, including for technicians.
5. Provide speakers for undergraduate lecture series, high school outreach and college recruiting events.
6. Host faculty at your sites to better understand current industry needs.

Financial Support

1. Fund scholarships for students pursuing semiconductors degrees.
2. Support the Summer Training, Awareness, Readiness for Semiconductors (STARS) 2024 UG semiconductor program ($15K per student covers stipend, lodging, and program operating fees).
3. Sponsor VIP projects (e.g. tapeout fees).
4. Donate equipment.
5. Consider establishing a named professorship.
6. Support new program/course development (e.g. MicroMasters).
7. Offer unrestricted support for semiconductor WFD.

Establish Permanent Presence at Purdue

Start as small or as large as you'd like, office space available immediately.

Purdue Semiconductor Degree Leadership Board

Purdue has launched the Semiconductor Degree Leadership Board, an elite group of executives from leading semiconductor companies that will provide visionary input into the Purdue Semiconductor Degrees Program and other workforce development programs designed and implemented by Purdue.

We are proud to list the following members:

NAME	TITLE	COMPANY
Gregg Bartlett	Chief Technology Officer	GlobalFoundries
William Chappell	Chief Technology Officer Strategic Missions and Technology (SMT) Division	Microsoft
Juan de Bedout	Senior Vice President of Aerospace Technology	Raytheon Technologies
Debra Delise	Vice President of Security Products and Technology	Analog Devices
Brian Dunlap	Vice President 300mm Fab Operations	Texas Instruments
Keyvan Esfarjani	Executive Vice President, Chief Global Operations Officer and General Manager of Manufacturing, Supply Chain and Operations	Intel
Sudhir Gopalswamy	Senior Vice President and General Manager of the Advanced Solutions Group (ASG)	onsemi
Deirdre Hanford	Chief Security Officer	Synopsys
Brian Harrison	President	TSMC Arizona
Raghib Hussain	President of Products and Technologies	Marvell Technologies
Mohammed Kassem	CoFounder and Chief Technology Officer	Efabless
Mukesh Khare	General Manager of IBM and Vice President of Hybrid Cloud	IBM
Steve Kosier	Executive Vice President, Chief Technology Officer	SkyWater
Matt Massengill	Chairman of the Board and Former Chief Executive Officer	Western Digital
Om Nalamasu	Senior Vice President and Chief Technology Officer	Applied Materials
John Neuffer	President and Chief Executive Officer	Semiconductor Industry Association
Alexander Ocsilowski	President	Tokyo Electron Technology Center America
Jonghoon Oh	Executive Vice President and General Manager for U.S. Research and Development	SK hynix
Mark Papermaster	Executive Vice President and Chief Technology Officer of Technology and Engineering	AMD
Adam Peters	Chief Executive Officer, North America	Air Liquide Group
Nirmal Ramaswamy	Vice President of Advanced DRAM and Emerging Memory	Micron Technology
Tom Rueckes	Chief Technology Officer and CoFounder	Nantero
Charlie Schadewitz	Vice President, North American Field Operations at Cadence Design Systems	Cadence
Stéphane Sireau	Vice-President, High-Tech Industry	Dassault Systemes
Ian Steff	President and Chief Executive Officer	mySilicon Compass, LLC
Edward Tiedemann	Senior Vice President	Qualcomm
Samuel Valenti	Vice President, Engineering and Technology	Space & Airborne Systems/L3Harris Technologies
Ronnie Vasishta	Senior Vice President	NVIDIA
Patrick Wilson	Vice President, Government Relations	MediaTek
Philip Wong	Willard R. and Inez Kerr Bell Professor, ECE	Stanford University
Jie Xue	Vice President, Technology and Quality	Cisco Systems
Anthony (Tony) Yen	Vice President and Head of Technology Development Center	ASML

CEO Endorsements for the Purdue Semiconductor Degree Program

"The foundation of U.S. semiconductor leadership is America's talented technology workforce. It is critical we support and strengthen this workforce by creating, promoting, and investing in policies and programs that enable the training and retention of skilled semiconductor talent. I am thrilled Purdue University is taking a bold step in this mission with the creation of its new credentials and degrees focused on microelectronics and semiconductors at the undergraduate and graduate level. We strongly support these exciting and innovative initiatives."

John Neuffer, President and CEO, Semiconductor Industry Association (SIA)

"AI is the most impactful technology of our time. The automation of intelligence expands humanity's potential, enabling once-unimagined advances across science, industry and even the arts. Leadership in this era will require a new generation of engineers and computer scientists. It's exciting to see Purdue establish this program to prepare students for this challenge, enabling them to help shape fields from autonomous vehicles and robots to healthcare and climate science, and improve our world."

Jensen Huang, President and CEO, NVIDIA

"I am pleased to hear about the new graduate and undergraduate credentials and degrees on microelectronics and semiconductors being launched at Purdue University. These innovative and much-needed initiatives will play a key role in satisfying the voracious demand for skilled talent in the semiconductor industry. I am confident that graduates from this program will be in much demand at Lattice and other companies in our industry."

Jim Anderson, President and CEO, Lattice Semiconductor

"As one of the world's leading semiconductor manufacturers based in the U.S., GlobalFoundries strongly supports the efforts to grow U.S.-based semiconductor manufacturing. We recognize that to accomplish this goal, the shortage of semiconductor talent in the U.S. is a critical challenge the nation must address. I am pleased and encouraged to see Purdue University step up to this challenge by introducing a comprehensive set of degrees and credentials that will prepare students for exciting careers in semiconductors. We look forward to partnering with Purdue as these programs ramp up to support microelectronics across the U.S."

Thomas Caulfield, CEO and President, GlobalFoundries

"Today, semiconductors are more strategically and economically important to the world than ever and we need to significantly scale up the talent pipeline to support the future growth of our industry. Applied Materials is delighted to see Purdue University helping lead the charge to educate the tens of thousands of new engineers our industry needs through new degrees and credentials focused on microelectronics and semiconductors. We look forward to welcoming this next generation of innovators."

Gary Dickerson, President and CEO, Applied Materials, Inc.

"Every aspect of human existence is becoming digital, and everything digital runs on semiconductors. Increasing access to semiconductor and microelectronics education is essential for building a talented, diverse pipeline of future technologists. Intel plans to invest $100 million over the next decade to build a skilled semiconductor workforce in collaboration with universities, community colleges, and the NSF. I'm excited about Purdue's educational credentials focused on semiconductors and microelectronics, including the new interdisciplinary master's degree. With these timely and high-impact initiatives, Purdue is leading the way in bridging the skills gap and addressing the shortage of skilled human talent in the semiconductor industry."

Pat Gelsinger, CEO, Intel

"For three and a half decades, Synopsys has provided innovative design automation technology and products that catalyze the potential of semiconductor chips. Today, an exciting new era of microelectronics characterized by both scale and systemic complexity is beginning, and Purdue's new degrees and credentials will equip students with the practical skills needed in this new age. This initiative leads the way with the kind of comprehensive, innovative program that design automation and semiconductor companies, as well as the electronics ecosystem, critically need."

Aart de Geus, Chairman and CEO, Synopsys

"Semiconductors are the backbone of our digital society and global economy. Increasing investment in semiconductor education to train the next generation of technologists is vitally important for the long-term health and success of our industry. Purdue University's new graduate and undergraduate credentials and degree programs in semiconductors and microelectronics can serve as an incubator for the ideas and innovations of tomorrow. We strongly support this initiative and look forward to welcoming Purdue graduates to Marvell in the future."

Matt Murphy, President and CEO, Marvell

"It is essential for the United States to be a self-sufficient leader in semiconductor technology, which provides the foundation for the modern world and will lead to new innovations in critical industries. Purdue University's new credentials and degrees in microelectronics and semiconductors will help ensure that we have the large, skilled workforce that is needed to power the nation's semiconductor future."

Arvind Krishna, Chairman and CEO, IBM

"Semiconductor manufacturing requires a vast array of highly engineered and advanced materials and chemistries. CMC Materials and other leading materials companies look forward to supporting the expansion of semiconductors in the United States and globally. For the bold innovation in critical materials that is needed to advance technology and increase performance, a new generation of semiconductor engineers is critically needed. Purdue's new degrees and credentials will help students develop the depth and breadth needed for an exciting new era of technology that is just beginning. Kudos to Purdue for stepping up to address this key challenge for the U.S. semiconductor industry. Go Boilers!"

David Li, President and CEO, CMC Materials

"TSMC looks forward to being part of the resurgence of semiconductor manufacturing in the U.S. Success in this ambitious and critically important undertaking will require a much-expanded semiconductor talent with the knowledge and skills needed to innovate in a post-Moore's Law era. Purdue's innovative and comprehensive new suite of semiconductor degrees and credentials is exactly what is needed – at exactly the right time. We at TSMC look forward to working with Purdue to make this program a model for the nation."

Mark Liu, Chairman, TSMC

"Differentiated technologies that address a growing diversity of applications will characterize the next wave of electronics. This next wave will be driven by creative engineers with a broad understanding of microelectronics from materials, devices, and circuits to systems, packaging, and qualification. SEMI is delighted to partner with Purdue as part of the American Semiconductor Academy initiative, and I am pleased to see the university leading the way with the kind of comprehensive and innovative program that the semiconductor industry critically needs."

Ajit Manocha, President and CEO, SEMI

"Recent events have taught us all how critical chips are and how fragile supply chains can be, but a re-energized U.S. microelectronics landscape will require more than just building more fabs. As Moore's Law slows, new ways to advance the performance of electronics systems are needed, and this will require a new generation of bold and creative semiconductor engineers to pioneer equally as bold and creative semiconductor devices. I applaud Purdue in addressing this challenge with a comprehensive set of new semiconductor degrees and credentials that will help prepare a new generation of semiconductor engineers and address a critical need for Nantero and other companies."

Rob Snowberger, CEO, Nantero

"SkyWater sees tremendous value in partnering with Purdue University. They have tremendous faculty, researchers, and facilities around semiconductor creation. Their student body is developing into the workforce of the future, and with the new degree programs dedicated to semiconductors, those are just the graduates that SkyWater needs."

Thomas Sonderman, President and CEO, SkyWater

"We are entering an exciting new era of semiconductors with unprecedented demand driven by the need to execute artificial intelligence (AI) compute workloads. Graphcore is transforming the AI compute domain through innovative technologies that are going to be transformative across all industries and sectors with a real potential for positive societal impact from drug discovery and disaster recovery to decarbonization. Sustaining the rapid pace needed to have such an impact is going to require a big increase in the size of the semiconductor talent pool. I am excited to see Purdue leading the mission to educate the next generation of semiconductor workforce leaders by launching an innovative set of credentials and degrees. I expect this initiative to be a real difference-maker."

Nigel Toon, CEO, Graphcore

"Electronics is more and more often the differentiating factor in products, but the cost and complexity of design is exploding. As Efabless works to make custom chip design affordable and accessible to more companies, a critical challenge is the shortage of microelectronic talent. I applaud Purdue University for stepping up to this challenge. Purdue's new degrees and credentials meet prospective talent where they are with education and opportunity. This will help the next generation of students develop the knowledge, skills, and experience needed for an exciting new era of electronics."

Mike Wishart, CEO, Efabless

"We, at SRC, have sponsored more than 16,000 undergraduate and graduate research scholars and have a stated mission of building a diverse, inclusive, and highly trained workforce for tomorrow. Purdue's new credentials and degrees on microelectronics and semiconductors represent excellent and much-needed initiatives in semiconductor workforce development. We have a strong partnership with Purdue in the microelectronics revolution and look forward to further expanding this partnership to address the enormous possibilities for the industry and our country."

Todd R. Younkin, President and CEO, Semiconductor Research Corporation (SRC)

Purdue Semiconductor Degree Program

Purdue's reputation as an R&D trailblazer is matched by its leadership in workforce development programs for semiconductors. Several programs described below attest to a strong University culture, a tradition of innovation in workforce development, and an array of recent successes related to microelectronics training at scale.

Semiconductors Degrees and Certifications

A comprehensive new undergraduate semiconductor program has been launched in spring 2022. The undergraduate experience will begin with a new course "Changing the World with Chips—Introduction to Semiconductors", access to internships or co-op experiences to semiconductor undergraduates, continuing to semiconductor minors, concentrations and certificate, and a 5-year BS/MS program that will give students additional semiconductor knowledge and experience. The new interdisciplinary MS degree will be the only such degree focused entirely on semiconductors and microelectronics offered at any of the top-10 ranked Engineering Colleges in the country. These credentials and degrees will be available both for on-campus and online students.

> Purdue is the first U.S. university to launch a comprehensive set of minors and concentrations for undergraduates, Masters programs, and certificates, residential and online, dedicated to semiconductors along its entire supply chain to address the nation's critical need for microelectronics engineers.

TYPE OF DEGREE OR CREDENTIAL	RESIDENTIAL	ONLINE
Interdisplinary, 6-in-1 MS Degree	✓	✓
Graduate Concentration (MS and PhD)	✓	✓
Stackable Certificates	✓	✓
Undergraduate Concentration and Minor	✓	
Introduction to Semiconductors Freshman Course	✓	✓

Internships, Co-Ops, and Learning While Working

Purdue runs one of the largest and best undergraduate industry internship and co-op programs in the nation. Besides the inaugural semiconductor suite of degrees, Purdue has also created a Learning While Working program, enabling students to work towards their degrees while working full time. A good number of companies are subscribing to this model, running in parallel with internship and co-op programs.

https://www.opp.purdue.edu/

Partnerships

Recognizing the need to contribute to the entire range of microelectronics workers, Purdue is partnering with Ivy Tech Community College to develop several programs aimed to increase the number of technicians and also to strengthen the pipeline for four-year degrees. Ivy Tech has more than 40 locations across Indiana and teaches classes in more than 75 communities serving nearly 100,000 students annually. Ivy Tech is the largest public postsecondary institution in Indiana and the largest singly-accredited statewide community college system in the country. Additional partnerships are explored with academic partners, such as Rose Hulman Institute of Technology.

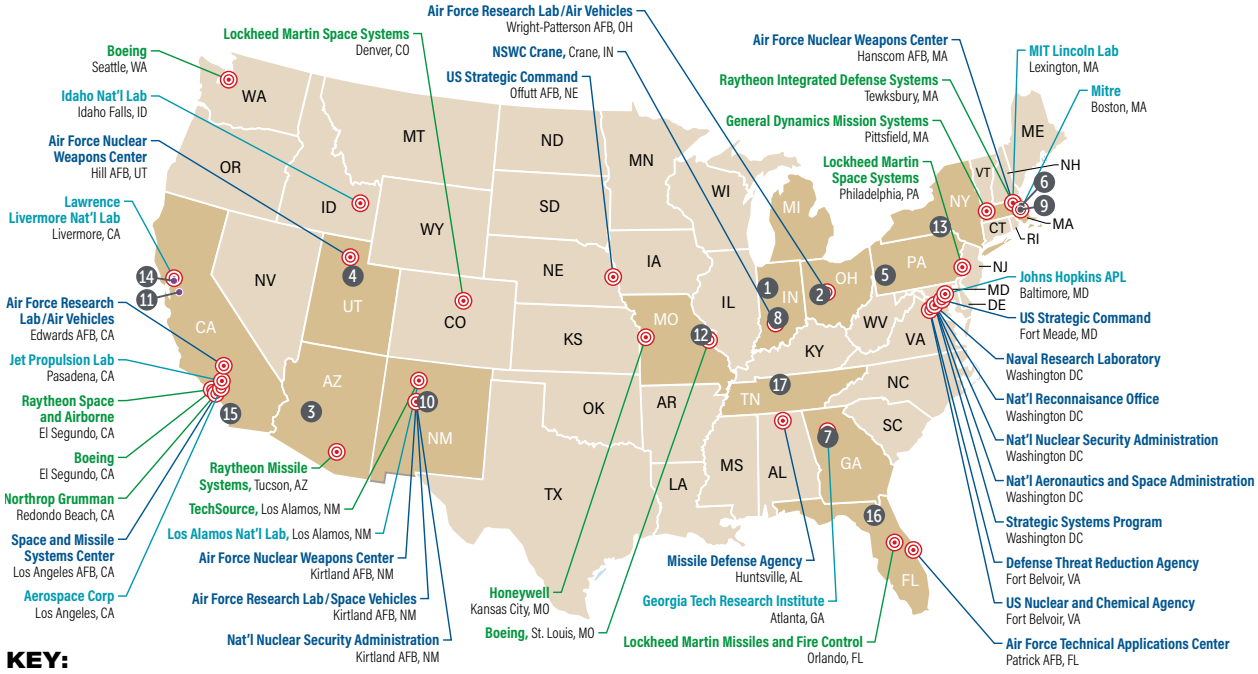
SCALE DoD Microelectronics WFD Center

Purdue University is leading a five-year, DoD-sponsored national initiative aimed at addressing the urgent need to develop a highly skilled U.S. microelectronics workforce to bolster national security. Comprising of 19 partner universities across the country, Scalable Asymmetric Life Cycle Engagement (SCALE) is a $42.8M—with a funding ceiling up to $99M—public-private-academic partnership formed to advance the technical capabilities of the domestic microelectronics workforce, and to motivate talented STEM undergraduate and graduate students to pursue federal government careers in the semiconductor field.

SCALE is being managed in partnership with the Naval Surface Warfare Center Crane Division as a nationally coordinated network of government, industry, and university partners, with regional execution. Faculty from across Purdue's College of Engineering are collaborating with experts from 19 other universities, the DoD, NASA, the Department of Energy NNSA labs, and the defense industry to create a microelectronics workforce focused on national security needs.

The workforce development program provides microelectronics modules, mentoring, public- and private-sector internship matching, and targeted research projects for college students interested in these microelectronics specialty areas:

- Radiation hardening
- Heterogeneous integration/advanced packaging
- System-on-chip electronics
- Embedded systems security/trusted artificial intelligence (AI)
- Radio frequency Optical electronics



KEY:

Target Institutions: Government · Federally Funded Research and Development Centers · Industry

Partners: (**Institution Topic Areas: RH** = Radiation Hardened, **HIAP** = Heterogeneous Integration/Advanced Packaging, **SC** = Supply Chain, **ESS** = Embedded Systems Security, **SoC** = System on Chip)

1. **Purdue University,** West Lafayette, IN (RH, HIAP, SC, ESS, SC)
2. **Air Force Institute of Technology,** Wright-Patterson Air Force Base, OH (RH)
3. **Arizona State University,** Tempe, AZ (RH, HIAP, SC)
4. **Brigham Young University, Provo,** UT (RH)
5. **Carnegie Mellon University,** Pittsburgh, PA (ESS, SoC)
6. **Draper Laboratory,** Campridge, MA (RH)
7. **Georgia Institute of Technology,** Atlanta, GA (RH, HIAP, SC, ESS, SoC)
8. **Indiana University,** Bloomington, IN (ESS, SoC)
9. **Massachusetts Institute of Technology,** Boston, MA (ESS, SoC)
10. **Sandia National Laboratory,** Albuquerque, NM (RH)
11. **Sandia National Laboratory,** Livermore, CA (RH)
12. **St. Louis University,** St. Louis, MO (RH)
13. **State University of New York at Binghamton,** NY (HIAP)
14. **University of California,** Berkeley, CA (ESS, SoC)
15. **University of California,** San Diego, CA (ESS)
16. **University of Florida,** Gainesville, FL (SC)
17. **Vanderbilt University,** Nashville, TN (RH)

SCALE Faculty include: Peter Bermel (Principal Investigator), Kerrie Douglas (Program Director), Tom McKinley (Managing Director), Ashraf Alam, Joerg Appenzeller, Shubhra Bansal, Nikhilesh Chawla, Allen Garner, Selcen Guzey, Carol Handwerker, Eric Holloway, Morgan Hynes, Mark Johnson, David Johnson, Jenn Linvill, Amy Marconnet, Saeed Mohammadi, Tamara Moore, Anand Raghunathan, Vijay Raghunathan, Kaushik Roy, Shreyas Sen, Alejandro Strachan, Ganesh Subbarayan, and Justin Weibel

For more information, visit: https://www.purdue.edu/discoverypark/scale/index.php

Purdue Summer Training, Awareness, and Readiness for Semiconductors (STARS)

Purdue University launched the 2023 Summer Training, Awareness, and Readiness for Semiconductors (STARS) program this past May. The eight-week program is designed to develop deep-tech skills like IC design, fabrication, and packaging, and semiconductor device and materials characterization. The program consisted of two tracks: chip design and semiconductor manufacturing. Students in each track participated in hands on activities in the Scifres Nanotechnology Cleanroom.

Students in the semiconductor design track received experience in designing, verifying, and submitting a digital integrated circuit for fabrication (tape-out). Students practiced discrete circuit construction and use of bench instrumentation. Students designed, simulated, and created FPGA prototypes of combinational logic functions such as multiplexers, adders, and decoders. Students then moved on to sequential functions such as state machines, counters, and shift registers. Students were also guided in using rigorous block diagrams to plan more designs based on many instances of functions implemented previously. Near the end of the program, students integrated their designs and ran the designs through a place and route and physical verification process. The design track was led by Dr. Mark C. Johnson.

Students in the semiconductor manufacturing track focused their skill development on chip fabrication, semiconductor materials, and device characterization. Students learned about cleanroom safety, substrate engineering, oxidation, lithography, thin film deposition (physical vapor deposition and atomic layer deposition), reactive ion etching and wet chemicals-based cleaning and etching, thermal diffusion and annealing, ion implantation, chemical mechanical polishing (CMP), and basic integration of MOSCAP and CMOS devices. For the material characterization, students learned about atomic force microscopy, x-ray diffraction analysis, secondary ion mass spectroscopy, scanning electron microscopy, x-ray photoelectron spectroscopy, and transmission electron microscopy. For the device characterization, students learned about MOSCAP and MOSFET performance and reliability measurement and analysis. The manufacturing track was led by Dr. Muhammad Hussain.

The final week consisted of a speech competition and portfolio exercise where the students competed for the opportunity to participate in SEMICON West. We are already looking at 2024, and are welcoming sponsors. If you would like to participate, please email Cristina Farmus at cfarmus@purdue.edu.

Thank you to our 2023 sponsors!

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High School READI Program

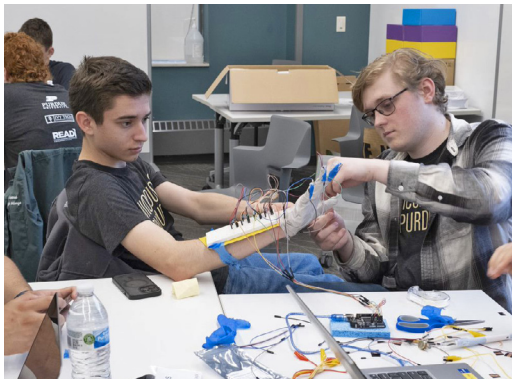
Fifty-five students from six counties and 12 different high schools in and around Tippecanoe County and the Greater Lafayette area have completed a two-week program that could give them a leg up in the rising semiconductor industry. The students were recognized for this achievement on June 16 during a graduation ceremony inside Convergence at Discovery Park District (DPD).

The event was the culmination of a partnership between Purdue University and Ivy Tech Community College to develop a talent pipeline of students and increase technician and engineer training to support the region's expected workforce demand for advanced semiconductor manufacturing. That demand is largely due to the planned construction of SkyWater Technology's $1.8B state-of-the-art facility in DPD. It is predicted that the 600,000-square foot plant will generate more than 700 jobs with annual salaries ranging from $60K for technicians to $130K for development and management positions.

In addition to building a wearable sensor and learning how to program a robot, the group of rising juniors and seniors, who split their time between Purdue and Ivy Tech, gained exposure to printed electronics and solar cells, designed and fabricated their own printed circuit boards

(PCBs) to measure the state-of-charge of a battery, and used semiconductors to solder electronic components onto their PCBs. Ultimately, students worked together in small teams in a three-day workshop to create their own custom projects out of paper electronics, which include a robo-spotter to automate safety in weightlifting, for personalized data dashboards, and an electronic safe. Also included in Ivy Tech's portion of the program was an overview of the soft skills required to be successful in the semiconductor industry. Participants attended a workshop to develop elevator speeches, then delivered them to peers and instructors.

Organizers are planning for summer 2024, when the program is expected to continue with even more students.



nanoHUB—Global Online Workforce Development

Purdue Engineering Online

nanoHUB is a vibrant and inclusive community. Over 1 million visitors download nanoHUB's educational materials each year, and 12,000 students in classes access nanoHUB simulation tools for semiconductors and materials. 16% of nanoHUB's simulation users are at minority-serving institutions (MSIs).

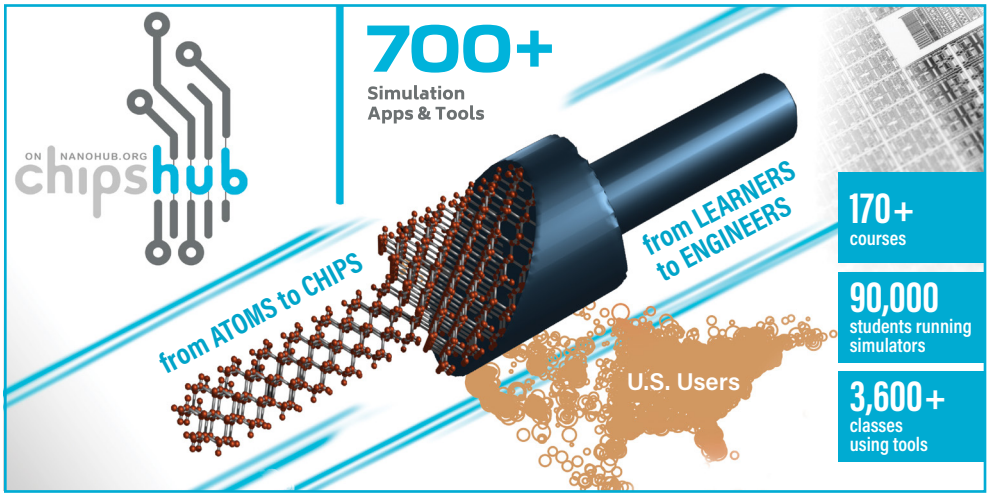
nanoHUB supports semiconductor workforce development at scale, providing industry-strength Computer Aided Design (CAD) and engineering tools, open-source and research-based tools that do not require students or instructors to download, install, license, support, or maintain the software. Instead, nanoHUB's Apps and Tools are accessible through any web browser and run on nanoHUB's computing cloud. Modeling, Simulation, and Data are available to users as both stand-alone tools and part of structured teaching and learning curricula. Most of the Tools are wrapped by easy-to-use Apps that do not require instructional manuals.

nanoHUB hosts over 700 Apps and Tools used by over 180,000 simulation users. 90,000+ of these were students in 3,600+ classes. 6,500+ other content items provide scaffolding around these tools consisting of free textbooks, over 170 complete courses, lectures, tutorials, homework, and project assignments. A subset of nanoHUB's resources is curated in a special group page for semiconductor workforce development. https://nanohub.org/groups/semiconductoreducation

From nanoHUB.org to chipshub.org—From Atoms to Chips

nanoHUB began in 1995 as one of the first web portals to provide access to scientific simulation tools via web forms. Even before the Apple iPhone, nanoHUB was creating user-friendly, easy-to-use Apps and created the first scientific end-to-end cloud before the "cloud" became a thing. Notably, in 2017 the Web of Science began listing nanoHUB Apps and Tools as a new type of digital publication. nanoHUB has demonstrated that it can overcome the barriers of entry to using computational simulation tools and project collaboration that were posed by complex software installation, software licensing, and computation hardware provisioning.

chipshub builds on nanoHUB's demonstrated competencies in delivering both open-source and commercial software in a simple-to-use cloud environment, provisioning needed educationally scaffolded materials, and building a community that rapidly embraces workforce development at scale. nanoHUB already hosts several commercial tools from SILVACO, ThermoCalc, and MATLAB. We are installing Cadence tools right now and are in license discussions with both Synopsys and Siemens. In addition to design tools, the chipshub infrastructure will enable chip manufacturing to be performed, seamlessly, with nanoHUB's partners. "From lab to fab": Using chipshub, students will be able to architect, design, optimize, and test chips in a single platform without any software installation, and faculty will be empowered to adopt newly available educational resources.



We envision chipshub will impact over 220,000 U.S. engineering students and specifically over 49,000 designers over 5 years.

Semiconductor Facilities

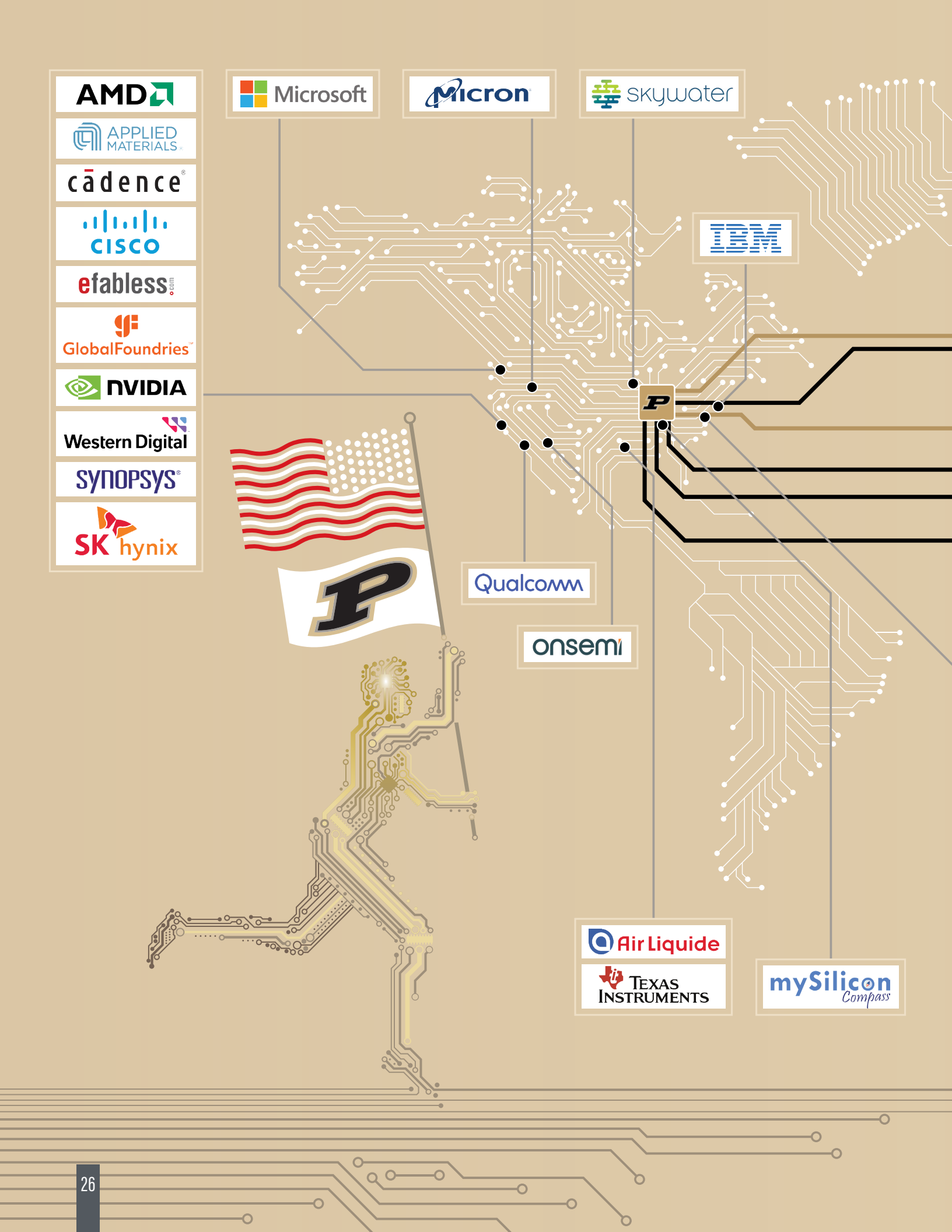
Purdue Investing $100 million in Semiconductor Facilities

For a virtual tour of Birck Nanotechnology Center, go to:
https://www.purdue.edu/discoverypark/birck/

Purdue University has announced $100 million of semiconductor facility updates with phase one of $49 million being approved by the Purdue Board of Trustees in April of 2023, for capital project and equipment procurement to upgrade the 18-year-old national treasure Birck Nanotechnology Center. The $49 million project will increase cleanroom space, add fabrication and characterization equipment and capabilities, and enhance the facility's capacity to support the lab-to-lab transition for CHIPS Act initiatives. This enhanced state-of-the-art facility will also support Purdue's broader, longterm research goals. The goals of the CHIPS and Science Act are to advance microelectronics and advanced packaging research and foster collaborations with industry partners. This project will enable Purdue to support this mission by providing Birck researchers with the resources they need to accelerate innovation, work efficiently with industry collaborators, and achieve the goals of CHIPS and Science Act through development of new technologies that can revolutionize the semiconductor industry. Purdue is committed to driving innovation and economic development, and this project underscores Purdue's commitment to providing critical resources to help our researchers become even more impactful. By supporting industry collaborations and the lab-to-fab transition, the Birck Nanotechnology Center is playing a critical role in helping to bring cutting-edge technologies to manufacturing. Construction on the project is expected to begin in the Fall of 2023, with completion targeted for Fall of 2024.

About the Birck Nanotechnology Center

The Birck Nanotechnology Center at Purdue University is a multidisciplinary research facility that includes professionally staffed 25,000 square foot. Scifres Nanofabrication Laboratory cleanroom and its state-of-the-art suite of tools. Together with specialized characterization labs throughout the Birck facility, this creates an environment for the research community to design, fabricate and characterize materials and devices at the nanoscale and integrate them at the advanced system and packaging level. Birck enables collaboration among faculty, researchers, and staff engineers, and facilitates partnerships with other academic institutions, industry, and government. It serves as a platform for public and private partnerships, bringing together diverse expertise and resources to address pressing challenges in the field of nanotechnology.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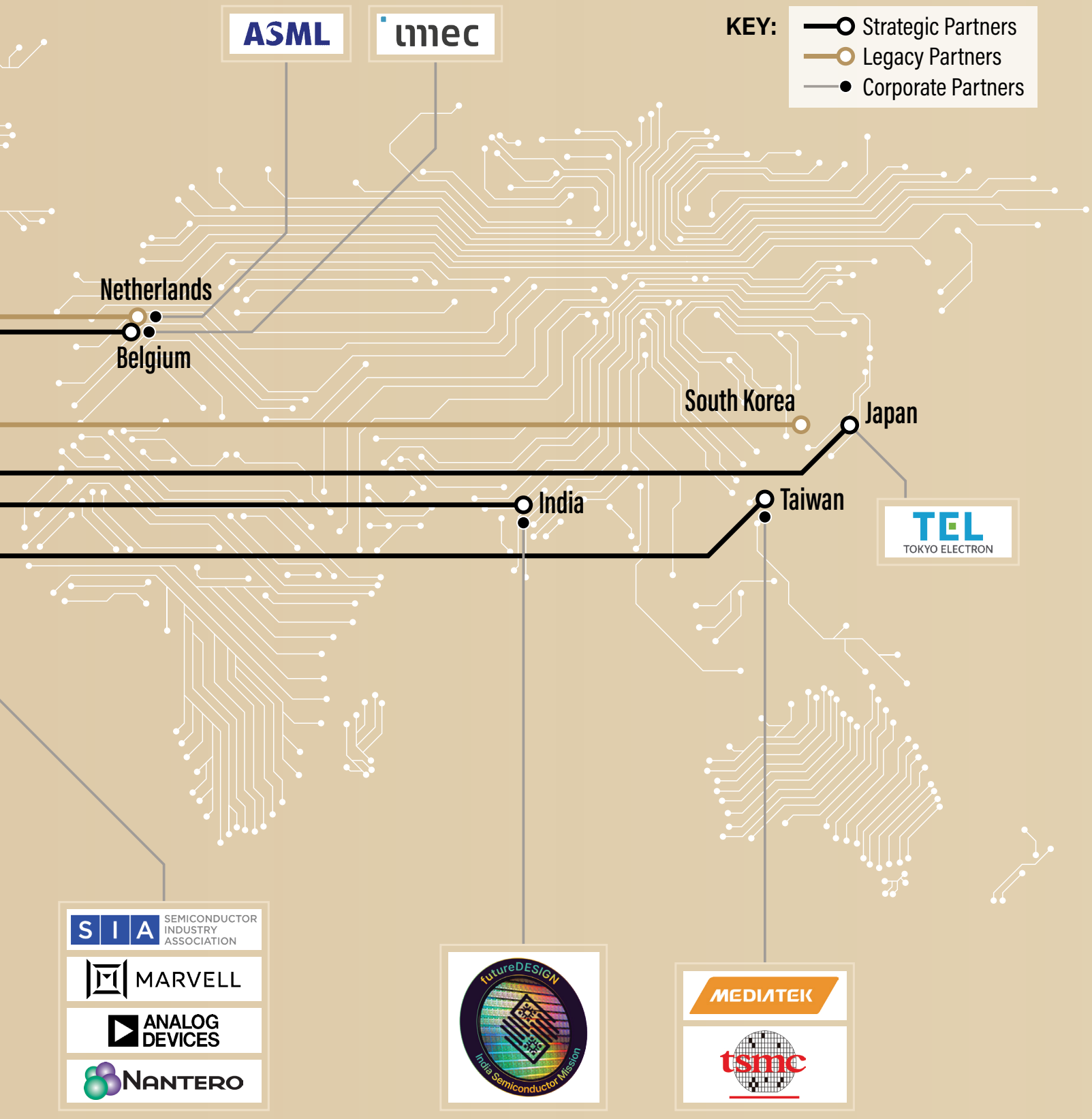


Purdue International Partnerships on Semiconductors

Purdue Signs Landmark U.S.-Japan Agreement in Semiconductors at G7 Summit

On May 21st, 2023 in Hiroshima, Japan, Purdue President Mung Chiang signed another landmark international agreement, partnering with Micron, Tokyo Electron, and other educational institutions in the U.S. and Japan to establish the "UPWARDS Network" for workforce advancement and research and development in semiconductors. The announcement was made during this year's Group of Seven (G7) summit in Hiroshima, which also included the Quad countries and other world leaders. The agreement was signed in the presence of U.S. Secretary of State Antony Blinken; Keiko Nagaoka, Japan's Minister for Education, Culture, Sports, Science and Technology; and Rahm Emanuel, U.S. Ambassador to Japan. The signatories later had a meeting with U.S. President Joe Biden at the end of the summit. Micron and Tokyo Electron, as founding industry partners, the National Science Foundation and universities together will invest over $60 million for the five-year project. Other U.S. university participants included in the Memoranda of Understanding (MOU) are Boise State University, Rensselaer Polytechnic Institute, Rochester Institute of Technology, the University of Washington, and Virginia Tech, while the Japanese university participants are Hiroshima University, Kyushu University, Nagoya University, Tohoku University, and Tokyo Institute of Technology.

President Joe Biden and Purdue President Mung Chiang at the G7 Summit in Japan.

Photographed above:

President Joe Biden
Prof. Mung Chiang, *President, Purdue University*
Rahm Emanuel, *U.S. Ambassador to Japan*
Hideo Ohno, *President, Tohoku University Mitsuo Ochi*
Marlene Tromp, *President, Boise State University*
Sanja Mehrotra, *CEO, Micron*
Among others

U.S.-Europe Semiconductors Collaboration

Purdue University and the state of Indiana continue to make giant leaps in semiconductor research growth with a first-of-its-kind agreement with a cutting-edge European nano- and digital technology innovation hub.

imec joined Indiana Governor Eric Holcomb, U.S. Senator Todd Young, Indiana Secretary of Commerce Brad Chambers, and Purdue President Mung Chiang in announcing the partnership during the SelectUSA Investment Summit, an annual international investment event by the U.S. Department of Commerce near Washington, D.C. With research sites across Belgium, imec leverages state-of-the-art research and development in advanced semiconductor technologies and artificial intelligence, uniting world-industry leaders across the semiconductor value chain.

The collaboration and equal investment between the three entities will strengthen the growing semiconductor ecosystem in Indiana and at Purdue with a steady exchange of expertise in the continually evolving and expanding industry. A stream of students, faculty, and professionals are expected to bolster the already growing semiconductor foundation at Purdue with new innovations and research.

> *"This MOU signed with Purdue University holds great significance for imec. It provides us with a unique opportunity to act as a major catalyst of worldwide semiconductor R&D in collaboration with a world-class American research university. This collaboration between these two R&D powerhouses from the U.S. and Europe underscores my strong conviction that international collaboration in semiconductor research and development is imperative for expediting progress by building on our strengths and innovating faster together. Advocating and executing on that spirit of collaboration is what imec is all about and we look forward to working with Purdue to strengthen the innovation ecosystem in the U.S. and Europe."*
>
> **Luc Van den hove,** imec CEO

(Photo: Purdue University)

Left to right:

Joe Pasetti, *Vice President of Corporate Affairs, imec*

Jimmy Costa, *Senior Vice President of Innovation and Semiconductor Strategy, Applied Research Institute Inc.*

Max Mirgoli, *Executive Vice President of Worldwide Strategic Partnerships, imec*

Prof. Mark Lundstrom, *Senior Advisor to the President and Chief Semiconductor Officer, Purdue University*

Prof. Mung Chiang, *President, Purdue University*

Brad Chambers, *Secretary of Commerce, Indiana*

Todd Young, *U.S. Senator, Indiana*

Eric Holcomb, *Govenor, Indiana*

Luc Van den hove, *CEO, imec*

Jillian Turner, *Senior Vice President, Global Investment and Partnerships, Indiana Economic Development Corporation*

Purdue and India Semiconductor Mission

On May 9th, 2023, Purdue President Mung Chiang signed an agreement establishing itself as a key collaborator with India and the India Semiconductor Mission (ISM) in skilled workforce development and joint research and innovation in the burgeoning fields of semiconductors and microelectronics. Purdue signed the agreement with the leadership of the India Semiconductor Mission in the presence of Honorable Minister Ashwini Vaishnaw, who is in charge of Railways, Communications, Electronics and Information Technology in India and also oversees the country's semiconductors program. With the agreement, Purdue will focus on:

1. Creating cutting-edge online and hybrid academic programs for specialized training in areas including chip design and fabrication, advanced packaging, semiconductor materials, and embedded system design that can be made available to Indian students as ISM-endorsed training programs, both as noncredit offerings and through integration into the curricula of Indian educational institutions.
2. Exploring the creation of dual-degree programs in semiconductors and microelectronics with Indian educational institutions.
3. Joint research and development programs aimed at designing, manufacturing, and commercializing semiconductor chips.
4. Driving technological advancement and strengthening bilateral relations between the U.S. and India by facilitating collaborations with Indian educational institutions and companies, to obtain joint funding opportunities in the areas of semiconductor research and chip design, manufacturing, and commercialization.

Purdue's Memoranda of Understanding (MOU) with India and ISM is for five years, with the opportunity to renew. This collaboration aligns with ISM's mission of driving India's strategies for developing a comprehensive semiconductors and display ecosystem. The agreement falls under the Semiconductor Supply Chain Innovation Partnership, signed by the U.S. and India on March 10th, 2023. It is also aligned with the U.S. and India initiative on Critical and Emerging Technology (iCET) partnership launched by the National Security Advisors of the U.S. and India in January 2023, collaboration in emerging and critical technologies, including semiconductors, artificial intelligence and quantum computing.

Left to right:

Dr. T.V. Nagendra Prasad, *Consul General of the Indian Consulate in San Francisco*

Hon. Ashwini Vaishnaw, *India's Union Minister for Railways, Communications, Electronics and IT*

Prof. Mung Chiang, *President, Purdue University*

Prof. Vijay Raghumathan, *Director of Semiconductor Education, Purdue University*

(Photo: Purdue University)

Inaugural Meeting of the U.S.-India Semiconductor Collaborative

On June 23, 2023, Purdue University President Mung Chiang joined top U.S. and Indian government officials and technology industry leaders in Washington, D.C. for the inaugural meeting of the U.S.-India Semiconductor Collaborative, aimed at growing the relationship between Purdue and the South Asian nation. The roundtable event, co-hosted by Purdue and SEMI, a global industry association serving the electronics design and manufacturing supply chain, coincided with the first official state visit to the U.S. of Indian Prime Minster Narendra Modi.

Attendees at the Semiconductor Collaborative's launch event included U.S. Senator Todd Young (R-Indiana); Congressman Jim Baird (Indiana-D4); India's Union Minister for Electronics and IT, the Honorable Ashwini Vaishnaw; Assistant Secretary of State, the Honorable Ramin Toloui; Deputy Director of NIST's CHIPS R&D Office Eric Lin; SEMI CEO Ajit Manocha; India Semiconductor Mission CEO Amitesh Sinha; and the Director of the Indian Institute of Technology Madras, V. Kamakoti. Senior executives from leading U.S. technology companies including Micron, Intel, IBM, Texas Instruments, MediaTek, GlobalFoundries, Microsoft, Marvell, Synopsys, Cadence, NVIDIA, and others also participated in the meeting and shared their ideas and support for a strong semiconductors partnership between the two countries.

Hailing the U.S.-India relationship as one of the most defining relationships of this century, Minister Vaishnaw said, "Our cooperation in the area of semiconductors and critical and emerging technologies is vital. The recently signed Purdue-ISM MOU adds value to Purdue, the U.S., and India."

Vaishnaw thanked the U.S. government and partners for their great cooperation and reinforced that the U.S.-India relationship will define the world order in the coming years.

The attendees discussed that a goal is to prepare for the G20 meeting in September 223 and compile a roadmap to advance research and development in semiconductors between the two countries.

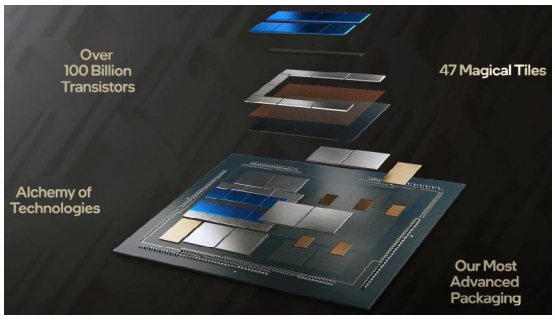
Nearly three-dozen representatives from leading U.S. tech companies and Indian government officials took part in the inaugural U.S.-India Semiconductor Collaborative, hosted by Purdue and semiconductor industry organization SEMI in Washington, D.C. The event coincided with the official state visit of Indian Prime Minister Narendra Modi.

(Photo: Purdue University photo/Pooja Chaudhary)

Research Centers

C-BRIC

The Center for Brain-inspired Computing (C-BRIC) is funded by SRC and DARPA under the JUMP center program. Led by Professors Kaushik Roy (Director) and Anand Raghunathan (Associate Director), C-BRIC has a mission to deliver key advances in cognitive computing that will enable a new generation of autonomous intelligent systems such as self-flying drones and interactive personal robots. C-BRIC is led by Purdue and includes researchers from 11 universities working on neuro-inspired algorithms and theory, neuromorphic computing fabrics, and distributed intelligence. C-BRIC brings together experts from machine learning, computational neuroscience, theoretical computer science, integrated circuits and systems, distributed computing, robotics, and autonomous systems to pursue improvements in cognitive systems that are difficult for these communities to achieve independently.



CHIRP

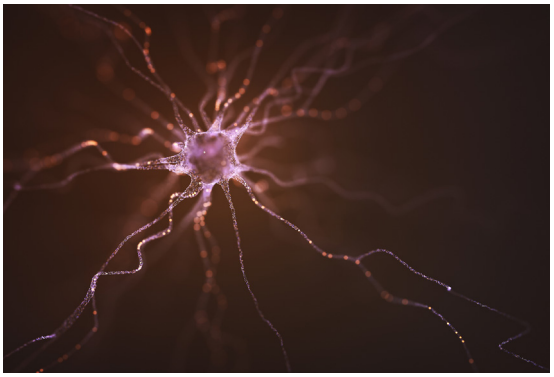
The Center for Heterogeneous Integration Research on Packaging (CHIRP) is co-directed by Ganesh Subbarayan of Purdue and Bahgat Sammakia of SUNY Binghamton. CHIRP's mission is to enable the building of future Systems-in-Package through Heterogeneous Integration. The areas of CHIRP research focus include design enablement, global interconnects, power delivery, thermal management, modeling, metrology, and reliability that together optimally address the power, performance, area, and cost metrics of systems. CHIRP also works to educate engineers who can design and build heterogeneously integrated systems. The center was established in 2019 with support from ARM, Intel, IBM, MediaTek, NXP, Samsung, and Texas Instruments, and has since funded over $6M in projects. CHIRP engages nearly 20 investigators from Purdue and SUNY Binghamton.

NEW LIMITS

The NEW Materials for Logic, Memory and InTerconnectS (NEW LIMITS) center is directed by Professor Zhihong Chen. The center's vertically integrated mission is to develop synthesis, integration, and evaluation schemes for new materials that will be used in unique logic, memory, and interconnect applications to enable novel computing and storage paradigms beyond the capabilities of conventional CMOS. The key idea is to utilize the properties of 2D material systems that are NON-EXISTENT in traditional 3D materials to achieve the performance or realize the novel functionalities that existing technologies are not able to offer. The center covers the following research vectors: material and device research, nanofabrication and advanced manufacturing processes, innovative metrology and characterization, and simulation and modeling.

CSME

The Center for a Secure Microelectronics Ecosystem (CSME) was launched with support from founding companies TSMC and Synopsys in conjunction with support through a U.S. Department of Defense (DoD)-funded workforce development program. CSME is co-directed by Professors Joerg Appenzeller and Anand Raghunathan. CSME is a first-of-its-kind global partnership of academia, industry, and government to advance research and workforce development in designing secure microelectronics. Its aim is to enable the creation of secure semiconductor chips and related products, from the foundry to the packaged system, based on a zero-trust model. CSME will provide advanced training opportunities to SCALE participants, while SCALE will support CSME through graduate traineeships, addressing the urgent need for engineering graduates with secure microelectronics skills.



ICC

The Institute for Cognitive Computing aims to advance the field of cognitive computing through cross-layer innovation spanning brain-inspired computing models, algorithms, architecture, and hardware fabrics. The institute brings together faculty with diverse backgrounds to pursue these goals by facilitating collaborative research and training the next generation workforce in this critical domain.

COOLING TECHNOLOGIES RESEARCH CENTER

CTRC

The Cooling Technologies Research Center (CTRC) is a graduated National Science Foundation Industry/University Cooperative Research Center and addresses pre-competitive, longer-term research and development issues in the area of high-performance heat removal from compact spaces.

Purdue Engineering to Play Key Role in Two New SRC JUMP 2.0 Centers

Purdue University College of Engineering faculty have been tapped for leadership positions in two new research centers launched by the Semiconductor Research Corporation (SRC) and the Defense Advanced Research Projects Agency (DARPA) to accelerate U.S. advances in information and communications technologies.

The Joint University Microelectronics Program 2.0 (JUMP 2.0) is a public-private partnership co-sponsored by the SRC, DARPA, the commercial semiconductor industry and the defense industrial base. JUMP 2.0 will pursue high-risk, high-payoff research spanning seven thematically structured centers.

Purdue faculty, all representing the Elmore Family School of Electrical and Computer Engineering (ECE), will take on lead research roles and lend expertise in semiconductors and hard artificial intelligence to two of the centers, in which investment totals $65.7 million. Both multi-university centers are led by Georgia Institute of Technology.

In the Center for the Co-Design of Cognitive Systems (CoCoSys), Anand Raghunathan, Silicon Valley Professor in ECE, is the Purdue principal investigator and associate director. Purdue co-PIs are Kaushik Roy, the Edward G. Tiedemann Jr. Distinguished Professor in ECE; Vijay Raghunathan, ECE professor and director of semiconductor education; and Sumeet Gupta, ECE associate professor.

CoCoSys's vision is to enable seamless human-AI collaboration. The next wave of AI will impact everyday lives through collaborative intelligent systems such as digital humans and collaborative robots. These systems will drive unprecedented levels of automation, amplify human capabilities and fundamentally reshape the nature of work, personal life, and the human experience itself. CoCoSys researchers will enable human-AI systems through synergistic advances in neuro-symbolic-probabilistic algorithms, technology-driven hardware motifs, algorithm-hardware co-design and collective and collaborative intelligence.

In the Center on Cognitive Multispectral Sensors (CogniSense), Vijay Raghunathan is the Purdue PI and leader of one of the center's research themes, and Stanley Chan, ECE associate professor, is the Purdue co-PI.

CogniSense addresses the demand for high-quality unobstructed perception for the safe operation of emerging autonomous systems. Current sensing technologies generate unmanageable data volumes and consume too much power. The center's vision is to develop cognitive multispectral sensors that directly generate trustworthy insight from wideband multimodal analog signals. By designing sensors that dynamically adapt to "what is being sensed" and "how sensed signals are processed" according to real-time changes in the environment, CogniSense research is projected to dramatically reduce the volume of data produced by these sensors.

Research Excellence

Purdue research in semiconductors spans the "full stack" from materials and devices, to circuits, systems, and architecture.

Advanced Packaging and Heterogeneous Integration

Co-directed by Professors Handwerker and Subbarayan

Purdue is home to one of the nation's leading programs in advanced packaging and heterogeneous integration. Purdue co-leads the Semiconductor Research Corporation's Center for Heterogeneous Integration Research in Packaging (SRC CHIRP), the only advanced packaging center in the SRC portfolio. In addition, Purdue leads the SRC n-CORE NEW LIMITS: NEW materials for LogIc, Memory and InTerconnectS Center, co-funded by SRC members and NIST to develop synthesis, integration, and evaluation schemes for new BEOL materials for unique logic, memory, and interconnect applications to enable novel computing and storage paradigms beyond the capabilities of conventional CMOS. Complementing the above two SRC centers is the Cooling Technologies Research Center (CTRC), a graduated National Science Foundation Industry/University Cooperative Research Center (NSF/IUCRC), that has conducted leading-edge research on the thermal management of electronics for nearly 25 years. The Purdue team is addressing a critical research gap—the need to enable quick-turn, top-down packaged system development is an ability to automatically convert design intent into packaging strategy, materials selection, appropriate thermal solutions, and package circuit layout.

With a total of 24 faculty in advanced packaging across Purdue's College of Engineering, the Purdue team is focused on developing game-changing technologies such as electrical-thermal-mechanical deep co-design tools and techniques to translate design intent into automated package circuit layout. Specific research activities include Machine Learning (ML) assisted computational models that match multiphysics behavior of packages accurately, low power interconnects, advanced power-delivery solutions, innovative thermal solutions for die stack as well as package-level cooling, and advanced x-ray metrologies that enable real-time defect metrology, while also meeting the reliability and manufacturing yield goals so necessary for translating R&D to technology innovation. The goal of Purdue research is to enable a 50 times reduction in system realization time from architectural design to packaging.

Novel Approaches to Information Processing: Cognitive Computing

The boundary between memory and processing that was drawn clearly in the early days of computing by von Neumann still defines virtually all modern computing platforms, but the gap between processor and memory speeds has grown to create the daunting "memory wall" that threatens to stymy further progress in computing system performance. Further, the energy cost of moving data between DRAM and processors in the roughly 100 million computer servers in the world exceeds the output of over two Hoover Dams! After decades of progress in computing systems, we must revisit the von Neumann paradigm. Professors Roy and Raghunathan lead research on new approaches to information processing in C-BRIC, the $36M SRC/DARPA Center for Brain-inspired Computing and in the Institute for Cognitive Computing. The goal is to deliver key advances in cognitive computing to enable a new generation of autonomous intelligent systems.

Research Excellence *(cont'd)*

Cognitive computing brings together leading researchers from the fields of machine learning, computational neuroscience, theoretical computer science, neuromorphic hardware, distributed computing, and robotics and autonomous systems. Artificial Intelligence (AI) Hardware, another area of particular strength at Purdue, is also within the scope of the SRC/DARPA Center for Brain-inspired Computing. Eight faculty members from the School of ECE, with an ongoing search targeting two new hires, contribute to this effort. A major part of C-BRIC is focused on Compute-in-Memory (CiM) for efficient AI and data analytics. Computing-in-Memory (CiM) fundamentally blurs the distinction between processing and memory by bringing them closer, and in the extreme embedding processing capabilities within memory arrays. Besides radically improving the performance and energy efficiency of computing systems, CiM has the potential to enable entirely new categories of products and markets. Purdue researchers have pioneered several advances in the design of CiM systems and demonstrated them through tape outs of chips. A few of the recent tape outs include a 35.5 – 127.2 TOPS/W dynamic sparsity-aware reconfigurable-precision Compute-in-Memory SRAM macro for machine learning and a 65nm digital Compute-in-Memory Macro with fused weights and membrane potential for spike-based sequential learning tasks.

Atomic-Scale Engineering of Semiconductor Materials and Devices

Under the leadership of Professor Ye, Purdue faculty are actively engaged in the exploration of novel electronic materials and devices for post-Moore era semiconductor technologies. One of the utilized technologies is called atomic layer deposition (ALD). ALD is a thin-film deposition technique with atomic-scale controllable accuracy based on the sequential use of a self-limiting chemical process; it is a subclass of chemical vapor deposition. ALD became an enabling technology for the continuation of Moore's law by integrating high-k dielectrics in Si CMOS processes. ALD is a key process in fabricating semiconductor devices in particular as the dimension of state-of-the-art device technology is approaching single-digit nanometer length scales.

In the past decades, we have been working actively on ALD dielectrics and their integration on traditional and novel semiconducting channel materials including Si, Ge, III-V compound semiconductors, 2D materials, and oxide semiconductors. Beyond high-k and higher-k dielectrics, we also have explored ALD-grown ferroelectrics such as HfZrO2 for emerging logic and memory applications (IEDM 2021). More recently, we pioneered the use of the ALD technique to form atomically thin oxide semiconductor channels with remarkable performance including unprecedented ultra-high drain currents and transconductances among all field-effect transistors based on any semiconductor materials (Nature Electronics 2022). ALD interlayers can also be used a phonon spectrum match buffer to enhance the thermal dissipation and electrical-thermal co-design of atomic-scale electronic devices.

Beyond graphene and transition metal dichalcogenides (TMDs) 2D materials research, Purdue faculty pioneered phosphorene (ACS Nano 2014) and tellurene (Nature Electronics 2018), two special elemental van der Waals 2D monolayers of phosphorus and tellurium with thickness less than one nanometer. We systematically studied their electrical, optical, thermal, and mechanical properties and their applications for electronic devices. More interestingly, we are able to form a single atomic chain of tellurium atoms towards the smallest semiconductor channel (Nature Electronics 2020).

These efforts are enabled by the Birck Nanotechnology Center, which is a state-of-the-art facility that allows atomic-scale nanomaterial synthesis and prototype atomic-scale fabrication and characterization.

Novel Approaches to Information Processing: Probalistic Spin Logic

Probabilistic Spin Logic (PSL) is a novel approach for information processing that is being explored by a team led by Professors Datta, Chen, and Appenzeller. The majority of today's digital circuitry is based on building blocks called bits that are deterministically 0 or 1. At the other end of the spectrum are quantum computers consisting of qubits which occupy some superposition of 0 and 1. The probabilistic-bit occupies a niche between these extremes, sharing qualities with both the classical-bit and the quantum-bit. The p-bit fluctuates probabilistically between 0 and 1, and can be pinned to one or the other state based on the magnitude and sign of its input. For a popular description see IEEE Spectrum at https://ieeexplore.ieee.org/abstract/document/9393992.

Just as a bit is only useful when in conjunction with other bits, p-bits can be correlated to form p-circuits. These circuits can be programmed to tackle a variety of problems that are often targeted by quantum computing, such as optimization, inferencing, and data encryption and decryption—without, however, the need for ultra-low temperatures. It is in the variety of applications, and the classical nature of the p-bit, that this building block comes to life, providing orders of magnitude improvement in performance (see Applied Physics Letters at https://aip.scitation.org/doi/full/10.1063/5.0067927) over standard CPU and GPU implementations.

To date the Purdue team has published many other breakthroughs (for an overview see https://ieeexplore.ieee.org/abstract/document/8995804), most notably an experimental demonstration of optimization and invertible logic using unstable magnetic tunneling junctions (MTJs), see Nature (https://www.nature.com/articles/s41586-019-1557-9), and the feasibility of MTJs to demonstrate that complex circuit operations are achievable in realistic hardware systems. This is particularly exciting because it demonstrates the feasibility of fabricating compact energy-efficient hardware p-bits by modifying existing magnetic random access memory (MRAM) technology.

For more information, see: https://www.purdue.edu/p-bit/.
To learn about a company commercializing this technology, see: https://ludwigcomputing.com/.

Research Excellence *(cont'd)*

Emerging Logic, Memory, and Interconnect Technologies

Purdue Professors Alam, Appenzeller, Chen, Janes, and Ye are actively engaged in the exploration of emerging logic, memory, and interconnect technologies. Purdue's leadership is apparent from the support that these faculty receive from the Semiconductor Research Corporation (SRC) through center-level activities such as the nCORE NEW LIMITS Center (directed by Professor Chen) and JUMP, where Purdue PIs are involved in the ASCENT Center. In particular, these faculty have focused on experimental demonstrations of the above technologies based on novel materials including low-dimensional materials and ferroelectrics.

Professor Ye has been at the forefront of exploring novel materials for ferroelectric memory applications, and oxide-based channel materials such as In2O3 for back-end-of-line (BEOL) in-memory computing that requires transistors with ultra-low standby power specs and high on-current capabilities. Professor Ye has worked in strong collaboration with Professor Alam, who focuses on the reliability physics of these unexplored novel active device elements.

Professors Chen and Appenzeller have experimentally demonstrated that novel low-dimensional materials such as transition metal dichalcogenides (TMDs) with body thickness less than one nanometer can be utilized as channel materials in ultra-high performance transistors and offer performance beyond what silicon technologies can offer. Their work highlights the excellent scalability of devices from TMDs for the next generations of logic computing units.

https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=9372049

The same sub-1nm thickness also proved highly promising for the use of TMDs as diffusion barriers in future back-end-of-line (BEOL) interconnect technologies.

https://aip.scitation.org/doi/10.1063/5.0013737

Professors Chen and Appenzeller also observed that MoTe2 (a member of the TMD family) based memories give rise to a novel type of phase change switching that is controlled by electric fields. This is a low-power, fast switching memory that combines the characteristics of resistive random access memories (RRAM) and phase change memories (PCM).

https://www.nature.com/articles/s41563-018-0234-y

These efforts on emerging technologies are enabled by the Birck Nanotechnology Center, which is a state-of-the-art facility that allows prototype fabrication and characterization at scale.

Reliability of Semiconductor Logic and Memory Devices

Under the leadership of Professor Alam, Purdue is well-known for fundamental work on the reliability physics of semiconductor logic and memory devices, both for application-specific consumer electronics and radiation-hardened secure electronics for defense applications. A variety of test equipment available at the Birck Center would support the development of new performance/reliability characterization techniques for DRAM and Flash memories.

It is well known that bit errors (and "repeated-read" security failures) increase significantly as DRAM transistors are scaled below 28-32 nm node because the stored charge at the capacitor node and the leakage through the access transistor are sensitive to transistor scaling. Radiation- induced charge loss and SILC-related gate leakage are concerns that must be addressed. Similarly, next-generation 3D NAND Flash memories will continue to grapple with read-margin, retention, and endurance issues arising from: (a) the threshold-voltage variation due to ambient temperature-sensitivity of polysilicon channel mobility, (b) threshold-voltage fluctuation due to trapping/de-trapping in the tunnel oxides, and (c) the reduced channel cross-section and enhanced field making the bottom cells susceptible to correlated HCI, TDDB, and radiation damages. There is an opportunity to develop a more efficient ECC because the bit-flips in 3D NAND Flash are likely to be correlated. Further, for the Compute-in-Memory (CiM) applications involving both logic and memory transistors, classical ECC may not be relevant.

In short, Purdue can support the development of new characterization techniques and physics-based reliability models for HCI, SILC, TDDB, and radiation-related reliability issues of DRAM and Flash memories. These reliability models will be informed by a deep understanding of the cross-layer design considerations, including those arising from heterogeneous integration (HI) that defines the thermal and stress-related cross-talk among various components.

Research Excellence *(cont'd)*

Sustainability of Electronic Ecosystems

Sustainability is a core value at Purdue, as evidenced not only in green buildings and clean energy, but also in creating technologies that make the world a better place. Under the leadership of Professor Handwerker, Purdue is committed to the "Double Bottom Line" to care for people and the planet through the development of new technologies.

Purdue has a strong tradition in quantifying the economic, environmental, and societal impacts of the decisions made in early-stage R&D on the ultimate impacts in the realized products and their global supply chains. We welcome collaborations in coupling sustainability R&D at Purdue with the supply chains, technology developers, and decision-makers of companies. Three examples of recent collaborations that could serve as models are:

1. DOE Critical Materials Hub in which Purdue provides quantification of both commercialization potential and environmental impact of technologies being developed by researchers from four DOE Labs, ten companies, and eight universities;
2. iNEMI Project on Value Recovery from End-of-Life Electronics, co-led by Purdue, in which Seagate, Google, Microsoft, Cisco, and others demonstrated nine circular economy technologies for remanufacturing, reuse, and recovery of rare earth magnets in hard drives; and
3. NSF graduate education and training program on Design for Globally Sustainable Electronics in which DBL is a central tenet, with a customizable curriculum based on partner company needs. For the latter, these courses are part of the new MS in Semiconductors and Microelectronics at Purdue and the undergraduate certificate in Semiconductors.

Finally, Purdue not only has deep expertise in R&D but also in workforce development to address issues of local, regional, and global concern, including but not limited to clean energy, smart grids, system design and operation for Net Zero, and developing leadership for creating and operating sustainable systems.

High Frequency Electronics

Purdue University is a pacesetter in High-frequency Electronics, also referred to as Radio Frequency (RF) Engineering. There are more than 12 faculty members and 100 PhD students, postdocs, and research scientists that lead major centers/projects spanning the sub-GHz to the millimeter-wave space. In addition to Birck Nanotechnology Center facilities, RF researchers utilize more than 10,000 square feet in the Elmore Family School of Electrical and Computer Engineering to design and characterize devices up to 220 GHz. Recent breakthroughs include:

- PiezoMEMS resonant actuators from 100 MHz to 50 GHz for LIDAR, microwave-to-optical quantum coherent converters, and mechanical control of color center defects in Diamond and Silicon Carbide (Bhave).
- Low-noise RF front-ends, online adaptive calibration schemes, and massive sensor data processing. The team demonstrated the first electromagnetic tracking system with an unprecedented level of accuracy and a non-invasive current monitoring system with world record SNR (Jung).
- Multi-functional RF filter architectures in the 1-100 GHz range. Examples include supercavity resonators, automatically tunable filters, and all-silicon tunable filters. Moreover, we have demonstrated the first switchable on-chip silicon plasma devices and antennas such as K-band silicon monopoles, plasma-switch impedance tuners, and DC-110 GHz plasma silicon switches (Peroulis).
- Adaptive sub-6 GHz and non-radiative Covert Communication (kHz-GHz) Integrated Circuits and Systems. We demonstrated the first physically secure Electro-Quasistatic Communication on Human Body and other conductors with 100x lower energy than Bluetooth. EM-Security which includes first ultra-resilient circuit-level EM-Side Channel Protection, RF-PUF, RF-PSF and EM-emanation detection. Also, we work on EM based Biosensors and application of RF/EM Sensing and Communication in Internet of Bodies (Sen).
- Photonically-enabled RF arbitrary waveform generation, including application to high range resolution W-band radar, RF photonic down-converters for use in sampling broadband electronic signals, interferometric direction-finding and signal characterization architectures for wideband sensing, and optical frequency combs for coherent links between RF and optical frequencies (Weiner, McKinney).
- Fast and efficient math/physics-based modeling of highly complex RF structures resulting in greatly reduced computer time (Chew).

https://tinyurl.com/WangHallLabs

Faculty

Faculty Name, Title, and Department	RESEARCH AREAS							
	Heterogeneous Integration and Advanced Packing	High-Frequency Electronics	Integrated Circuits and Systems Design	MEMS and Photonics	New Devices, Materials, and Fabrication	Sensors and Thermal Imaging	Simulation and Modeling	Sustainability and Life Cycle Analysis
 **Hadiseh Alaeian** Assistant Professor, Electrical and Computer Engineering and Physics and Astronomy					●			
 **Muhammad Ashraf Alam** Jai N. Gupta Professor, Elmore Family School of Electrical and Computer Engineering					●			
 **Joerg Appenzeller** Scientific and Director of Nanoelectronics and Barry M. and Patricia L. Epstein Professor, Elmore Family School of Electrical and Computer Engineering					●			
 **Santokh Badesha** Distinguished Professor of Electrical and Computer Engineering					●			
 **Shubhra Bansal** Associate Professor, School of Mechanical Engineering					●			
 **Thomas Beechem** Associate Professor, School of Mechanical Engineering					●			
 **Peter Bermel** Director of SCALE; Associate Director of Graduate Admissions; and Elmore Associate Professor, Elmore Family School of Electrical and Computer Engineering					●	●		●
 **Sunil Bhave** Associate Director of Operations, Birck Nanotechnology Center and Professor, Elmore Family School of Electrical and Computer Engineering		●	●	●	●			
 **John Blendell** Professor, School of Materials Engineering	●							
 **Alexandra (Sasha) Boltasseva** Ron and Dotty Garvin Tonjes Distinguished Professor, Elmore Family School of Electrical and Computer Engineering					●			

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	Heterogeneous Integration and Advanced Packing	High-Frequency Electronics	Integrated Circuits and Systems Design	MEMS and Photonics	New Devices, Materials, and Fabrication	Sensors and Thermal Imaging	Simulation and Modeling	Sustainability and Life Cycle Analysis
 **Bryan Boudouris** Associate Vice President for Research and Strategic Interdisciplinary Research and Professor, Chemical Engineering					●			
 **Michael Capano** Professor, Electrical and Computer Engineering					●			
 **Nikhilesh Chawla** Ransburg Professor, School of Materials Engineering	●							
 **Yong Chen** Karl Lark-Horovitz Professor, Physics and Astronomy					●			
 **Zhihong Chen** Mary Jo and Robert L. Kirk Director of Birck Nanotechnology Center and Professor, Elmore Family School of Electrical and Computer Engineering					●			
 **Weng Chew** Distinguished Professor, Electrical and Computer Engineering		●						
 **Supriyo Datta** Thomas Duncan Distinguished Professor, Elmore Family School of Electrical and Computer Engineering					●			
 **Chelsea Davis** Assistant Professor, School of Materials Engineering	●							
 **Daniel Elliott** Professor, Electrical and Computer Engineering and Physics					●			
 **Edwin García** Professor, School of Materials Engineering							●	

Faculty *(cont'd)*

Faculty Name, Title, and Department	RESEARCH AREAS							
	Heterogeneous Integration and Advanced Packing	High-Frequency Electronics	Integrated Circuits and Systems Design	MEMS and Photonics	New Devices, Materials, and Fabrication	Sensors and Thermal Imaging	Simulation and Modeling	Sustainability and Life Cycle Analysis
 **James Gibert** Associate Professor, Mechanical Engineering	●							
 **Luis Gomez** Assistant Professor, Electrical and Computer Engineering		●						
 **Ananth Grama** Samuel D. Conte Professor, Computer Science								●
 **Jeffery Gray** Associate Professor, Electrical and Computer Engineering					●			
 **Sumeet Gupta** Elmore Associate Professor, Elmore Family School of Electrical and Computer Engineering			●					
 **Carol Handwerker** Reinhardt Schuhmann, Jr. Distinguished Professor in the School of Materials Engineering	●							●
 **Mahdi Hosseini** Assistant Professor, Elmore Family School of Electrical and Computer Engineering				●	●			
 **John Howarter** Associate Professor, School of Materials Engineering and Environmental and Ecological Engineering	●							
 **Inez Hua** Professor, School of Civil Engineering and Environmental and Ecological Engineering								●
 **Muhammad Hussain** Professor, Elmore Family School of Electrical and Computer Engineering					●			

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	Heterogeneous Integration and Advanced Packing	High-Frequency Electronics	Integrated Circuits and Systems Design	MEMS and Photonics	New Devices, Materials, and Fabrication	Sensors and Thermal Imaging	Simulation and Modeling	Sustainability and Life Cycle Analysis
 **Zubin Jacob** Elmore Associate Professor, Electrical and Computer Engineering					●			
 **David Janes** Professor, Elmore Family School of Electrical and Computer Engineering					●			
 **Dan Jiao** Synopsys Professor, Elmore Family School of Electrical and Computer Engineering		●					●	
 **Byunghoo Jung** Professor, Elmore Family School of Electrical and Computer Engineering		●	●					
 **Alexander Kildishev** Professor, Electrical and Computer Engineering		●						
 **Gerhard Klimeck** Director of the Network for Computational Nanotechnology; Reilly Director of the Center for Predictive Materials and Devices; and Elmore Professor, Elmore Family School of Electrical and Computer Engineering					●	●		
 **Cheng-Kok Koh** Professor, Electrical and Computer Engineering			●					
 **Marisol Koslowski** Assistant Head for Engagement and Partnerships and Professor, School of Mechanical Engineering							●	
 **Tillmann Kubis** Katherine Ngai Pesic and Silvaco Associate Professor, Elmore Family School of Electrical and Computer Engineering					●		●	
 **Haitong Li** Assistant Professor, Elmore Family School of Electrical and Computer Engineering			●		●			

Faculty *(cont'd)*

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	Heterogeneous Integration and Advanced Packing	High-Frequency Electronics	Integrated Circuits and Systems Design	MEMS and Photonics	New Devices, Materials, and Fabrication	Sensors and Thermal Imaging	Simulation and Modeling	Sustainability and Life Cycle Analysis
 **Yung-Hsiang Lu** Professor, Electrical and Computer Engineering			●					
 **Mark Lundstrom** Chief Semiconductor Officer and Don and Carol Scifres Distinguished Professor, Elmore Family School of Electrical and Computer Engineering					●			
 **Mike Manfra** Scientific Director, Microsoft Quantum Lab Purdue; Bill and Dee O'Brien Distinguished Professor, Physics and Astronomy; and Professor, Elmore Family School of Electrical and Computer Engineering and School of Materials Engineering					●			
 **Amy Marconnet** Associate Professor, School of Mechanical Engineering	●							
 **Jason McKinney** Associate Professor, Electrical and Computer Engineering		●						
 **Michael Melloch** Professor, Electrical and Computer Engineering					●			
 **Saeed Mohammadi** Professor, Elmore Family School of Electrical and Computer Engineering		●	●		●			
 **Issam Mudawar** Betty Ruth and Milton B. Hollander Family Professor, School of Mechanical Engineering					●			
 **Evgenii Narimanov** Elmore Professor, Electrical and Computer Engineering					●			
 **Liang Pan** Associate Professor, School of Mechanical Engineering	●							

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	Heterogeneous Integration and Advanced Packing	High-Frequency Electronics	Integrated Circuits and Systems Design	MEMS and Photonics	New Devices, Materials, and Fabrication	Sensors and Thermal Imaging	Simulation and Modeling	Sustainability and Life Cycle Analysis
 **Dimitrios Peroulis** Senior Vice President for Purdue University Online and Reilly Professor, Elmore Family School of Electrical and Computer Engineering		●	●	●	●			
 **Irith Pomeranz** Cadence Professor, Electrical and Computer Engineering			●					
 **Minghao Qi** Professor, Elmore Family School of Electrical and Computer Engineering				●	●			
 **Anand Raghunathan** Silicon Valley Professor, Elmore Family School of Electrical and Computer Engineering			●					
 **Vijay Raghunathan** Director of Semiconductor Education and Professor, Elmore Family School of Electrical and Computer Engineering			●					
 **Rahim Rahimi** Assistant Professor, School of Materials Engineering						●		
 **Thomas Roth** Assistant Professor, Electrical and Computer Engineering		●						
 **Kaushik Roy** Director of Center for Brain-Inspired Computing, a DARPA/SRC JUMP Center and Edward G. Tiedemann Jr. Distinguished Professor, Elmore Family School of Electrical and Computer Engineering			●		●			
 **Xiulin Ruan** Director of Graduate Recruitment and Admissions and Professor, Mechanical Engineering							●	
 **Shreyas Sen** Elmore Associate Professor, Elmore Family School of Electrical and Computer Engineering and Biomedical Engineering		●	●					

Faculty *(cont'd)*

Faculty Name, Title, and Department	RESEARCH AREAS							
	Heterogeneous Integration and Advanced Packing	High-Frequency Electronics	Integrated Circuits and Systems Design	MEMS and Photonics	New Devices, Materials, and Fabrication	Sensors and Thermal Imaging	Simulation and Modeling	Sustainability and Life Cycle Analysis
 **Ali Shakouri** Professor, Elmore Family School of Electrical and Computer Engineering					●	●		
 **Vladimir Shalaev** Bob and Anne Burnett Distinguished Professor, Electrical and Computer Engineering					●			
 **Ganesh Subbarayan** Co-director, SRC Center for Heterogeneous Integration Research in Packaging *(CHIRP)* and James G. Dwyer Professor of Mechanical Engineering	●						●	●
 **John Sutherland** Fehsenfeld Family Head, School of Environmental and Ecological Engineering								●
 **Pramey Upadhyaya** Assistant Professor, Elmore Family School of Electrical and Computer Engineering					●			
 **Haiyan Wang** Basil S. Turner Professor, Elmore Family School of Electrical and Computer Engineering and School of Materials Engineering					●			
 **Kevin Webb** Professor, Elmore Family School of Electrical and Computer Engineering					●			
 **Tiwei Wei** Assistant Professor, School of Mechanical Engineering	●							
 **Dana Weinstein** Dean of Graduate Education, College of Engineering and Professor, Elmore Family School of Electrical and Computer Engineering		●	●	●	●			
 **Justin Weibel** Associate Professor, School of Mechanical Engineering	●							

Faculty Name, Title, and Department	RESEARCH AREAS							
	Heterogeneous Integration and Advanced Packing	High-Frequency Electronics	Integrated Circuits and Systems Design	MEMS and Photonics	New Devices, Materials, and Fabrication	Sensors and Thermal Imaging	Simulation and Modeling	Sustainability and Life Cycle Analysis
 **Andrew Weiner** Scifres Family Distinguished Professor, Electrical and Computer Engineering		●			●			
 **Dongyan Xu** Samuel D. Conte Professor of Computer Science; Director of CERIAS; and Assistant Professor, Purdue Polytechnic Institute								●
 **Xianfan Xu** James J. and Carol L. Shuttleworth Professor, School of Mechanical Engineering, Professor, Elmore Family School Electrical and Computer Engineering (by courtesy)				●	●			
 **Peide (Peter) Ye** Richard J. and Mary Jo Schwartz Professor, Elmore Family School of Electrical and Computer Engineering					●			
 **Xinghang Zhang** Professor, School of Materials Engineering	●							
 **Fu Zhao** Professor, School of Mechanical Engineering and Environmental and Ecological Engineering								●

PURDUE UNIVERSITY

Semiconductors@Purdue in the News

Washington Post

October 23, 2022

Economic Future of U.S. Depends on Making Engineering Cool

"By rapidly expanding chip education, Purdue is aiming to graduate 1,000 semiconductor engineers annually as soon as possible. [...] Purdue is rolling out new courses and labs for UGs, a new master's program and a push to place students in chip internships..."

The New York Times

January 1, 2023

U.S. Pours Money Into Chips, but Even Soaring Spending Has Limits

"Purdue University, which built a new semiconductor laboratory, has set a goal of graduating 1,000 engineers each year..."

THE WALL STREET JOURNAL.

January 14, 2023

Chips are the New Oil and America is Spending Billions to Safeguard its Supply

"Mung Chiang, president of Purdue University, [...] said Purdue has created a dedicated semiconductor program it hopes will award more than 1,000 certificates and degrees annually by 2030 in person and online."

August 5, 2023

The Economist

America is Building Chip Factories. Now to Find the Workers

"Leading the charge is Purdue University in Indiana, which last year launched a semiconductor degree programme for both undergraduates and graduates. The explicit aim of Purdue's 'lab-to-fab' model is to collaborate more closely with companies."

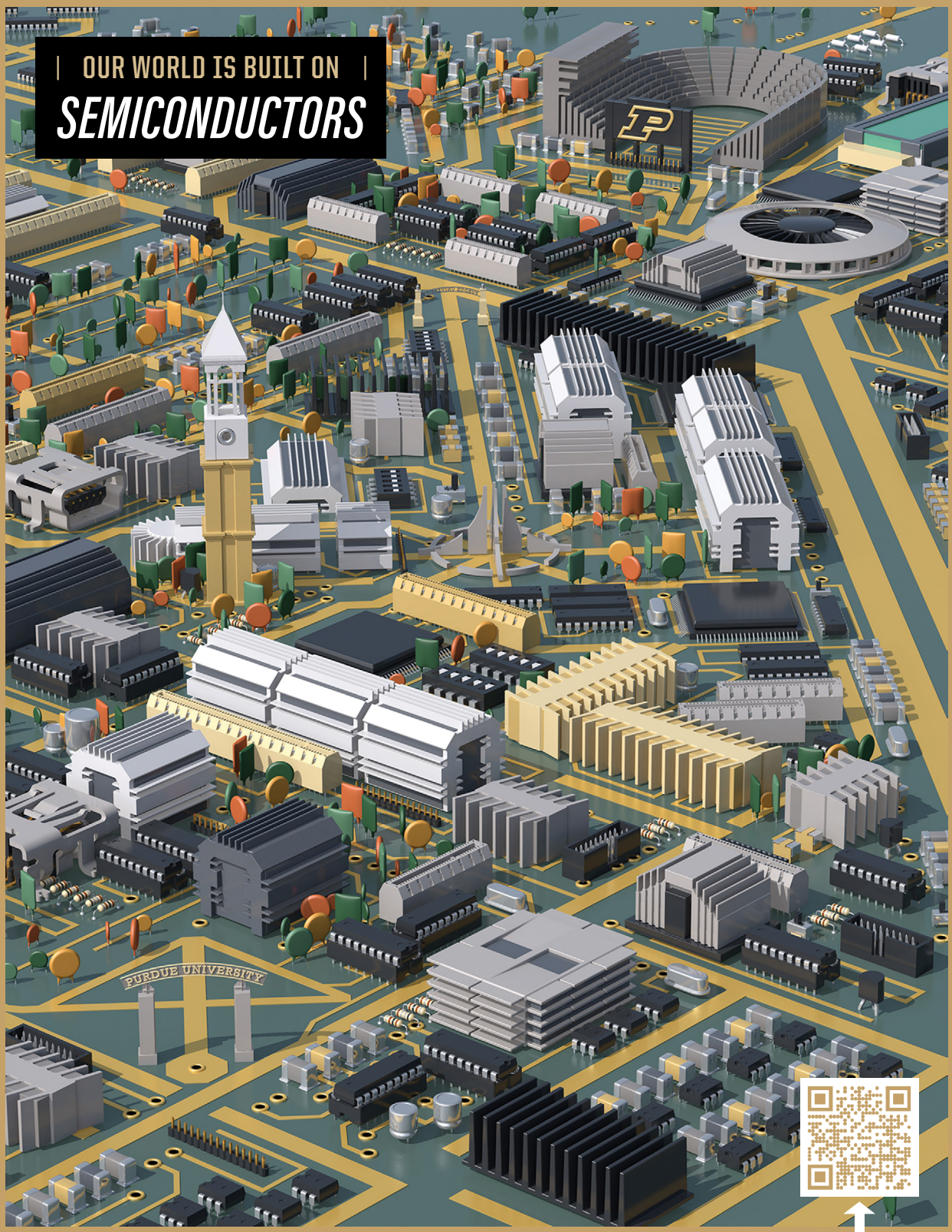
The New York Times

August 6, 2023

Indiana Tests if the Heartland can Transform into a Chip Hub

"Some of the work paid off. When Indiana beat out four other states for SkyWater's $1.8 billion chip facility, the company said it was impressed by the coordination between state leaders and Purdue's new president, Mung Chiang, who launched the nation's first semiconductor degree programs to nurture workers for chip makers."

Purdue University = Heart of Silicon Crossroads



CHIP rendering of the Purdue Campus | Take a quick tour!

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