Swagath Venkataramani

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465, Northwestern Avenue ◇ West Lafayette, IN 47907

EDUCATION

Purdue University August 2010 - May 2016 (*Expected*)
Ph.D., Electrical and Computer Engineering *West Lafayette,IN*
Integrated Systems Laboratory
Major Advisor: Prof. Anand Raghunathan
Overall GPA: 4.0/4.0 (A+ in 11 out of 12 courses)
Awarded **Intel PhD Fellowship** and **Bilsland Dissertation Fellowship**
Best paper award nominations at DAC 2016 (result pending) and ISLPED 2014

College of Engineering Guindy, Anna University August 2006 - June 2010
B.E., Electrical and Electronics Engineering *Chennai, India*
Overall GPA: 9.73/10.0
University Gold Medallist

WORK EXPERIENCE

Parallel Computing Labs, Intel Labs August 2015 - February 2016
Visiting Research Scientist *Bangalore, India*

I was the leading contributor in a research project: *Scalable Compute Architecture for Deep Learning*.

- Designed *DeepSCALE*, a scalable, dense, compute node architecture for training and evaluating deep-learning networks with heterogenous processing cores and chips, in-memory compute and synchronization, and a 3-tiered interconnect architecture.
- DeepSCALE can deliver 750 TFLOPS (peak) under 1.5 KW power, and achieve an order of magnitude improvement in training performance over state-of-the-art deep learning implementations.

Sensing and Energy Research Group, Microsoft Research June 2014 - August 2014
Research Intern *Redmond, WA*

I worked on two projects that investigated techniques to design energy-efficient hardware and software implementations of machine learning algorithms on IoT/portable devices.

- Designed SAPPHIRE, an always-ON system for IoT devices, which achieves 2× battery life improvement by reducing data transmitted when executing computer-vision applications.
- Developed Scalable-effort classifiers, a machine learning classifier framework which improves energy efficiency by intrinsically modulating classifier effort based on input difficulty.
- The internship resulted in 2 conference publications, 5 patent applications (undisclosed) and 1 book chapter.

Exascale Computing Research, Intel Corporation June 2013 - August 2013
Graduate Technical Intern *Hillsboro, OR*

I was part of a Department of Energy (DoE) sponsored exascale research initiative at Intel. I worked with the processor RTL design and on-chip network design teams.

- Developed a hierarchical framework to model both on-chip and off-chip network costs in the exascale functional simulator in a manner scalable to thousands of cores.
- Involved in front-end design tasks such as RTL design and verification of the exascale processor core.

I received *Intel Employee Recognition Award* for my performance and contributions.

TECHNICAL STRENGTHS

High-level Programming Languages	C, C++, C#, Perl, Python
RTL Design Languages	Verilog, VHDL
EDA Tools	Synopsys Design Compiler, Prime Time
FPGA Prototyping	ModelSim, Synopsys VCS, Altera SoC design flow: Quartus, SoPC builder, NIOS2-IDE, Xilinx Vivado
HLS Tools	Mentor Graphics Catapult
Transistor level design and analysis	Nanosim, HSPICE
Layout	Cadence Virtuoso
Open Source	SIS (logic synthesis), SimpleScalar, Simics-GEMS (Cycle-accurate simulators)

RESEARCH AND PUBLICATIONS

Interests: Energy-efficient machine learning on mobile/portable devices, high performance clusters, and cloud; Deep learning and neuromorphic computing; Parallel and heterogenous Architectures; System-on-chip design

Thesis: "Approximate Computing: Computing Efficiently with Good-enough Results"

The gap created by diminishing benefits from technology scaling on the one hand, and the continued increase in computing demand from emerging workloads on the other, presents a grand challenge to designers of computing platforms. My dissertation explores approximate computing as a promising direction to address this conundrum. Approximate computing exploits a fundamental shift in the nature of computing workloads. Most emerging workloads, such as recognition, data mining and analytics, search, computer vision, inference, etc., share the characteristic that they do not produce a unique, precise numerical end result; rather, a range of results are acceptable. Thus, they are endowed with a forgiving nature, or an ability to produce acceptable results even in the presence of approximations to their underlying computations. My dissertation aims to lay the foundations for this emerging field by proposing conceptual underpinnings, systematic approaches, and techniques to apply approximate computing at various layers of the computing stack. In addition to my dissertation research, I have also explored spintronic computing systems and the design of programmable accelerators for next-generation computing workloads.

Peer-reviewed Conferences:

C23. N. Gala, **S. Venkataramani**, V. Kamakoti and A. Raghunathan, "STOCK: Stochastic Checkers for Faults in Approximate Applications", in Proc. IEEE/ACM International Symposium on Lower Power Electronics and Design (ISLPED), August 2016 (*under review*).

C22. Y. Kim, **S. Venkataramani**, K. Roy and A. Raghunathan, "Designing Approximate Circuits using Clock Overgating", in Proc. IEEE/ACM Design Automation Conference (DAC), June 2016 (**Nominated for Best Paper Award**).

C21. S. Sarwar, **S. Venkataramani**, A. Raghunathan and K. Roy, "Multiplier-less Artificial Neurons Exploiting Error Resiliency for Energy-Efficient Neural Computing", in Proc. Design, Automation and Test at Europe (DATE), March 2016.

C20. S. Jain, **S. Venkataramani**, and A. Raghunathan, "Approximation through Logic Isolation for the Design of Quality Configurable Circuits", in Proc. Design, Automation and Test at Europe (DATE), March 2016.

C19. **S. Venkataramani**, K. Roy, and A. Raghunathan, "Efficient Embedded Learning for IoT Devices", in Proc. IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Jan 2016 (*Special Session: Design Challenges for Energy-Efficient IoT Edge Devices*).

C18. **S. Venkataramani**, S. Chakradhar, K. Roy and A. Raghunathan, "Approximate Computing and the Quest for Computing Efficiency", in Proc. IEEE/ACM Design Automation Conference (DAC), June 2015 (*Special Session: Dark Silicon: No way Out?*).

C17. **S. Venkataramani**, J. Liu, A. Raghunathan and M. Shoaib, "Scalable-effort Classifiers for Energy Efficient Machine Learning", in Proc. IEEE/ACM Design Automation Conference (DAC), June 2015.

C16. A. Ranjan, **S. Venkataramani**, X. Fong, K.Roy and A. Raghunathan, "Approximate Storage for Energy Efficient Spintronic Memories", in Proc. IEEE/ACM Design Automation Conference (DAC), June 2015.

C15. **S. Venkataramani**, V. Bahl, X.-S. Hua, J. Liu, J. Li, M. Phillipose, B. Priyantha and M. Shoaib, "Sapphire: An Always-on Context-aware Computer Vision System for Portable Devices", in Proc. Design, Automation and Test at Europe (DATE), March 2015.

C14. **S. Venkataramani**, S.Chakradhar, K. Roy and A. Raghunathan, "Computing Approximately, and Efficiently", in Proc. Design, Automation and Test at Europe (DATE), March 2015 (*Invited*).

C13. A. Raha, **S. Venkataramani**, V. Raghunathan, and A. Raghunathan, "Quality Configurable Reduce-and-Rank for Energy Efficient Approximate Computing", in Proc. Design, Automation and Test at Europe (DATE), March 2015.

C12. R. Venkatesan, **S. Venkataramani**, X. Fong, K. Roy and A. Raghunathan, "SPINTASTIC: Spin-based Energy-efficient Stochastic Logic", in Proc. IEEE/ACM Design, Automation and Test at Europe (DATE), March 2015.

C11. **S. Venkataramani**, S.Chakradhar, K. Roy and A. Raghunathan, "Approximate Computing for Efficient Information Processing", in Proc. IEEE Symposium on Embedded Systems For Real-time Media (ESTIMedia), Embedded Systems Week (ESWEEK), October 2014 (*Special Session: Emerging Trends for the Next-Generation Multimedia*).

C10. V.Kozhikkottu, **S. Venkataramani**, S. Dey, A. Raghunathan, "Variation tolerant design of a vector processor for Recognition, Mining and Synthesis", in Proc. IEEE/ACM International Symposium on Lower Power Electronics and Design (ISLPED), August 2014.

C9. **S. Venkataramani**, A. Ranjan, K. Roy and A. Raghunathan, "AxNN: Energy Efficient Neuromorphic Systems using Approximate Computing", in Proc. IEEE/ACM International Symposium on Lower Power Electronics and Design (ISLPED), August 2014 (**Nominated for Best Paper Award**).

C8. V. K. Chippa, **S. Venkataramani**, K. Roy and A. Raghunathan, "StoRM: A Stochastic Recognition and Mining Processor", in Proc. IEEE/ACM International Symposium on Lower Power Electronics and Design (ISLPED), August 2014.

C7. R. Venkatesan, S. Ramasubramanian, **S. Venkataramani**, K. Roy and A. Raghunathan "STAG: Spintronic-Tape Architecture for GPGPU Cache Hierarchies", in Proc. IEEE/ACM International Symposium on Computer Architecture (ISCA), June 2014.

C6. A. Ranjan, A. Raha, **S. Venkataramani**, K. Roy and A. Raghunathan, "ASLAN: Synthesis of Sequential Approximate Circuits", in Proc. IEEE/ACM Design, Automation and Test at Europe (DATE), March 2014.

C5. **S. Venkataramani**, V.K. Chippa, S. Chakradhar, K. Roy and A. Raghunathan, "Quality Programmable Vector Processors for Approximate Computing", in Proc. IEEE/ACM International Symposium on Microarchitecture (MICRO), December 2013.

C4. V.K. Chippa, **S. Venkataramani**, K. Roy and A. Raghunathan, "Approximate Computing: An Integrated Hardware Approach", in Proc. IEEE/ACM Asilomar Conference on Signals, Systems and Computers (ASILOMAR), Nov 2013.

C3. S. Ramasubramanian, **S. Venkataramani**, A. Paranthaman and A. Raghunathan "Re-timing for Energy Efficient Recovery based Designs", in Proc. IEEE/ACM Design Automation Conference (DAC), June 2013.

C2. **S. Venkataramani**, K.Roy and A. Raghunathan, "Substitute-and-Simplify: A Unified Design Paradigm for Approximate and Quality Configurable Circuits" , in Proc. IEEE/ACM Design, Automation and Test at Europe (DATE), March 2013.

C1. **S. Venkataramani**, A. Sabne, V.Kozhikkottu, K.Roy and A. Raghunathan, "SALSA: Systematic Logic Synthesis of Approximate Circuits", in Proc. IEEE/ACM Design Automation Conference (DAC), June 2012.

Book Chapters:

B1. M. Shoaib, **S. Venkataramani**, X.-S. Hua, J. Liu, and J. Li, "Exploiting On-device Image Classification for Energy Efficiency in Ambient-aware Systems", in Mobile and Cloud Visual Media Computing, Springer Publishers, 2015.

Conference Tutorials:

T1. **S. Venkataramani**, K. Roy, and A. Raghunathan, "Approximate Computing", Half-day tutorial, International Conference on VLSI Design, Jan 2016.

Journals:

J7. A. Raha, **S. Venkataramani**, V. Raghunathan and A. Raghunathan, "Energy-Efficient Reduce-and-Rank using Input-Adaptive Approximations", in IEEE Trans. on VLSI systems (TVLSI) (*under review*).

J6. P. Panda, A. Sengupta, **S. Venkataramani**, A. Raghunathan and K. Roy, "Object Detection using Semantic Decomposition for Energy-Efficient Neural Computing", in IEEE Trans. on VLSI systems (TVLSI) (*under review*).

J5. R. Venkatesan, **S. Venkataramani**, X. Fong, K. Roy and A. Raghunathan, "Energy Efficient Stochastic Computing with Spintronic Devices", in IEEE Trans. on Computers (TC) (*under review*).

J4. **S. Venkataramani**, S. Chakradhar, K. Roy and A. Raghunathan, "Approximate Hardware: Principles and Design Techniques", in IEEE Design and Test Magazine, 2016.

J3. J. Liu, **S. Venkataramani**, S. Venkatakrishnan, Y. Pan, C. Bouman and A. Raghunathan, "EMBIRA: Efficient Model Based Iterative 3D Reconstruction Accelerator", in IEEE Trans. on VLSI systems (TVLSI), 2016.

J2. Z. Pajouhi, **S. Venkataramani**, K. Yogendra, A. Raghunathan and K. Roy, "Exploring Spin-Transfer-Torque Devices for Logic Applications", in IEEE Trans. on computer-aided design of Integrated Circuits and Systems (TCAD), 2015.

J1. **S. Venkataramani**, V. Kozhikkottu, A. Sabne, K. Roy and A. Raghunathan, "Logic Synthesis of Approximate Circuits", in IEEE Trans. on computer-aided design of Integrated Circuits and Systems (TCAD), 2015.

Patents:

P7-8 **S.Venkataramani**, D. Das, A. Rajan, S. Banerjee, S. Avancha, A. Jagannathan, A. Durg, D. Nagaraj, B. Kaul, and A. Raghunathan, **2** invention disclosures (undisclosed) related to "Design of scalable compute architecture for deep learning networks" filed, Feb 2016 (*Asignee*: Intel Corporation).

P6 J. Liu, **S. Venkataramani**, S.Venkatakrishnan, C. Bouman, and A. Raghunathan, "Tomographic Reconstruction System", U.S patent application filed, Feb 2016 (*Asignee*: Purdue University, High Performance Imaging Inc.).

P1-5 **S.Venkataramani**, M. Shoaib, J. Liu, X.-S. Hua, J. Liu, J. Li, M. Phillipose, B. Priyantha, and V. Bahl, **5** U.S. patent applications (undisclosed) related to "Design of always-ON systems" and "Computationally efficient machine learning" filed, Jan 2015 (*Asignee*: Microsoft Corporation).

Invited Presentations:

I7. Invited Talk, "Addressing the Computing Efficiency Gap with Approximate Computing", in School of ECE, Georgia Institute of Technology, Atlanta GA, April 2015.

I6. Invited Speaker, "Approximate Computing for Energy-efficient Error-resilient Multimedia Systems", in IEEE/ACM Workshop on Variability Modeling and Characterization, International Conference on Computer Aided Design (ICCAD), November 2014.

I5. Invited Speaker, "Approximate Computing for Efficient Information Processing", in IEEE Symposium on Embedded Systems For Real-time Media (ESTIMedia), Embedded Systems Week (ESWEEK), October 2014.

I4. Invited Presentation, "Approximate Computing: Computing Efficiently with Good-enough Results", School of Computer Science and Engineering, University of Washington, Seattle WA, August 2014.

I3. Invited Expert, ISAT/DARPA Workshop on Accuracy Trade-offs across System Stack, Orlando FL, February 2014.

I2. Invited Attendee, Intel Labs Approximate Computing Workshop, Portland OR, August 2013.

I1. Invited Presentation, "Approximate (but Good-enough) Computing: Embracing Errors for Efficiency", Electrical Engineering Department, Indian Institute of Technology-Madras, Chennai, India, November 2012.

Research featured in the media:

- "Approximate computing' improves efficiency, saves energy", Purdue Newsroom
  http://www.purdue.edu/newsroom/releases/2013/Q4/approximate-computing-improves-efficiency,-saves-energy.html
- "Chip Saves Power by Fudging the Figures", MIT technology review
  http://www.technologyreview.com/news/522711/chip-saves-power-by-fudging-the-figures/
- "Approximation may reduce energy use of electronics", Physics Today
  http://scitation.aip.org/content/aip/magazine/physicstoday/news/news-picks/approximation-may-reduce-energy-use-of-electronics-a-news-pick-post
- "Approximate computers could do tasks not requiring exact answers", Space daily
  http://www.spacemart.com/reports/Approximate_computers_could_do_tasks_not_requiring_exact_answers_999.html
- Also featured on Slashdot, ACM Tech News headlines, NSF News from the field *etc.*

AWARDS AND RECOGNITIONS

- "Intel PhD Fellowship" (2014-15) in the category *Computing Leadership*, Intel Corporation; 1 of 9 PhD students throughout USA.
- "University Gold Medal" and 2 endowment awards for securing 1^{st} rank in Undergraduate at Anna University.
- "Bilsland Dissertation Fellowship" (2014-15), College of Engineering, Purdue Graduate School, Purdue University; awarded to the top 1 or 2 doctoral students in the department.
- "Best Paper Award Nomination (Result pending)" at IEEE/ACM Design Automation Conference (DAC) 2016.
- "Best Paper Award Nomination" at IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED) 2014.
- "2-year Graduate Teaching Assistantship" (2010-2012) awarded with PhD admission by the School of Electrical and Computer Engineering, Purdue Univerisity.
- "Summer Research Fellowship" (2009) awarded by Indian Institute of Technology - Madras.
- "Intel Employee Recognition Award" during summer internship at Intel Corporation.
- "Best Outgoing Student Award" (2009-10) and associated "Golden Jubilee Reunion" endowment at Anna University, Chennai.
- "The Kandasamy Alagarsamy Scholarship" and "Guindy Engineering-62 Trust Award" by the Alumni Association of Anna University.
- "Best Outgoing Student Award" and "Outstanding Student Award" in Secondary and Higher Secondary Schools.
- "Young Student Support Award" (now Richard A. Newton Young Student Fellowship) at IEEE/ACM Design Automation Conference (DAC), 2012.

ACADEMICS

Relevant Coursework @ Purdue:
System-on-Chip Design (695r), Advanced Computer Systems (666), Computer System Architecture (565), Programming Parallel Machines (563), Computer Design and Prototyping (437), Digital System Design Automation (595z), Advanced VLSI Design (695kr), Modelling and Optimization of High Performance Interconnects (670), Solid State Devices (606), MOS VLSI Design (559).

Hands-on Projects:

1. "Scalable Effort" Hardware Accelerator Design for Real Time Handwriting Recognition using Support Vector Machines (Verilog, C++).
2. A Programmable Stream-based Parallel Accelerator Architecture for RMS and Multimedia Applications (Verilog, C++).
3. RTL Design and FPGA implementation of an In-order, Pipelined and Split-Cached Dual-Core Processor (VHDL, Quartus).
4. Evaluation of Various Sequential Hardware Prefetching Mechanisms for Shared Memory Multiprocessors (Simics-GEMS - C++).
5. A survey of Adaptive Replacement Polices for Last Level Caches (C++).
6. pCNN: Parallel Convolutional Neural Network Implementations for Handwritten Digit Recognition (C++, Pthreads, MPI)
7. iCruze: An FPGA based Controller for Automobiles (Verilog).
8. Voltage Overscaling by Unbalanced Pipelining - Case Study: 8-bit Wallace Tree Multiplier (Layout - Cadence Virtuoso, Nanosim).

ACADEMIC EXPERIENCE

Integrated Systems Laboratory, Purdue *West Lafayette,IN*
Graduate Research Assistant *Aug. 2011 - Jul. 2014, Aug. 2015 - Present*
Intel PhD Research Fellow *Aug. 2014 - Jul. 2015*

I have worked on several research projects broadly in the areas of Approximate computing, Spin based logic and memory design, Accelerator based computing and Variation-aware recovery based design.

School of Electrical and Computer Engineering, Purdue *West Lafayette,IN*
Graduate Teaching Assistant *Aug. 2010 - Dec. 2011*

I developed partial course material and exams for *Linear Circuit Analysis (201)*. I was appointed head TA to administrate and co-ordinate a group of 6 TAs for 201, that had an enrollment of roughly 500 sophomore and junior level students.

Power Quality Laboratory, Indian Institute of Technology, Madras *Chennai, India*
Summer Research Fellow *May 2009 - Aug. 2009*

I was awarded an undergraduate research fellowship by the Department of Electrical Engineering, Indian Institute of Technology Madras, and worked with Dr. Mahesh Kumar on real-time power quality monitoring using DSPs.

- Designed a TMS320Cx DSP based monitoring system that measures the higher order harmonic content present in supply voltage.
- Frequency variations in the supply can pose significant challenges to the measurement and was dealt with using suitable sampling techniques.

EXTRA CURRICULAR AND LEADERSHIP ACTIVITIES

- Class representative and Member of Student council College of Engineering, Guindy for the academic year 2009-10.
- Appointed Head Teaching Assistant to administrate a group of 6 TAs for a class with an enrollment of roughly 500 students.
- "National Social Service" (NSS, Govt. of India) volunteer and member of media team during service camps.
- Treasurer, Purdue Badminton Club 2014-15; Community service chair, Purdue Badminton Club, 2013-14; Primary Organizer, Purdue Badminton Open 2014-16.
- Winner of District (County) level Badminton Championships in the super senior (Higher Secondary) category. Avid Badminton enthusiast; medallist at several university tournaments in the mid-west and pudget-sound regions.
- State-level Orchestra Competition winner as a violinist during high school. Member of Indian Classical Music Association at Purdue.
- Contributor to college magazines *viz.* "Guindy Times" and "Impulse".
- Organizer of various inter/intra-college technical events (more than 500 attendees) at Anna University, Chennai.