RANGHARAJAN VENKATESAN
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EDUCATION

- PhD, Electrical and Computer Engineering (August 2009 - present)
  Purdue University
  Thesis: Post-CMOS Computing – Circuits and Architectures
  Primary research area: VLSI and Circuit Design
  Advisor: Prof. Anand Raghunathan
  Expected graduation date: June 2014
  CGPA: 3.98/4.00
- B.Tech in Electronics and Communication Engineering (July 2005 - May 2009)
  Indian Institute of Technology Roorkee
  Thesis: Effect of Process variations on FinFET based SRAM at 32nm node
  Advisor: Prof. Sudeb Dasgupta
  CGPA: 9.03/10.00 **(Top Ranked Student in ECE department)**

RESEARCH INTEREST

- Emerging memory technologies
- Approximate computing
- Low power circuit/architecture design
- Neuromorphic computing
- System-on-Chip (SoC) design

PROFESSIONAL EXPERIENCE

- Graduate research intern – Circuit Research Labs, Intel, Jones Farm, Hillsboro, Oregon (June 2013 – Sept 2013)
- Graduate technical intern – Graphics Low power path-finding team, Intel, Jones Farm, Hillsboro, Oregon (May 2012 – Sept 2012)
- Undergraduate research intern – The Khorana Program for Scientific Exchange , University of Wisconsin – Madison (May 2008 – July 2008)

HONORS

1. Awarded Bilsland Dissertation Fellowship by College of Engineering, Purdue University, 2013-14.
2. Best Paper Award, International Symp. on Low Power Electronics and Design (ISLPED), 2012.
3. Awarded Ross fellowship by the graduate school, Purdue University, 2009-10.
4. Received Silver medal for being ranked 1st in ECE, IIT Roorkee, 2009.
5. Best Undergraduate Thesis Award, Electronics and Communication Engineering-2009, IIT Roorkee.
6. Awarded Khorana scholarship by University of Wisconsin-Madison, 2008.
7. Awarded National Talent Search Examination scholarship by Govt. of India, 2003-09.

PATENTS

1. "Memory Cell With Retention Using Resistive Memory," Filed with USPTO 2013.

SKILLS

- Programming Languages – C, C++, Verilog, Python, Tcl.
- EDA tools – Synopsys (Design Compiler, ICC, Primetime), Cadence (ICFB, Virtuoso, Encounter Library Characterizer), Spice, Quartus, Modelsim, CACTI.

RELEVANT COURSES

MOS VLSI Design, VLSI Design Automation, System-on-Chip Design, Advanced VLSI Design, Computer Architecture, Programming Parallel Machines, Modeling and Optimization of High performance Interconnects, Solid State Devices.

RESEARCH EXPERIENCE

- **Graduate Research Intern, Circuit Research Labs, Intel Corp. (June'13-Sep'13)**
  - **STT-MTJ based Retention Flip-Flop Design for Fine-grained power gating(Patent pending)**
    - Proposed a novel, robust retention flip-flop design using STT-MTJs.
    - Analyzed the tradeoffs and demonstrated the working of the proposed design under 5σ variation in process parameters.
    - Performed break-even analysis and examined the utility of STT-MTJ flip-flop for fine-grained power-gating.
- **Graduate Technical Intern, Graphics Path-Finding Team, Intel Corp. (May'12-Sep'12)**
  - **Low power design techniques for graphics processing cores**
    - Developed a tool to identify potential hot-spots for power reduction.
    - Evaluated the benefits of different power optimization techniques for various hardware building blocks in graphics processing units.
- **Graduate Student Researcher, Purdue University (Aug'09-Present)**
  - **Spintronic Deep Learning Engine (SPINDLE)**
    - Proposed a programmable architecture with 3-tier hierarchy of processing elements that captures different levels of parallelism in neuromorphic workloads.
    - Explored different architecture-level organization and scheduling policies to match the characteristics of spin-devices with applications.
  - **Spin-based Cache Hierarchy for GPGPUs**
    - Explored the tradeoffs involved in cache design for GPGPUs.
    - Designed a spin-based cache hierarchy consisting of different variants of spin memories to achieve high density, energy efficient cache.
    - Proposed warp-id based prediction scheme and Shift-aware Preshift Buffer design to optimize the performance.
  - **Domain Wall Memory (DWM) based Cache Hierarchy for general purpose processors**
    - Designed different DWM bit-cell structures considering various architectural requirements and application characteristics.
    - Proposed an All-Spin cache design with suitable organization and management policies.
    - Developed suitable circuit and architectural models for evaluating the proposed cache.
  - **Domain-specific Many-core processor using spin-based memories and Tunneling FETs**
    - Designed many-core processor for RMS applications using DWM and STT-MRAM based memory and Tunneling FET (TFET) based processing cores.
    - Performed architectural exploration to match device-application characteristics and obtain optimum benefits in power and performance.
  - **Benchmarking of post-CMOS general purpose processor and GPU designed using spin-based memories and Heterogeneous Tunneling FET (HTFET) based logic**
    - Developed a standard cell library based on Heterogeneous Tunneling FETs (HTFETs) at 10nm node.
    - Developed CACTI model to evaluate spin-based memories (STT-MRAM and Domain Wall Memory).

- Synthesized and evaluated the power and performance of Leon3 embedded processor, UltraSparc processor core and Theia GPU (an open-source GPU).

- **Variation-aware System-on-Chip Performance Analysis using Emulation**
  - Proposed emulation based framework to analyze effect of process variations on SoC
  - Achieved considerable speed-up over state-of-the-art system-level simulation tools.
  - Demonstrated the utility in performing design-space exploration efficiently.
- **Verification of Circuits for Approximate Computing**
  - Developed a novel verification framework for approximate circuits using BDD and SAT solvers.
  - Demonstrated the effectiveness in evaluating different approximate arithmetic circuits for different verification metrics.

➢ **Undergraduate Research Intern, University of Wisconsin-Madison (May'08-Aug'08)**

- **Calibration of Thermal Sensors in Integrated Circuits**
  - Developed a novel technique to estimate the calibration parameters of embedded thermal sensors.
  - Demonstrated the accuracy of the technique using a sample thermal profile of an integrated circuit.

➢ **Undergraduate Student Researcher, Indian Institute of Technology Roorkee (May'07-May'09)**

- **Effect of Process Variations on FinFET based SRAM at 32nm Node (Best Undergraduate Thesis Award).**
  - Analyzed FinFET characteristics at 32nm node.
  - Designed FinFET based SRAM and estimated SRAM performance metrics – power, access time, noise margin in the presence of variations.
  - Compared SRAM performance metrics between underlapped and self-aligned FinFET based SRAMs.
- **Ultra low power stacked SRAM cell design**
  - Analyzed the effect of stacking on various performance metrics of SRAM.
  - Compared SRAM performance metrics between Half-stacked and Full-stacked SRAM.

SELECTED COURSE PROJECTS

- **Hardware/Software co-design of JPEG encoder** (Sept'09-Dec'09)
- **Over-scaling by unbalanced pipelining using Wallace tree multiplier** (Sept'09-Dec'09)
- **Leakage power reduction using drowsy caches** (Sept'10-Dec'10)
- **Purdue Inductance Extraction Package** (Sept'12-Dec'12)

PUBLICATIONS

Conferences

1. **R. Venkatesan**, S. Ramasubramanium, S. Venkataramani, K. Roy, and A. Raghunathan, "STAG: Spintronic-Tape Architecture for GPGPU Cache Hierarchies," *International Symposium on Computer Architecture (ISCA)*, June 2014 (Accepted for publication).
2. S. Ramasubramanium, **R. Venkatesan**, M. Sharad, K.Roy, and A. Raghunathan, "SPINDLE: SPINtronic Deep Learning Engine for Large-scale Neuromorphic Computing," *IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)*, September 2014 (Accepted for publication).

3. M. Sharad, **R. Venkatesan**, X. Fong, A. Raghunathan, and K. Roy, "Energy-Efficient MRAM Access Scheme Using Hybrid Circuits Based on Spin-Torque Sensors," *IEEE Sensors*, November 2013.
4. M. Sharad, **R. Venkatesan**, A. Raghunathan, and K. Roy, "Multi-level Magnetic RAM using Domain wall Shift for Energy-Efficient, High-Density Caches", *IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)*, September 2013.
5. M. Sharad, **R. Venkatesan**, X. Fong, A. Raghunathan, K. Roy, "Reading Spin-Torque Memory with Spin-Torque Sensors", *IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)*, July 2013.
6. M. Sharad, **R. Venkatesan**, A. Raghunathan, and K. Roy, "Domain-wall Shift based Multi-Level MRAM for High-speed, High-density and Energy-efficient Caches", *IEEE/ACM Device Research Conference (DRC)*, June 2013.
7. **R. Venkatesan**, M. Sharad, K. Roy and A. Raghunathan, "DWM-TAPESTRI – An Energy-efficient All-Spin Cache using Domain Wall Shift based Writes", *IEEE/ACM Design, Automation, and Test in Europe (DATE)*, March 2013.
8. **R. Venkatesan**, V. Kozhikkottu, C. Augustine, A. Raychowdhury, K. Roy and A. Raghunathan, "TapeCache: A High Density, Energy Efficient Cache based on Domain Wall Memory", *IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)*, July- August 2012 (**Best Paper Award**).
9. **R. Venkatesan**, A. Agarwal, K. Roy, and A. Raghunathan, "MACACO: Modeling and Analysis of Circuits for Approximate Computing," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, November 2011.
10. **R. Venkatesan**, V. Chippa, C. Augustine, A. Raghunathan, and K. Roy, "Energy Efficient Many-core Processor for Recognition and Mining using Spin-based Memory," *IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)*, June 2011.
11. V. Kozhikkottu, **R. Venkatesan**, A. Raghunathan, and S. Dey, "VESPA: Variability Emulation for System-on-chip Performance Analysis," *IEEE/ACM Design, Automation, and Test in Europe (DATE)*, March 2011.

Journals

1. **R. Venkatesan**, M. Sharad, V. J. Kozhikottu, C. Augustine, A. Raychowdhury, K. Roy, and A. Raghunathan, "Cache Design with Domain Wall Memory," IEEE Transactions on Computers. (Accepted for publication)
2. **R. Venkatesan**, M. Sharad, K. Roy, and A. Raghunathan, "Dense, Energy-efficient All-Spin Cache Hierarchy using Shift based Writes and Multi-Level Storage," *ACM Journal on Emerging Technologies in Computing Systems*. (under review)
3. **R. Venkatesan**, V. Chippa, C. Augustine, A. Raghunathan, and K. Roy, "Domain-Specific Many-core Computing using Spin-based Memory," *IEEE Transactions on Nanotechnology*. (Accepted for publication).
4. X. Fong, **R. Venkatesan**, A. Raghunathan, and K. Roy, "Non-volatile Complementary Polarizer Spin-Transfer Torque (CPSTT) On-chip Caches: A Device/Circuit/Systems Perspective," IEEE Transactions on Magnetics. (Accepted for publication).
5. B. Raj, J. Mitra, D.K. Bihani, **R. Venkatesan**, A.K. Saxena, S. Dasgupta, "Process Variation Tolerant FinFET Based Robust Low Power SRAM Cell Design at 32 nm Technology," Journal of Low Power Electronics (JOLPE), April 2011.

6. B. Raj, J. Mitra, D.K. Bihani, **R. Venkatesan**, A.K. Saxena, S. Dasgupta, "Analysis of Noise Margin, Power and Process Variation for 32nm FinFET Based 6T SRAM Cell", Journal of Computers, May 2009.

Posters

1. **R. Venkatesan**, M. Sharad, K. Kwon, S. H. Choday, K. Roy, and A. Raghunathan, "Cache Hierarchy Design using Spin-based Memory," C-SPIN (SRC), September 2013.
2. S. Ramasubramanium. **R. Venkatesan**, M. Sharad, A. Raghunathan, and K. Roy, "Spintronic Deep Learning Processor," C-SPIN (SRC), September, 2013.
3. M. Sharad, **R. Venkatesan**, A. Raghunathan, and K.Roy, "Multi-level STT-MRAM using domain wall magnet for energy efficient, high density caches," Work-in-Progress Session, *ACM/IEEE Design Automation Conference (DAC)*, June 2013.
4. **R. Venkatesan**, V. Kozhikkottu, C. Augustine, A. Raychowdhury, K. Roy and A. Raghunathan, "Domain Wall Memory based Cache," Work-in-Progress Session, *ACM/IEEE Design Automation Conference (DAC)*, June 2012.
5. **R. Venkatesan**, A. Agarwal, A. Raghunathan, and K. Roy, "Modeling and Analysis of Circuits for Approximate Computing", Work-in-Progress Session, *ACM/IEEE Design Automation Conference (DAC)*, June 2011.
6. J. Mitra, D. K. Bihani, **R. Venkatesan**, and S. Dasgupta, "Ultra Low Power Stacked SRAM Cell Design at 90nm node," Workshop on Recent Advances of Low Dimensional Structures and Devices (WRA-LDSD), April 2008.

LEADERSHIP EXPERIENCE

- Treasurer of Purdue University Cricket Club (PUCC), 2012-14.
  - Managed financial activities of PUCC
  - Planned PUCC participation in 4 national/club tournaments
- Event manager of Cognizance'08 (Annual technical festival, IIT Roorkee).
  - Organized 8 technical/non-technical events.
  - Over 800 students from 76 different colleges participated in the event.
- Secretary of Yoga Club at IIT Roorkee for the 2008-09 and Joint Secretary for the year 2008-09.
  - Organized various intra-university yoga competitions.
  - Participated in national level inter-university yoga competition.

REFERENCES

- Available on request