A modular process for integrating thick polysilicon MEMS devices with sub-micron CMOS

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ABSTRACT

A new MEMS process module, called Mod MEMS, has been developed to monolithically integrate thick (5-10um), multilayer polysilicon MEMS structures with sub-micron CMOS. This process is particularly useful for advanced inertial MEMS products such as automotive airbag accelerometers where reduced cost and increased functionality is required, or low cost, high performance gyroscopes where thick polysilicon (>6um) and CMOS integration is required to increase poly mass and stiffness, and reduce electrical parasitics in order to optimize angular rate sensing. In this paper we will describe the new modular process flow, development of the critical unit process steps, integration of the module with a foundry sub-micron CMOS process, and provide test data on several inertial designs fabricated with this process.

Keywords: MEMS IC integration, Selective epi, CMP, surface micromachining, deep Si etch

1. INTRODUCTION

Previous integrated MEMS processes[1,2] have allowed the integration of only relatively thin polysilicon layers (<3um) with advanced CMOS processes. One process[1] interleaved the MEMS process steps in the middle of a BiCMOS process, which resulted in both topology and thermal budget constraints. The latter constraint limited the ability to stress relief the MEMS poly by high temperature annealing. A second process[2] used a MEMS first module approach which permitted high temperature poly stress relief, but utilized a well planarization approach which did not permit planarization after each MEMS poly layer, and complicated the definition and planarization of thick polysilicon layers. This inability to planarize (e.g. by oxide deposition and CMP) after each MEMS poly step also results in a large area increase of the overall MEMS module. Mod MEMS was developed to remove these limitations, and allow the area efficient integration of thick multi-layer MEMS poly structures, annealed at 1100C or higher for complete stress relief, with submicron CMOS processes.

The Mod MEMS process uses epi planarization[3] in combination with a post epi CMP step. The process flow for Mod MEMS is given in Fig. 1. The critical unit processes developed for Mod MEMS were: 1) growth of low stress 6um thick polysilicon, 2) growth of an oxide sidewall spacer on the MEMS islands prior to the selective epi step, 3) selective epi which provided good planarization between the very thick MEMS regions and the surrounding Si which was used for submicron CMOS, 4) CMP to both smooth the thick polysilicon, and planarize the MEMS module after epi to facilitate subsequent submicron CMOS processing, 5) Bosch etching to define 6um poly MEMS structures with vertical sidewalls, 6) modification of the ADI proprietary resist pedestal release process for final release of the MEMS structures. Most of the MEMS processing is done prior to CMOS processing thus allowing all high temperature MEMS processing prior to CMOS. As will be described below post epi CMP provides good surface planarity for subsequent sub-micron CMOS processing.

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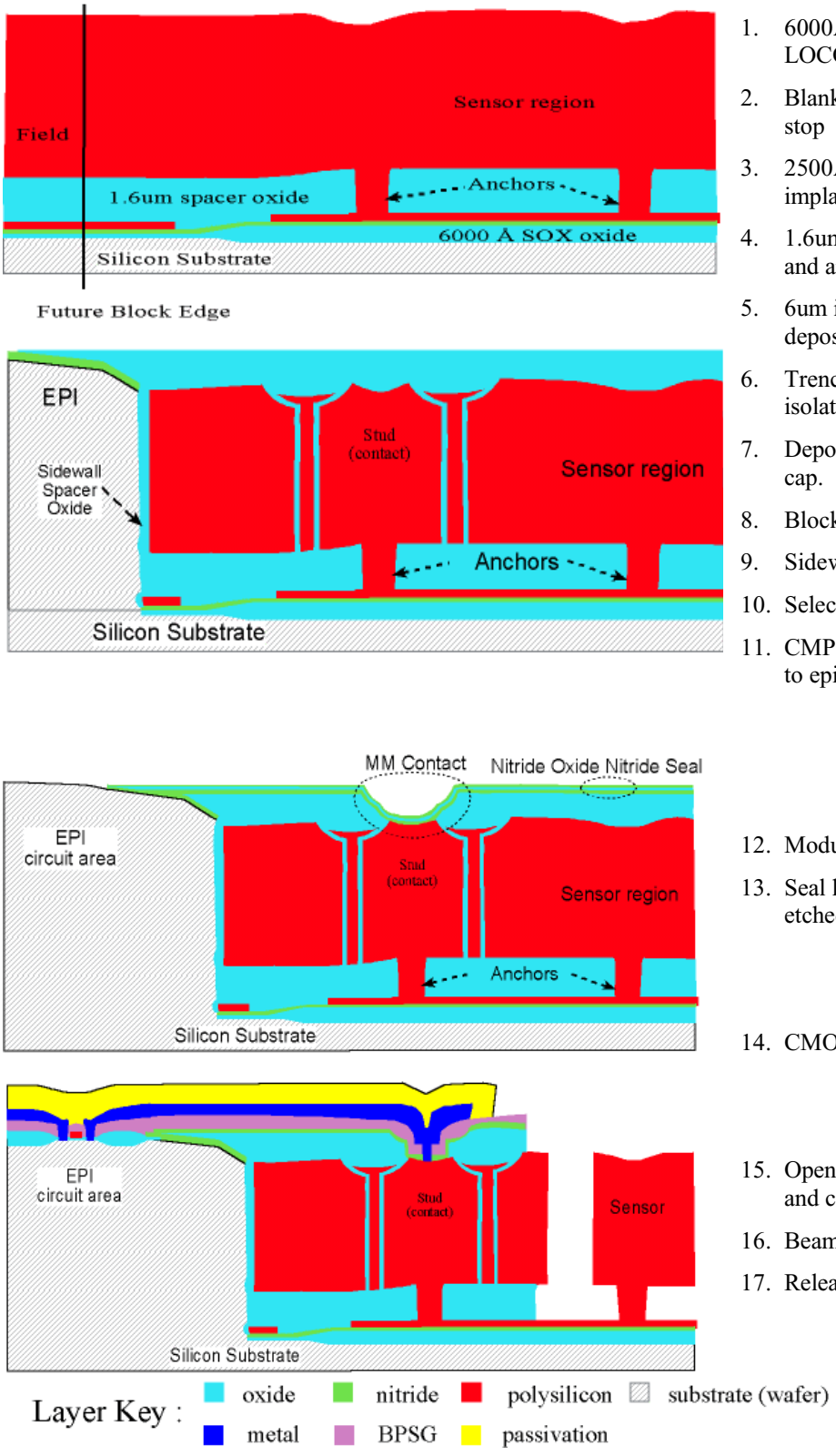

1. 6000A sensor oxide grown with LOCOS process
2. Blanket nitride for release etch stop
3. 2500A poly ground plane implanted and patterned
4. 1.6um spacer oxide deposited and anchors patterned
5. 6um in-situ doped poly deposited
6. Trench for contact stud isolation
7. Deposit 2um undoped TEOS cap.
8. Block isolation etch
9. Sidewall spacer
10. Selective epitaxy
11. CMP to planarize MEMS block to epi
12. Modular MEMS contact opened
13. Seal layers deposited and etched
14. CMOS module process
15. Open etch (cuts through seal and cap layers)
16. Beams mask and etch
17. Release

Figure 1: Mod MEMS process flow.

The modularity of the process was demonstrated by fabricating the MEMS module steps at Analog Device's MEMS manufacturing line, and then using either ADI's standard Bimos process (used for ADI accelerometer production[1]) or a 0.8um, double metal CMOS external foundry process for the IC process integration. Successful module integration was achieved for both processes as will be described below.

2. EXPERIMENTAL

2.1 6um polysilicon growth, contact trenches, and block sidewall spacer

An ASM A400 vertical CVD furnace was used to deposit both the 0.25um ground poly layer, and the 6um structural poly layer. In-situ phosphorus doping was used during the 6um poly growth layer in order to uniformly dope this very thick poly layer. The deposition temperature, gas flows and pressure were carefully balanced to obtain crack free as-deposited poly which was a critical control issue at poly layer thicknesses greater than 5um. Once the poly was given a 900C anneal or higher the risk of cracking was eliminated. After annealing at 1100C or higher the films were nearly stress free with an in-plane tensile stress of ~2E7 dyne/cm^2, and very low vertical stress gradients as evidenced by out of plane curvature of released 500um long cantilevered beams of 0.1um or less which corresponded to a radius of curvature of >0.5m. The 6um poly sheet resistance was 15 ohm/square. The poly surface was quite rough after growth and it was found necessary to perform a brief CMP touch polish to remove this roughness prior to subsequent oxide CMP planarization after the selective epi planarization step. After the poly CMP step the poly surface roughness was reduced from a total range of 8,000A to less than 200A, and an RMS roughness of <1nm as measured by AFM.

After the 6um structural poly growth and anneal the next most critical step was the formation of isolation trenches to provide electrical isolation between MEMS regions at different potentials. This involved a deep Si etch through the 6um poly layer using an Alcatel deep Si Bosch etch tool. We then used a standard Novellus TEOS conformal oxide deposition and oxide etch back to form a trench sidewall spacer. Finally, a poly deposition was used to fill the isolation trench followed by a poly etch back to remove the trench fill poly from the surrounding field. The main process control issue in this isolation trench process was to insure that an adequate overetch margin was used to etch completely through the 6um MEMS poly to the spacer oxide. Since the poly etch had good selectivity to oxide, and the spacer oxide was thick, this was relatively straightforward. However, in the early development phase special test structures were created to allow hand probing after poly trench fill and etchback to insure that good isolation had been achieved.

After the isolation trenches were completed a 2um capping oxide and nitride (used as an oxidation barrier) was deposited, and the MEMS structural regions were then separated as isolated blocks by a photoresist mask and etch step. This etch was done to the ground poly which was unpatterned in the field. The field ground poly acted as an etch stop for this step. A thermal oxidation then formed a self-aligned oxide spacer on the block 6um poly sidewall. Next the oxide formed on the field ground poly and the field ground poly itself were dry etched to the underlying field nitride layer. This nitride, and the block capping nitride were then removed in a hot phosphoric etch. Finally, the thin oxide under the field nitride was dipped off in a brief HF etch. At this point the MEMS poly was encapsulated in oxide and the devices were now ready for selective epi planarization. Several strategies were explored to provide the MEMS block oxide encapsulation, but this process was found to be the most robust.

2.2 Selective epi planarization

The next step was the key to providing planarization around the very thick MEMS structures in order to allow integration with submicron CMOS. With the MEMS regions encapsulated in oxide, a selective epi process was developed to grow epi around the MEMS block regions up to the top of the block. This epi process was developed in an ASM Epsilon One single wafer, low pressure epi tool. Substantial effort was required to develop this process, but the final process was robust, and highly repeatable. The Si source to Cl gas ratio was varied during growth to achieve good selective epi, and good epi uniformity across the wafer. The ground poly at the edge of the MEMS blocks was actually not covered with a sidewall oxide. However, it turned out that this poly was close enough to the

surrounding Si substrate, that the substrate epi rapidly overgrew this region, and good epi was obtained all the way up the block sidewall. Due to slow crystal growth planes exposed at the edge of the block, a roughly 1.5um facet was typically observed at the edge of the MEMS block region. A schematic drawing, description, and cross section SEM of the epi growth process are shown in Figure 2.

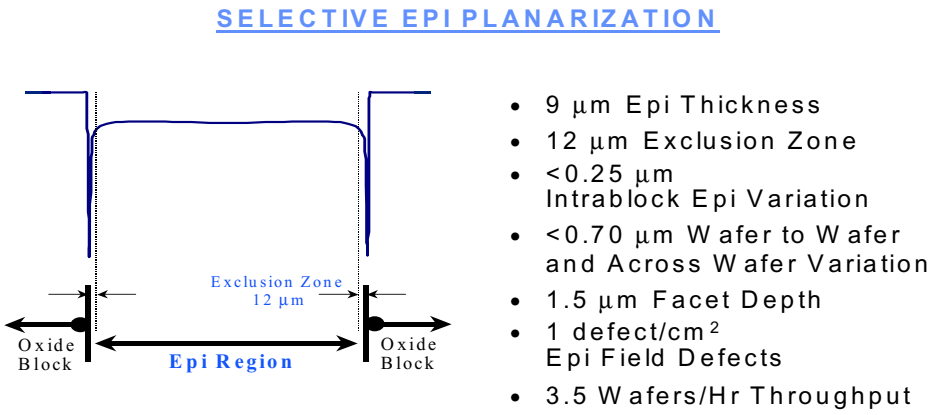

Figure 2: Selective epi planarization process.

Typically 9um epi was needed to bring the final silicon surface for CMOS processing above the level of the ground poly, spacer oxide, 6um structural poly, and capping oxide. This permitted subsequent CMP planarization and accounted for cumulative variations in the MEMS module layer thicknesses. The 12 um exclusion region in the epi next to the MEMS block was the area where the epi growth rate was lower due to the presence of slow growth

crystal planes in this area. The reduced growth rate resulted in an epi facet 1.5um deep near the block edge. Outside this exclusion region the epi thickness varied by no more than 0.25um which was considered more than adequate for CMOS stepper photolithography depth of field requirements. The use of selective epi, which requires a higher chlorine gas flow, and process tuning to get good across wafer epi growth uniformity resulted in relatively slow epi growth rates. However the final wafer throughput of 3.5 wafers per hour was considered adequate for this critical step.

After selective epi, an oxide/nitride/oxide deposition followed by chemical mechanical polishing (CMP) filled the epi facet and finished the MEMS planarization process. The nitride provided a polish stop layer for a conventional oxide CMP process. After CMP, the nitride polish stop layer was removed from the epi field, and a large area, shallowly sloped contact wet etch was performed to the 6um MEMS poly to provide a contact region where a standard CMOS metal 1 contact process could be performed. Finally, seal layers were deposited and patterned to provide protection for the MEMS region during the subsequent CMOS process. This seal was a multilayer oxide and nitride stack designed to protect the MEMS layers during clean steps, initial oxidations, wet etches and the LOCOS field oxide process sequence used at the start of a typical CMOS or BiCMOS process. The seal layer stack and thicknesses can be tailored as needed to accommodate the desired circuit module. A cross section SEM of a MEMS block edge at this step is given in Figure 3. The striations in the epi seen next to the block are cleaving artifacts. As can be seen here, the final MEMS to field epi transition is highly planarized.

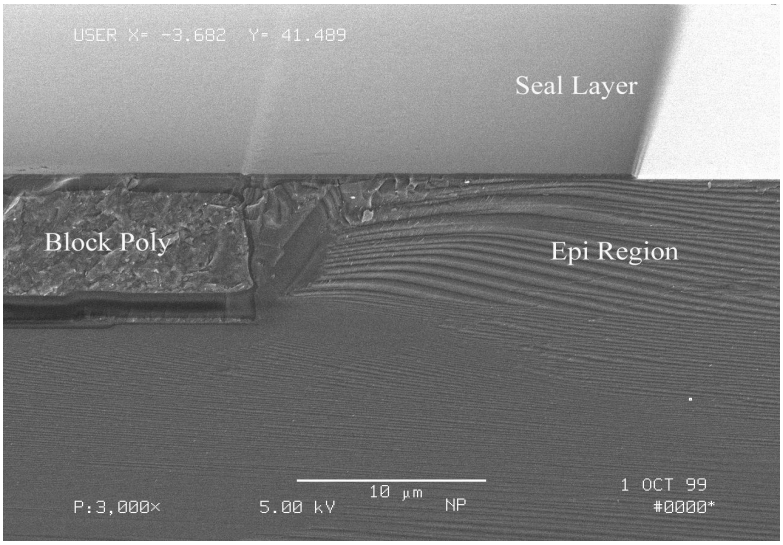

Figure 3: Mod MEMS after epi planarization and nitride seal.

At this point the wafers were ready for standard IC processing. Initially an ADI BiCMOS process was used to demonstrate the process using an automotive accelerometer design (ADXL76) modified to work with 6um poly, from the design for the standard 2um poly production process. The first lots with the final Mod MEMS process worked well and soon provided both very good wafer probe and final package yields (>70% probe yield). We then obtained designs from UC Berkeley designed to use Mod MEMS with 0.8um CMOS which was obtained from an external foundry using their standard 0.8um double level metal CMOS process. Two different design runs were eventually run from UC Berkeley and both resulted in good yields with all viable designs functional on the first pass of each design run.

The two major concerns for IC process integration with Mod MEMS were: 1) providing a MEMS seal layer that would withstand the standard oxidation and HF oxide etch steps, and the LOCOS field oxidation and nitride strip steps, and 2) providing good contact between Metal 1 and the MEMS poly using some form of the standard IC contact and metal 1 process. As it turned out a simple multi-layer oxide plus nitride stack provided adequate protection of the beam module, and the large area sloped pre-IC contact area etch to the Mod MEMS contact regions resulted in no changes to the contact or metal 1 processes for the two target IC processes described above. Furthermore it is believed that even with more advanced W plug contact processes that fairly simple modifications of the pre-IC MEMS contact area could be made which would minimize or possibly eliminate any required changes to the target CMOS contact process.

2.3 MEMS beam etch and release

After completion of the foundry IC process through passivation, the MEMS area was opened up and the 6um MEMS poly layer (beam) was etched and released. A photomask and dry/wet etch opened up the beams area. A resist photomask and Si Bosch etch (using a dep/etch process developed at Bosch for deep MEMS etching) on an Alcatel single wafer system was then used to pattern the 6um MEMS poly layer. A cross section SEM after beam etch but before resist strip is shown in Figure 4.

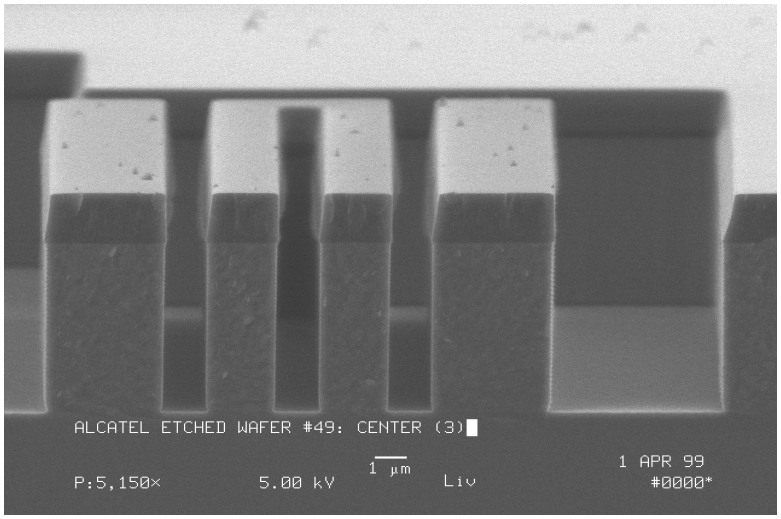

Figure 4: 6um beam poly etch (before resist strip).

Finally the beam poly was released using a slight modification of ADI's proprietary photoresist pedestal release process. This process places resist blocks under and between the beam poly which hold the beams in place (i.e. prevent lateral and vertical stiction) during drying after the oxide HF release etch and final spin rinse dry. One additional development required in this process was to modify the beam poly surface condition under the photoresist protecting the field around the beam module during the HF release step. This was necessary to prevent lifting of the resist protecting the field and subsequent attack of the circuitry surrounding the beam module during the long HF release step. Once optimized, no resist lifting (blowout) was seen and the surrounding circuit metal was protected. A SEM illustrating the pedestal release process is shown in Figure 5, e.g. note the resist blocks in the inset perpendicular to the poly beams which hold the poly in place during drying after HF release (the poly surface on this device did not receive CMP).

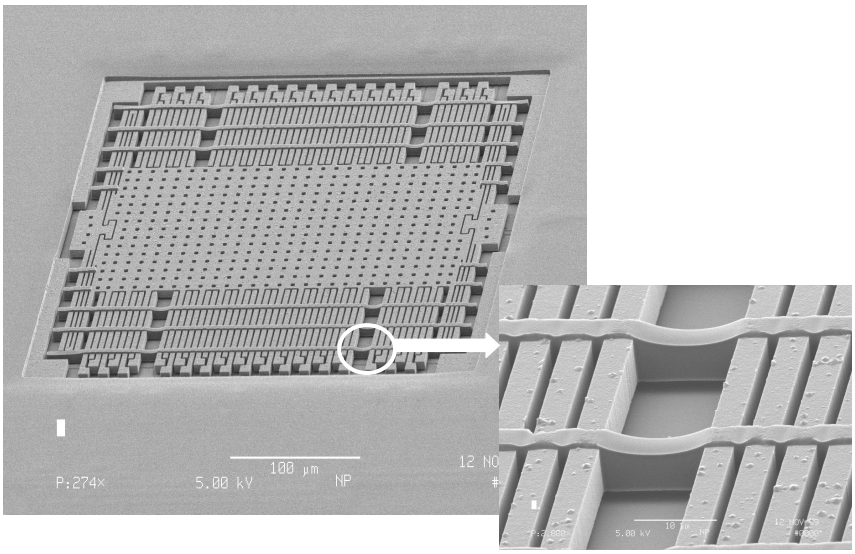

Figure 5: Resist pedestal release process.

After the HF release and spin rinse dry, the wafers were put in a downstream oxygen plasma to remove the resist in order to fully release the beams without stiction. A fully released structure is shown in Figure (6) in the next section.

This completes the processing of the Mod MEMS wafers. The Mod MEMS die were then diced and packaged using ADI's patented MEMS die soft cap protection and backside sawing process. The assembly yields for the Mod MEMS parts were quite high (>90%) and compared well to our standard production process.

3. RESULTS & DISCUSSION

The main process parameters and features of Mod MEMS are summarized as follows:

- 0.25um ground poly with a sheet resistance of 50 ohm/square.
- Oxide isolated poly trench vias to allow metal 1 contact to isolated ground poly lines
- 6um thick released MEMS structural layer with a sheet resistance of 15 ohm/square, in plane tensile stress ~1MPa, and radius of curvature of >0.5m
- Use of CMP to smooth the 6um poly surface to <1nm RMS roughness
- Sloped contact area process that allowed contact to the 6um MEMS poly by the IC first level Al with little or no modification of the first metal process (no modification for the two IC processes demonstrated).

The primary test vehicle was the ABM676; a 50g single-axis lateral accelerometer integrated with the ADI production BiCMOS process. The ABM676, shown in Figure 6, utilized the same circuit layout of the ADXL76, ADI's high volume airbag accelerometer, with only a modified sensor design. The sensor was designed to match the performance of the ADXL76 so that the production laser trim and test programs could be used without significant modifications thus jump-starting the characterization effort. Parameters that were matched included the resonant frequency, capacitive change per gee, and resulting sensitivity as well as the self-test voltage. Table 1 shows a summary of the results as compared with the ADXL76. The performance of the ABM676 was better than

that of the ADXL76 in all but the offset parameter, which is typically dominated by packaging effects. The laser trim yield of the ABM676 based on the ADXL76 production trim limits resulted in a yield of about 60% over all lots and wafers. This average yield is excellent for a process at this level of maturity.

Table 1: Results summary of the ABM676 as compared with the ADXL76 high volume airbag accelerometer.

	ABM676		ADXL76	
	mean	sigma	mean	sigma
Natural Frequency at Trim	**25.8 kHz**	**0.433 kHz**	**24.9 kHz**	**0.615 kHz**
Sensitivity	**39.2 mV/g**	**0.36 mV/g**	**38.3 mV/g**	**0.66 mV/g**
Offset	**63 mV**	**53 mV**	**29 mV**	**45 mV**
Self Test Voltage	**388 mV**	**26 mV**	**386 mV**	**16 mV**

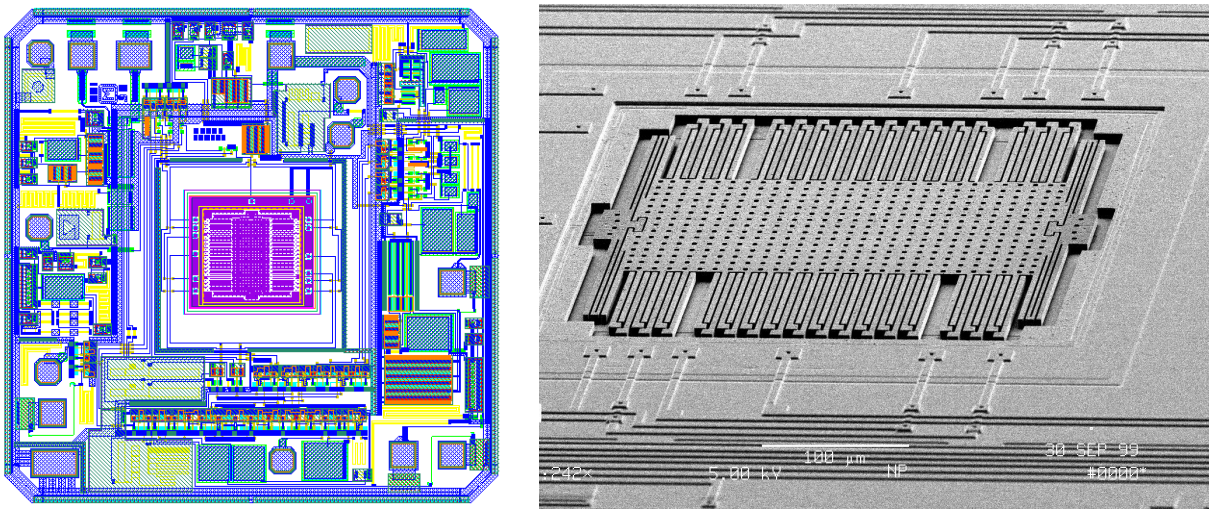

Figure 6: Layout and SEM of the ABM676, a 6um thick polysilicon lateral accelerometer integrated with an ADI BiCMOS process.

Two separate inertial design runs were also generated at the Berkeley Sensor and Actuator Center at UC Berkeley to demonstrate the use of Mod MEMS integrated with a standard foundry, 0.8um double metal CMOS process. Novel accelerometer and gyroscope devices were designed for these two runs. More detailed results for these devices are reported elsewhere[4,5], but both runs resulted in high functional test yields for most devices evaluated. One design of note was the dual x- and y-axis gyroscope[5], which is shown in Figure 7. This chip contains two separate mechanical structures and associated electronic circuits. The proofmass is electrostatically actuated to vibrate in the z-direction. Rotation about the x- and y-axis, respectively, produces an in-plane motion detected by the electronic circuitry with on-chip analog-to-digital conversion. The combination of high performance MEMS and sub-micron CMOS result in a compact layout of only 3mm^2 per axis. A detailed report of the performance of this device is provided in Ref 5.

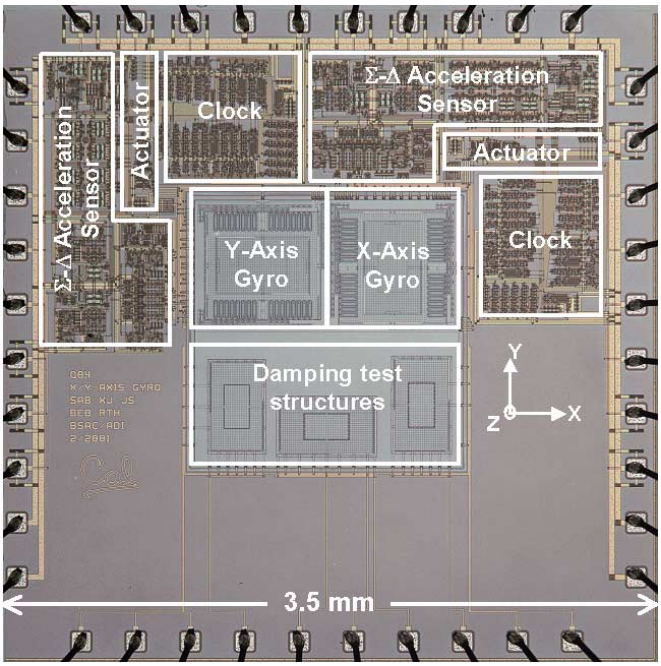

Figure 7: Microphotograph of the dual X and Y axis gyros[5] which were integrated using a 1um foundry CMOS.

4. CONCLUSIONS

A new modular process has been described, called Mod MEMS, which integrates thick polysilicon MEMS structures with sub-micron CMOS sense and control electronics. A MEMS first module is implemented to allow high temperature annealing of the MEMS poly structures for very low in-plane stress and low vertical stress gradients which results in very flat released MEMS structures. Key unit processes developed to implement this process were: 1) a thick, low stress polysilicon process, 2) CMP both after key MEMS poly steps and after epi planarization, 3) deep Si Bosch etching for good MEMS poly beam definition, 4) selective epi planarization, including an oxide encapsulation of the MEMS module prior to epi, 5) an oxide/nitride MEMS module seal layer to prevent process interactions between the MEMS and CMOS process modules, 6) a process to allow the CMOS first metal process to readily contact the MEMS poly, and 7) a process to release the MEMS structural layers after completion of all MEMS and IC processing.

Mod MEMS was demonstrated on a BiCMOS process, and a 0.8um foundry CMOS process. Good yields of fully functional die were obtained with both processes. Accelerometer electrical results with the BiCMOS process were presented which compared well in yield and performance to comparable commercial airbag accelerometers fabricated in ADI's production iMEMS process. Accelerometer and gyroscope designs from UC Berkeley were fabricated with Mod MEMS integrated with a standard foundry, double metal 0.8um CMOS process. All designs yielded functional die with good probe yield. Electrical results were presented on a novel x-y two axis gyroscope.

Mod MEMS provides a new process to monolithically, and cost effectively integrate high performance inertial MEMS and advanced CMOS for optimal electrical performance and a high degree of electrical functionality. The modular, MEMS first design, results in little or no compromise between the MEMS and CMOS devices and processes. Furthermore the excellent planarity and low surface roughness of the released MEMS poly makes Mod MEMS suitable for many optical MEMS applications.

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