# POLY-SIGE HIGH FREQUENCY RESONATORS BASED ON LITHOGRAPHIC DEFINITION OF NANO-GAP LATERAL TRANSDUCERS

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## ABSTRACT

In this paper, we describe a new approach for fabrication of micromechanical resonators for radio-frequency communication applications. The proposed process provides ultra-narrow lateral gaps using lithographically-defined sacrificial Ge blades. By using Germanium as a sacrificial material, we eliminate the need for HF etching to release mechanical structures and thereby simplify the integration of these devices with CMOS electronics. Polycrystalline silicon-germanium (poly-SiGe) is used as the structural material in order to keep the thermal budget low (maximum temperature 425°C), so as to be compatible with CMOS metallization stacks. Resonators with frequencies up to 200MHz and Q ranging from 3,500 to 14,000 are demonstrated.

***Index terms –*** MEMS, resonator, silicon-germanium

## INTRODUCTION

Micromachined resonators are promising as on-chip replacements for discrete filters and oscillators which are presently implemented using off-chip quartz and surface-acoustic-wave (SAW) devices in wireless communication systems [1]. The monolithic integration of control, amplification and signal-processing electronics with radio frequency micro-electromechanical devices (RF MEMS) also reduces parasitic capacitances and inductances as well as overall system power consumption. Recent progress toward a low-thermal-budget polycrystalline silicon-germanium (poly-SiGe) MEMS technology promises to make possible the modular cofabrication of high-performance surface-micromachined structures on top of completed CMOS wafers [2]. However, a detailed process integration scheme for poly-SiGe resonator fabrication -- particularly one that provides ultra-narrow lateral gaps between the resonator and drive/sense electrodes -- has yet to be explored.

There are several process requirements for post-CMOS integration of RF resonators. First, the MEMS fabrication thermal process budget must be carefully designed in order to retain the performance and reliability of the CMOS electronics. Interconnect reliability, rather than transistor performance, limits the post-processing temperature, which should not exceed 450°C. High-quality poly-SiGe structural layers with Ge content greater than ~60% can be deposited by conventional low-pressure chemical vapor deposition without exceeding this temperature limit [3]. Second, the metallization stack of the underlying electronics must be protected from chemical attack during the microstructure release etch. The use of Ge rather than $SiO_2$ as the sacrificial material is advantageous because it can be rapidly etched in a heated $H_2O_2$ solution which does not attack oxide, metal, poly-Si, or poly-SiGe with a Ge content less than ~70%. Third, extremely small (sub-100 nm) electrode gaps are needed in order to achieve low motional resistances, hence low insertion losses [4]. For the definition of nanoscale lateral gaps, a sidewall sacrificial oxide spacer process has already been developed for poly-Si MEMS technology [4]. In this process, the poly-Si electrode layer (which is deposited after the sacrificial spacers are formed) must be etched with high selectivity to the sacrificial oxide, in order to clear it completely along the sidewalls of the structural poly-Si layer in the areas where the electrode layer must be removed. Because Ge etches more quickly (by a factor of ~3) than poly-SiGe or poly-Si in a standard $Cl_2$/HBr dry-etch chemistry, the sidewall spacer process cannot be used if Ge is employed as the sacrificial material, however [5]. Therefore, we have developed a simple Damascene process, featuring unconstrained placement of lateral gaps.

## DAMASCENE GE-BLADE PROCESS

Figure 1 illustrates the fabrication process; scanning electron microscopy (SEM) pictures at various steps are presented in Figure 2. A Si wafer covered with 1-µm CVD-$SiO_2$ was used as the starting substrate. For simplicity, a two-mask process was used. First, a 2-µm-thick *in-situ* boron-doped poly-Ge sacrificial film was deposited by LPCVD (350°C, 2hr deposition) and patterned using i-line lithography. The structures include 0.5µm minimum-width lines to define the transducer's lateral gaps (Figure 1.a). Photoresist ashing in $O_2$ plasma was used to reduce the minimum line width to 50nm (Figure 1.b and Figure 2.a). The photoresist pattern was then transferred to the Ge layer using a $HBr/Cl_2$ chemistry in a transformer-coupled plasma (TCP) etcher. Figure 2.b shows SEM images of a high-aspect-ratio (10~20) Ge blade. Note that sidewall taper in the etched Ge structures, due mainly to a tapered photoresist profile, must be minimized for peak resonator performance. (Sidewall taper is undesirable for the aforementioned sidewall sacrificial oxide spacer process as well.) To avoid any potential adhesion issue for the narrow Ge-blades on $SiO_2$, the Ge was not etched all the way down to the underlying $SiO_2$; rather, a second mask was used to define anchoring contacts to the $SiO_2$ (Figure 1.c). Next, a 2.2µm-thick *in-situ* boron-doped poly-$Si_{0.35}Ge_{0.65}$ structural layer was deposited by LPCVD (425°C, 400mtorr, $SiH_4/GeH_4/B_2H_6$[10% in $H_2$] = 100/60/60sccm, 4hr40min. deposition) as shown in Figure 1.d and 2.c. This deposition step accounts for the majority of the total thermal process budget. Figure 2.d shows that the poly-$Si_{0.35}Ge_{0.65}$ is deposited conformally over the Ge blade. After chemical mechanical polishing (CMP) of the poly-$Si_{0.35}Ge_{0.65}$ layer, the sacrificial poly-Ge layer was removed in $H_2O_2$ at 90°C. Figure 2.e shows an SEM image of a fabricated Double-Ended Tuning Fork (DETF) resonator. Figure 2.f shows a cross-sectional SEM image of the nanoscale gap. Due to high compressive stress and strain gradient in the poly-$Si_{0.35}Ge_{0.65}$ film, the gap is reduced to almost zero and the resonator is vertically displaced from the electrodes by ~100nm, respectively. Optimization of the poly-$Si_{0.35}Ge_{0.65}$ deposition process is underway to minimize these effects.

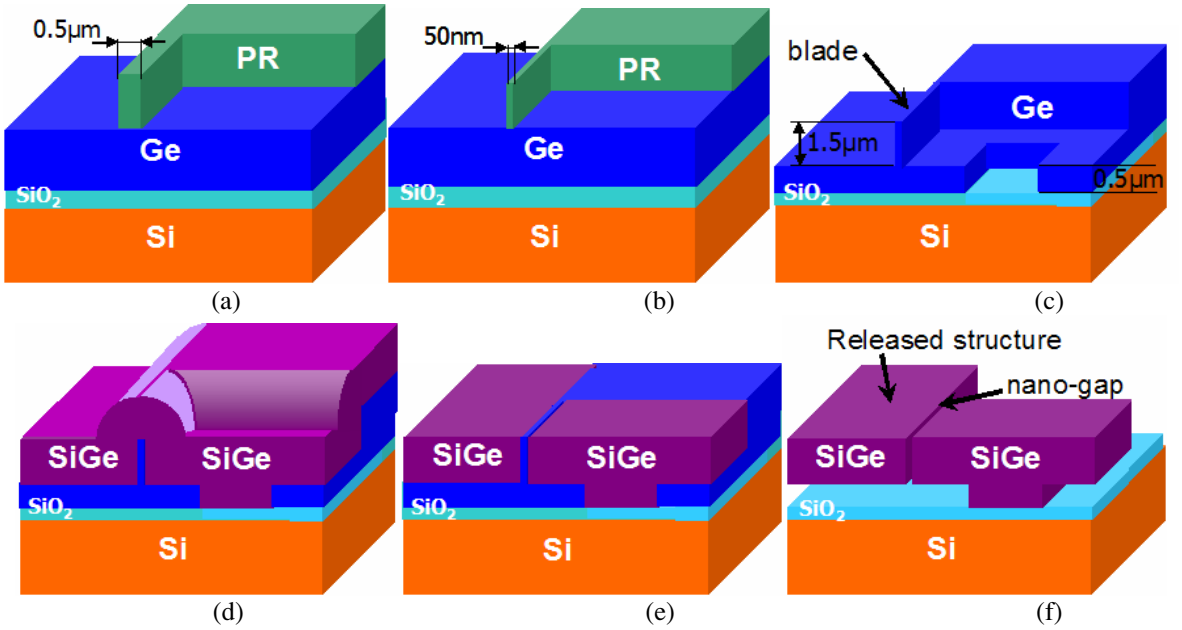



**Figure 1:** Outline of the 2-mask Germanium Blade Damascene Process which provides ultra-narrow gaps.

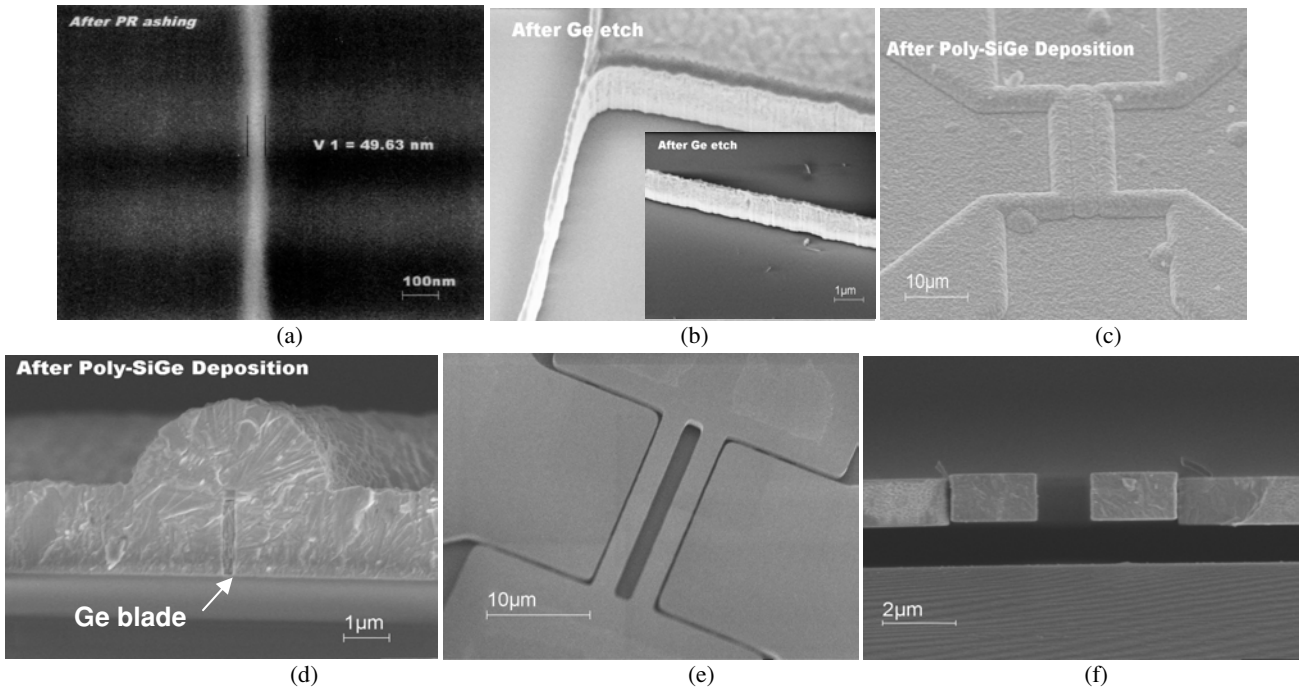



**Figure 2:** SEM pictures corresponding to various steps depicted in Figure 1 in the case of a double-ended tuning fork (DETF): **(a)** 50nm line definition by lithography and photoresist ashing; **(b)** High-aspect-ratio Ge blade; **(c)** top view and **(d)** cross-section after SiGe structural layer deposition; **(e)** Released DETF top view and **(f)** cross-section

This new process provides significant advantages for manufacturing. First, a single deposited layer is used to form the resonator structure and drive/sense electrodes, so that there is no need for a highly selective etch process in order to avoid the formation of unwanted "stringers" along the resonator sidewalls. Because the number of film deposition steps is reduced, the thermal process budget is substantially reduced. Second, nanoscale lateral gaps are achieved by lithographically patterning ultra-narrow lines rather than spaces. Line patterning technology for ~100nm features is well established, as 50nm physical gate-length transistors are now used in products at the 90nm CMOS technology node. This is because the well-controlled formation of ultra-narrow line widths is feasible using photoresist ashing [6] or hard-mask trimming [7] techniques. Also, because of the unique etching characteristics of Ge, the width of a Ge blade after it is formed by dry etching can be further reduced in a controllable manner, in hot (~90°C) deionized water. Finally, the unconstrained placement of lateral gaps is an additional advantage of this method as compared to the sidewall spacer process.

## HIGH-FREQUENCY SIGE DEVICE CHARACTERIZATION

Devices fabricated using the 2-mask damascene Ge-blade process were characterized using various methods:

*2-port measurement method:*

The main problem encountered in testing of MEMS resonators is the feed-through capacitance. Indeed, using direct 2-port measurement of the 24MHz resonator in Figure 2.e, the peak height achievable was only 0.5dB. To address this problem, we used a differential drive/sense scheme as illustrated in Figure 3. The proof mass is used either as a drive or sense element, allowing better efficiency but higher direct feed-through via capacitive transduction. The use of a power combiner/splitter adds flexibility, allowing actuation of both symmetric/asymmetric modes, and providing feed-through cancellation for the asymmetric differential mode in particular.

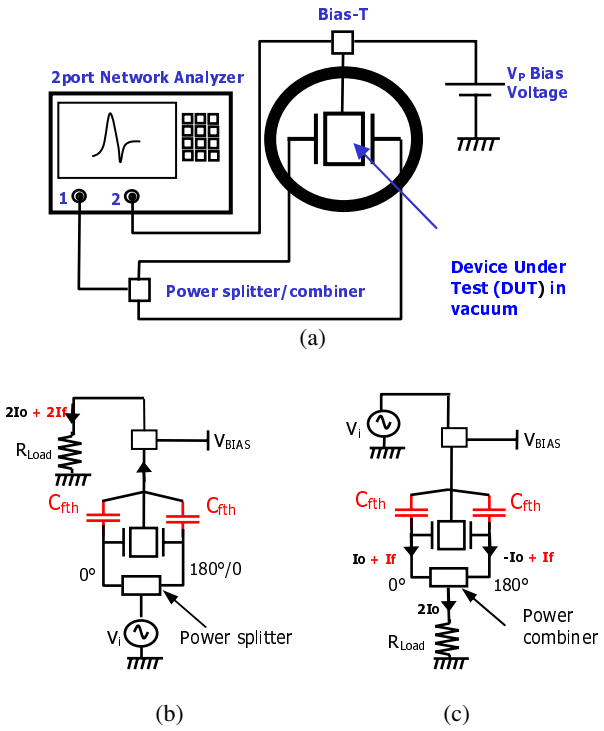



**Figure 3:** (a) Experimental set-up for Transmission Measurement with Differential Drive Configuration (b) and Differential Sense Configuration (c)

Using the differential drive/sense scheme, the transmission characteristic of the same DETF is shown in Figure 4.a, exhibiting a resonance peak increased to 8dB at 24.05MHz, and a quality factor of 4800. Based on frequency pulling extraction, the effective gap was determined to be 295nm, which accounts for the low transduction efficiency. This gap broadening can be attributed primarily to insufficient etch selectivity (of Ge *vs.* $Si_{0.35}Ge_{0.65}$) during the long release etch in $H_2O_2$ [5], which can be remedied by using a structural layer with Ge content below 65%. Poor critical-dimension (CD) control on the blade definition mask may also have contributed to the gap broadening.

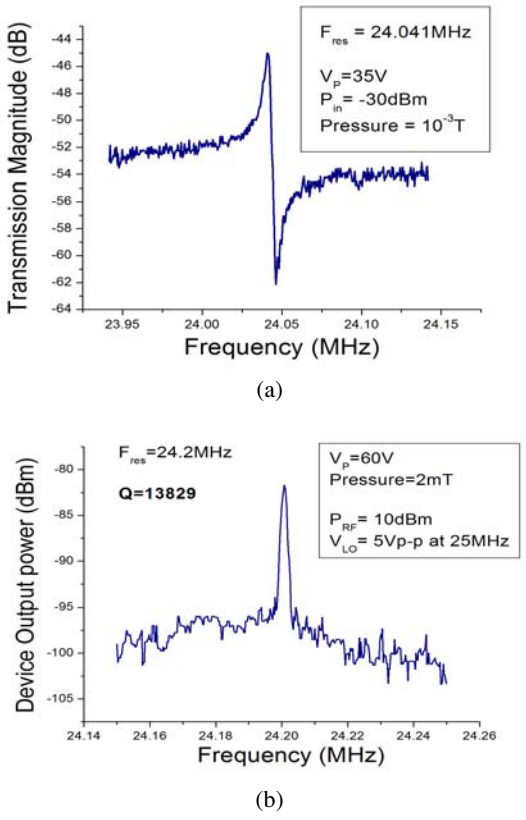



**Figure 4:** Transmission Magnitude of the Double-Ended Tuning Fork shown in Figure 2.e, in the case of Differential Sense Configuration for the asymmetric mode (a), and RF/LO technique for the symmetric mode (b)

*RF/LO technique:*

The RF/LO technique [8] was used to perform characterization of fabricated device at higher frequencies. Indeed, this technique takes advantage of the capacitive non-linearity of the transducer to perform mixing and thus further minimize the influence of any parasitic feed-through in the resonance band.

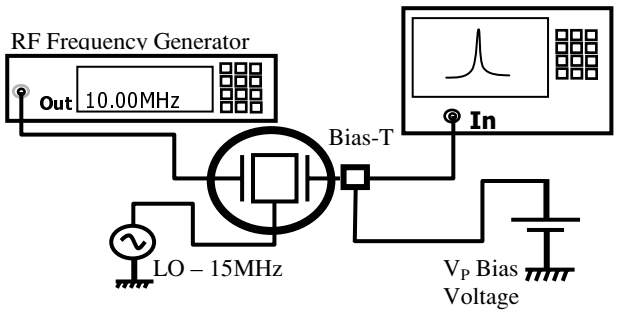



**Figure 5:** Experimental set-up for RF/LO measurement technique

In the case of the 24MHz tuning fork, this technique was used to characterize the symmetric mode and to extract an expectedly higher Q of 13,800 (Figure 4.b).

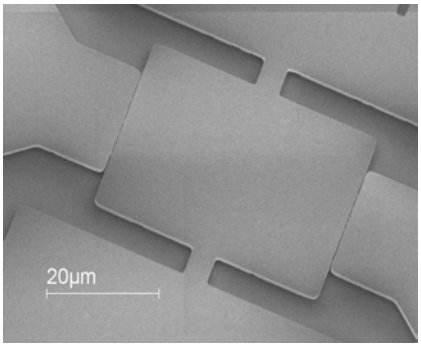
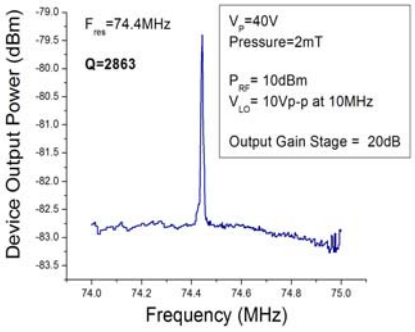
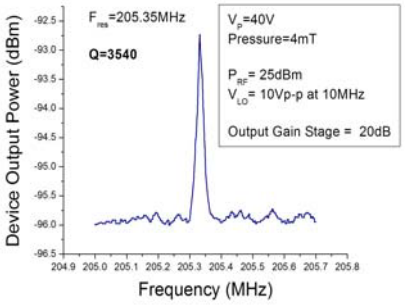



**Figure 6:** SEM picture of bulk-longitudinal resonator.

A 40µm-long and 32µm-wide bulk-longitudinal resonator (Figure 6) was also characterized using this technique. A 74.4MHz resonance was observed for the fundamental mode, while the third harmonic mode was visible at 205MHz, as shown in Figure 7.a and 7.b. The quality factors were measured to be 2,900 and 3,500 respectively.




(a)




(b)

**Figure 7:** Device output power of the Bulk Longitudinal Resonator shown in Figure 6 using the RF/LO measurement technique: (a) Fundamental Mode (b) Third Harmonic

*Temperature Drift:*

Figure 8 presents the temperature dependence of the DETF, which exhibits $TC_F$ = -85ppm/°C, greatly influenced by the compressive stress due to thermal-expansion mismatch between the SiGe structure and Si substrate. Using a simple model, the corresponding $TC_F$ for SiGe was extracted to be -104ppm/°C. On the same plot, a simulated curve shows the benefit of matching the thermal expansion coefficients of the substrate and the structure, resulting in a lower $TC_F$ of -48ppm/°C. Although these values are higher than for poly-Si, it is possible to take advantage of such a mismatch to integrate efficient temperature-sensing structures for compensation purpose.

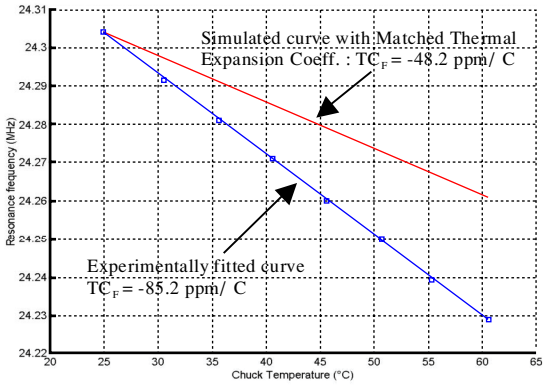



**Figure 8:** Measured and Simulated Frequency dependence versus Temperature for a DETF

## CONCLUSIONS

A new Ge-Blade Damascene Process is proposed and successfully applied to fabricate a high-frequency DETF resonator. Due to its low thermal budget, HF-free release process, and highly-planar surface topography, this new process is promising for post-CMOS integration of nano-mechanical resonators applicable for RF communication systems.

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