Ge-Blade Damascene Process for Post-CMOS Integration of Nano-Mechanical Resonators

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***Abstract*—A novel process is demonstrated for fabrication of high-frequency mechanical resonators applicable for on-chip radio-frequency communication. This Ge-blade damascene process (GBDP) provides ultranarrow lateral gaps using lithographically defined sacrificial Ge blades (high-aspect-ratio Ge features). The use of Ge as the sacrificial material eliminates the need for a hydrogen fluoride etch process to release the mechanical structures, and, hence, simplifies the integration of micro-electromechanical (MEMS) with CMOS circuitry. Polycrystalline silicon-germanium (poly-SiGe) is used as the structural material in order to keep the thermal budget low (maximum temperature 425 °C), so as to be compatible with CMOS metallization stacks. A 24-MHz double-ended tuning fork resonator was successfully fabricated using the GBDP.**

***Index Terms*—Micro-electromechanical (MEMS), resonator, silicon-germanium.**

I. Introduction

MICROMACHINED resonators are promising as on-chip replacements for discrete filters and oscillators which are presently implemented using off-chip quartz and surface-acoustic-wave (SAW) devices in wireless communication systems [1]. The monolithic integration of control, amplification and signal-processing electronics with radio frequency micro-electromechanical devices (RF MEMS) also reduces parasitic capacitances and inductances as well as overall system power consumption. Recent progress toward a low-thermal-budget polycrystalline silicon-germanium (poly-SiGe) MEMS technology promises to make possible the modular cofabrication of high-performance surface-micromachined structures on top of completed CMOS wafers [2]. However, a detailed process integration scheme for poly-SiGe resonator fabrication—particularly one that provides for ultranarrow lateral gaps between the resonator and drive/sense electrodes—has yet to be explored. In this letter, we propose a novel process for post-CMOS fabrication of poly-SiGe RF resonators with sub-100-nm electrode gaps.

II. GBDP Process

There are several process requirements for post-CMOS integration of RF resonators. First, the MEMS fabrication thermal process budget must be carefully designed in order to retain the performance and reliability of the CMOS electronics. Interconnect reliability, rather than transistor performance, limits the post-processing temperature, which should not exceed 450 °C [3]. High-quality poly-SiGe structural layers with Ge content greater than $\sim$60% can be deposited by conventional low-pressure chemical vapor deposition without exceeding this temperature limit[4], [5]. Second, the metallization stack of the underlying electronics must be protected from chemical attack during the microstructure release etch. The use of Ge as the sacrificial material is attractive because it can be rapidly etched in a heated H_2O_2 solution which does not attack oxide, metal, poly-Si, or poly-SiGe with a Ge content less than $\sim$70% [6]. Third, extremely small (sub-100-nm) electrode gaps are needed in order to achieve low motional resistances, hence low insertion losses [7]. For the definition of nanoscale lateral gaps, a sidewall sacrificial oxide spacer process has already been developed for poly-Si MEMS technology [8]. In this process, the poly-Si electrode pattern is formed after patterning the structural poly-Si layer and depositing the sacrificial oxide spacer layer. Hence, the etching of the electrode layer must be performed with very high selectivity to the sacrificial layer, in order to clear it completely along the sidewalls of the structural layer in the areas where the electrode layer must be removed. The required high-etch selectivity is achievable for the poly-Si structural layer and the SiO_2 sacrificial layer. However, since Ge etches more quickly (by a factor of $\sim$3) than poly-SiGe or poly-Si in a standard Cl_2/HBr dry-etch chemistry[9], the sidewall spacer process cannot be used if Ge is employed as the sacrificial material [10].

We propose here a Ge-blade damascene process (GBDP) for integration of poly-SiGe RF resonators with CMOS electronics. This new process defines ultranarrow lateral gaps lithographically, and utilizes a damascene process similar to that which is used for state-of-the-art interconnect technologies[11]. Fig. 1 shows the sequence of the proposed process. After CMOS fabrication is completed, a sacrificial Ge layer is deposited. The Ge is patterned using conventional lithography and etch processes to form $\sim$ 100-nm-wide features, which will eventually define the nanoscale gaps. Then, the Ge layer is partially etched to form a Ge blade (a high-aspect-ratio Ge fin) (i), and the photoresist is removed. Areas where the structural layer will be anchored are then defined by lithography and Ge etching (ii). After the photoresist is removed, the poly-SiGe layer (which forms the resonator structure and the electrodes) is deposited (iii) and planarized by chemical-mechanical polishing (CMP). Finally, the sacrificial Ge is removed in a heated H_2O_2 bath, to release the resonator structure (iv). This new process provides significant advantages for manufacturing. First, a single deposited

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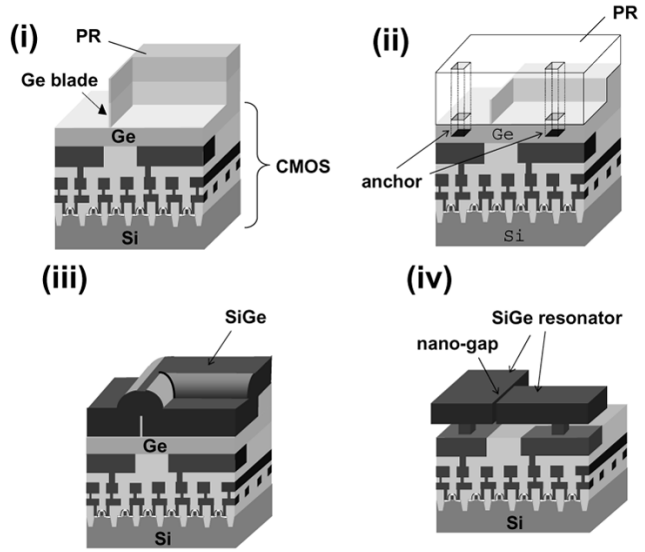

Fig. 1. GBDP sequence.

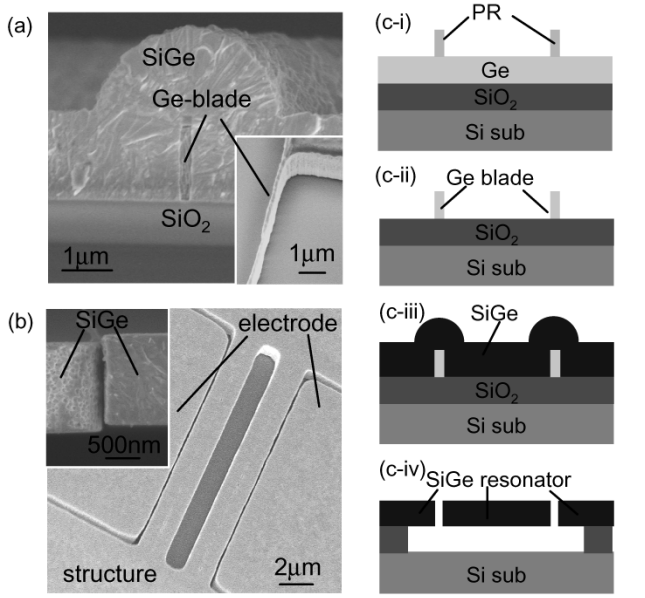

Fig. 2. (a) SEM images of the resonator after poly-$Si_{0.35}Ge_{0.65}$ deposition and after Ge etching (inset). (b) SEM images of the DETF nanoscale gap in perspective view and cross-sectional view (inset). (c-i–iv) Simplified process sequence used in this study.

layer is used to form the resonator structure and drive/sense electrodes, so that there is no need for a highly selective etch process in order to avoid the formation of unwanted "stringers" along the resonator sidewalls. Because the number of film deposition steps is reduced, the thermal process budget is substantially reduced. Second, nanoscale lateral gaps are achieved by lithographically patterning ultranarrow lines rather than spaces. Poly-Si(SiGe) line patterning technology for ~100-nm features is well-established, as 50-nm physical gate-length transistors are now used in products at the 90-nm CMOS technology node [12]. [Unlike transistors which can have complex layout patterns, simple resonator structures do not require the use of optical proximity correction (OPC) techniques. Thus, the cost of the Ge-blade mask can be much lower than that of a CMOS gate-level mask.] In addition, fine tuning of ultranarrow line widths is feasible using resist ashing [13] or hard-mask trimming [14] techniques. Also, because of the unique etching characteristics of Ge[6], the width of a Ge blade after it is formed by dry etching can be reduced in a controllable manner, in hot (~90 °C) deionized water. Finally, the unconstrained placement of lateral gaps is an additional advantage of the GBDP as compared with the sidewall spacer process. Thickness deviation by time-etch of the Ge layer is not of a concern, considering that the final structural thickness does not impact resonance frequencies up to the second order. Compared to SiO_2 sacrificial layers, the adoption of Ge is advantageous in terms of low thermal budgets (350 °C versus 450 °C) and maturity of etching technologies (sub-50-nm line patterning versus ~100-nm hole patterning), and its drawback would be relatively high material costs.

III. Nano-Mechanical Resonator Fabrication

To demonstrate the feasibility of the proposed new process, mechanical resonators were fabricated using a simplified GBDP sequence. For simplicity, a one-mask process instead of the two-mask process (Fig. 1) was used, and an Si wafer covered with 1-μm chemical vapor deposition (CVD)-SiO_2 was used as the starting substrate. A 2-μm-thick *in situ* boron doped poly-Ge layer was deposited as the sacrificial layer by low-pressure CVD (LPCVD) (350 °C, 2 hr deposition). *I*-line lithography and photoresist ashing were used to pattern sub-100-nm lines. Note that sidewall taper in the etched Ge structures, due mainly to a tapered photoresist profile, must be minimized for peak resonator performance. Sidewall taper is undesirable for the sidewall sacrificial oxide spacer process [8] as well. The photoresist pattern was then transferred to the Ge layer using a HBr/Cl_2 chemistry in a transformer-coupled plasma (TCP) etcher. Fig. 2(a) show scanning electron microscopy (SEM) images of a high-aspect-ratio (10–20) Ge blade. No adhesion issue for the narrow Ge-blades on SiO_2 was encountered. Hence, the mechanical stability of the Ge blades should not be an issue for the two-mask process (Fig. 1), in which underlying Ge supports the blades. Next, a 2.2 μm-thick *in situ* boron doped poly-$Si_{0.35}Ge_{0.65}$ layer was deposited by LPCVD (425 °C, 400 mtorr, SiH_4–GeH_4/B_2H_6 (10% in H_2) = 100/60/60 sccm, 4 h, 40 min deposition). This deposition step accounts for the majority of the GBDP total thermal process budget. Fig. 2(a) inset shows that the poly-$Si_{0.35}Ge_{0.65}$ is deposited conformally over the Ge blade. After CMP of the poly-$Si_{0.35}Ge_{0.65}$ layer, the sacrificial poly-Ge layer was removed in H_2O_2 at 90 °C. The simplified one-mask process requires the use of hydrogen fluoride (HF) for the final release (to remove the bottom SiO_2 layer under the poly-$Si_{0.35}Ge_{0.65}$ layer). This HF etch step is not necessary for the two mask process (Fig. 1). The Fig. 2(b) inset shows an SEM image of a fabricated double-ended tuning fork (DETF) resonator[15]. Fig. 2(b) shows a cross-sectional SEM image of the nanoscale gap. Due to high compressive stress and strain gradient in the poly-$Si_{0.35}Ge_{0.65}$ resonator film (by an unexpected process problem of the furnace), the gap is reduced to almost zero and the resonator is vertically displaced from the electrode by ~100 nm, respectively. Fig. 3 shows the resonator's electrical

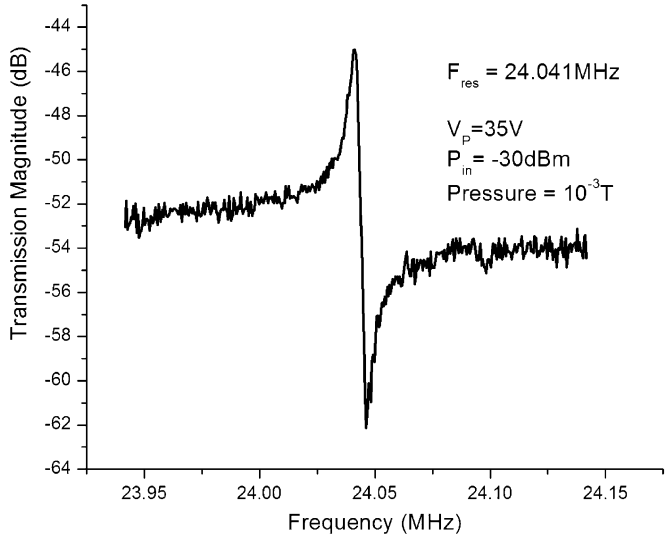

Fig. 3. Transmission spectrum of the fabricated DETF resonator. Measured resonance frequency was 24.04 MHz (versus 24.59 MHz designed frequency). Q was 6000 by differential drive, and 14 000 by a mixing technique [16].

transmission characteristics. Operating in vacuum, the device exhibits an 8-dB peak at 24.04 MHz fundamental resonance frequency. A nanoscale-gap DETF resonator was thus successfully fabricated using the GBDP, for the first time in poly-SiGe MEMS technology. More detailed characteristics of fabricated resonators of other designs yielding higher resonant frequencies will be reported elsewhere [17].

IV. Conclusion

A new GBDP is proposed and successfully applied to fabricate a high-frequency DETF resonator. Due to its low thermal budget, HF-free release process, and highly planar surface topography, this new process is promising for post-CMOS integration of nano-mechanical resonators applicable for RF communication systems, which would realize various kinds of on-chip RF filters and/or on-chip clocks, leading to dramatic improvement of total system performance.

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