Interconnect Issues for Integrated MEMS Technology

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ABSTRACT

This paper reviews recent progress toward the monolithic, modular integration of micro-electromechanical devices (MEMS) with electronics. The interconnect metallurgy poses a thermal budget limit on the processes that can be used to build the MEMS structures after the electronics are completed. In addition, the metal interconnect and inter-metal dielectric layers must be protected during the removal of sacrificial material to release the microstructures. Polycrystalline silicon germanium (poly-SiGe) is a promising structural material, with mechanical properties similar to polycrystalline silicon, which can be conformally deposited by low pressure chemical vapor deposition at temperatures compatible with modern multi-level interconnect technologies. Ideally, it should be possible to form a low-resistance and low-parasitic-capacitance contact directly between poly-SiGe and an underlying metal interconnect. Initial specific contact resistance measurements between p-type poly-SiGe and TiN/Al are reported.

Key words: *heterogeneous integration, MEMS, polycrystalline, silicon-germanium, surface micromachining, interconnect*

INTRODUCTION

Micro-electromechanical devices (MEMS) are presently used in a variety of products for chemical sensing, inertial measurements, and optical switching. Monolithic integration of electronics (used for control, amplification and/or signal processing) with MEMS is desirable for improved microsystem performance and reliability. For the semiconductor industry, the integration of MEMS with electronics represents an opportunity to enhance the performance and/or functionality of integrated-circuit (IC) devices, for example, by integrating high-quality-factor passive components to enable low-cost, low-power RF communications, or by adding sensing and actuating capabilities, or by providing on-chip cooling.

In order to minimize the manufacturing cost of an integrated microsystem, the microstructures should be fabricated in a modular fashion, on silicon wafers with completed complementary metal-oxide-semiconductor (CMOS) circuitry. This paper first describes different approaches to modular integration of MEMS with foundry CMOS electronics. A high-performance, low-process-temperature MEMS technology based on polycrystalline silicon-germanium (poly-SiGe) is then discussed. Initial contact resistance measurements for poly-SiGe films deposited directly onto metal interconnects are presented. Considerations for future interconnect technology development are noted.

MODULAR INTEGRATED MEMS PROCESSES

The most straightforward approach to fabricating MEMS on CMOS wafers is to utilize the metal interconnect and/or inter-metal dielectric ("metallization") layers themselves as the structural materials. For specific applications, such as the MEMSIC dual-axis thermal accelerometer [1], this approach has proven successful. Silicon (Si) is the preferred structural material, however, because of its high mechanical strength (comparable to steel), flexibility and resistance to fatigue. The Single Crystal Reactive Etching and Metallization (SCREAM) process is one approach to post-CMOS fabrication of single-crystalline Si microstructures [2]. In this process, the dielectric layers are patterned and used as a hard mask for deep reactive ion etch (DRIE) of the substrate. Thin-film deposition followed by anisotropic etching is used to form oxide and metal layers on the etched-Si sidewalls, to provide electrical interconnections and to mask the isotropic plasma etch used to release the structures. The metal layers in a standard CMOS technology can also be used as an etch mask to define a single-crystalline Si structural layer as follows: first, DRIE is used to pattern the metal and dielectric layers; then, the patterned stack is used as a hard mask to pattern the silicon substrate; finally, a backside etch is used to release the high-aspect-ratio composite structure [3]. This process has recently been applied to fabricate a lateral accelerometer after completion of the sensing electronics [4]. The multiple electrical interconnects on the mechanical structure enable new approaches to both electrostatic actuation and capacitive position sensing. However, the performance of the composite structure is to some extent impaired by the sub-optimal mechanical properties, such as residual stress, of the interconnect stack.

Oftentimes it is desirable to fabricate MEMS devices directly above the electronics in order to minimize the parasitic resistances and capacitances associated with the MEMS-to-CMOS interconnections which degrade performance. Also, in order to fabricate sophisticated MEMS devices, multiple structural layers are needed; *i.e.* alternating layers of sacrificial material and structural material must be deposited (and patterned) with a total thermal budget which is compatible with the underlying electronics. The Texas Instruments Digital Micromirror Device™ is a commercial product which employs an array of over 10^6 tilting mirrors fabricated using a modular process in which sputtered metals are used as structural layers for the micromirror structures and deep-UV-hardened photoresist is used for the sacrificial layers [5]. An oxygen plasma is used to release the mirrors, which eliminates stiction problems. For high-frequency resonator/filter applications, a large ratio of the Young's modulus to density, E/ρ, is required. Composite structural layers can be formed from a standard inter-metal dielectric layer (which provides the large E/ρ needed to achieve a high resonant frequency) together with a standard metal layer (which provides the electrical conductivity needed for electrostatic actuation). This approach has recently been proposed for the fabrication of vertically resonating cantilever-beam RF filters, with process steps added to a standard BiCMOS process only for the sacrificial layer etch and vacuum encapsulation [6].

Polycrystalline silicon (poly-Si) films have excellent mechanical properties and are commonly used in MEMS sensors. Over the past decade, the development of MEMS foundry processes (*e.g.* SUMMiT™ [7] and MUMPS® [8]) based on poly-Si surface micromachining has stimulated the design of various standard mechanisms, actuators, and position sensors. It is therefore highly desirable to develop a low-temperature equivalent to poly-Si surface micromachining technology, to allow for modular fabrication of MEMS on completed CMOS wafers while leveraging existing MEMS foundry processes and industry design experience.

POLY-SIGE SURFACE MICROMACHINING TECHNOLOGY

Recently, the application of poly-SiGe films as structural and sacrificial layers for surface micromachining has been investigated [9]-[11]. Poly-SiGe is attractive for modular integration of MEMS with electronics, because it can be deposited at much lower temperatures than poly-Si films [12] and yet has excellent mechanical properties [13].

Deposition of poly-SiGe films by LPCVD

SiGe films are deposited in a conventional LPCVD reactor, using germane (GeH_4) as the germanium source gas, in addition to silane (SiH_4) or disilane (Si_2H_6) as a silicon source gas; phosphine (PH_3) or diborane (B_2H_6) can be used for *in-situ* doping. The alloy composition in the deposited film is dependent on the gas-flow ratio, deposition temperature, and deposition pressure. For a given deposition temperature, the film deposition rate increases with increasing Ge content in the film [12], due to the higher surface reaction rate of germane. It should be noted that the transition temperature between amorphous and polycrystalline film deposition is lowered with increasing Ge content, from ~550°C for pure Si to ~300°C for pure Ge. As-deposited polycrystalline films are preferred for MEMS applications, because their residual stress after annealing tends to be lower and more reproducible. In addition, amorphous films are not conductive as needed for most MEMS applications. In order to obtain as-deposited polycrystalline SiGe films at deposition temperatures less than 450°C, the Ge content should be greater than 50 atomic percent. *In-situ* doped p-type poly-SiGe films deposit rapidly at low temperatures (Figure 1) and have adequate conductivity without post-deposition annealing [14].

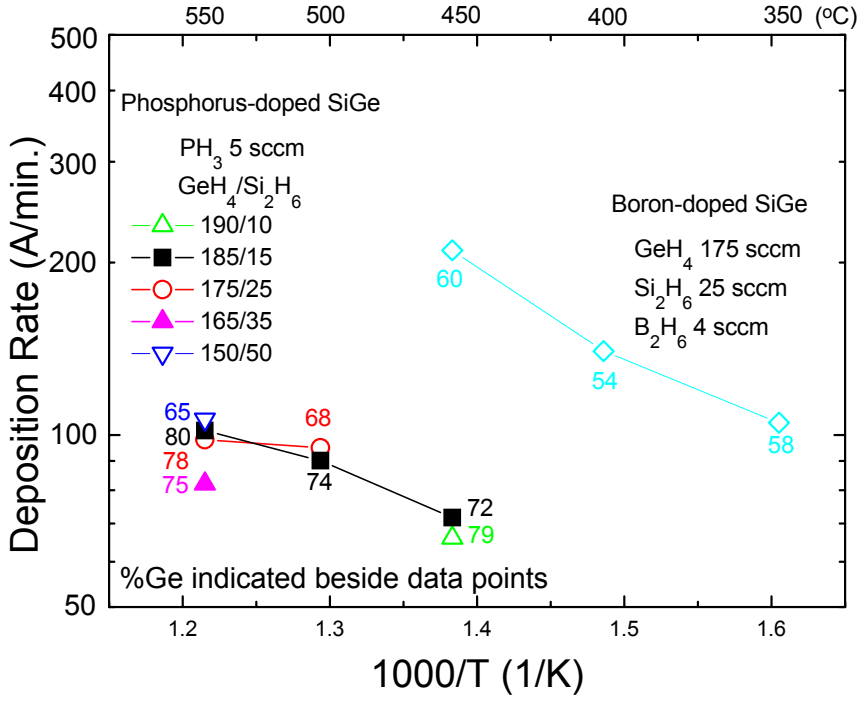

Figure 1: Arrhenius plot of deposition rate *vs.* temperature, for *in-situ*-doped poly-SiGe films deposited in a conventional LPCVD furnace using disilane and germane source gases at 300 mTorr pressure [14].

Poly-SiGe film properties

Poly-SiGe films can be patterned using standard poly-Si etch processes with fluorine-based or chlorine-based chemistries [12]. Germanium does not form a stable oxide and hence it can be easily etched in an oxidizing ambient or chemical solution, which makes the stability of Ge-rich SiGe films problematic. The etching behavior of SiGe films in heated hydrogen peroxide (a strongly oxidizing solution) has been reported [15]. High etch rates were found for films with Ge content greater than ~75%, while negligible etch rates were found for films with Ge content less than ~70%. For low-temperature fabrication of MEMS, then, the optimal Ge content lies between 50% and 70%.

Low residual stress and low strain gradient are desirable to minimize dimensional changes and out-of-plane bending in the microstructures upon release. Poly-$Si_{0.4}Ge_{0.6}$ films deposited at 450°C and 600 mT have low residual stress (-9 MPa, compressive) and low strain gradient (2.4×10^{-5} μm^{-1}) [16]. The deposition rate for these process conditions is 0.6 μm/hr, which indicates that a high-quality structural layer (typically >2 μm thick) can be deposited within several hours. The mechanical quality factor of as-deposited poly-SiGe has been found to be comparable to that of high-temperature-annealed poly-Si [13].

Electrical contact between poly-SiGe and metal interconnect

The development of a low-temperature deposition process for high-quality structural films is only one of several steps toward developing a post-CMOS integrated MEMS technology. Process-integration issues must be addressed in order to achieve a high-yield MEMS process that is independent of the details of the particular CMOS technology. For example, a scheme for forming robust electrical interconnections between the MEMS and CMOS is needed. Poly-Si surface micromachining technologies typically employ a poly-Si interconnect layer (often referred to as the "poly-Si_0" layer) deposited on an electrically insulating layer that is not removed during the structure-release etch. This interconnect layer is used to route signals to and from drive and sense electrodes and is also used as an electrostatic shield between suspended structures and the silicon substrate. For a post-CMOS surface micromachining process, a "poly-$SiGe_0$" interconnect layer can be deposited directly on the uppermost CMOS passivation layer through which contact openings have been formed (Figure 2). In modern CMOS technologies, the metal interconnects are typically coated with a thin diffusion barrier material such as TiN or TaN. Deposition of doped poly-SiGe films onto these barrier materials with resulting low contact resistance is necessary for straightforward connection between the MEMS and CMOS.

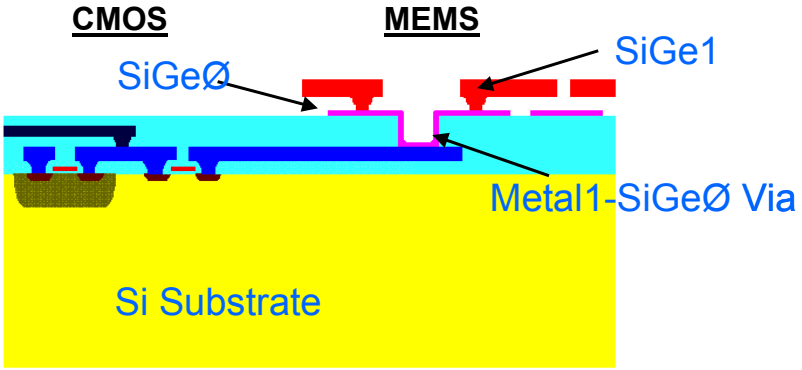

Figure 2: Schematic cross-section of poly-SiGe MEMS to CMOS interconnect scheme.

An experiment was conducted to determine the specific contact resistivity, ρ_c, for p-type (~1 mohm-cm) poly-$Si_{0.4}Ge_{0.6}$ deposited onto TiN-coated Al-2%Si. Standard Kelvin test structures were fabricated on oxidized Si wafers for measurement of contact resistance (Figure 3). After deposition and patterning of the metal and oxide layers, the wafers were subjected to an argon (Ar) plasma treatment followed by a dilute HF dip just prior to SiGe deposition in a conventional LPCVD furnace. Test structure fabrication was completed by patterning the SiGe. Scanning electron microscopy was used to determine the actual contact-hole size, in order to accurately calculate ρ_c. The average value of ρ_c was found to be in the range 2-5 μohm-cm^2, and it did not increase significantly for poly-SiGe deposited at 400^{o}C *vs.* 450^{o}C. These results confirm that poly-SiGe can be deposited directly onto TiN to form a low-resistance contact with an underlying CMOS metal interconnect.

Sacrificial material considerations

Another process integration issue is the protection of the CMOS metallization layers during the release-etch of the sacrificial layer(s). If LPCVD SiO_2 is used as the sacrificial material, as in poly-Si surface micromachining technologies, then HF is used as the release etchant. In this case, an HF-resistant, electrically insulating layer must be deposited on top of the CMOS metallization layers prior to the MEMS interconnect layer, to protect the CMOS layers during the release etch. Amorphous silicon was used for this purpose in an initial demonstration of the post-CMOS integration of poly-Ge structures [17]. A more elegant solution is to entirely avoid the use of HF as a release etchant, by using an alternative sacrificial material. Since poly-SiGe films with Ge content greater than ~75% can be etched at very high rates in heated (70^{o}C-90^{o}C) hydrogen peroxide solution, Ge-rich (>75% Ge) films or pure Ge can be used as a sacrificial material [18]. Hydrogen peroxide is an ideal release etchant, because it is benign to SiO_2, Si_3N_4, Si and many metals, so that a protective layer for the CMOS metallization layers is not necessary.

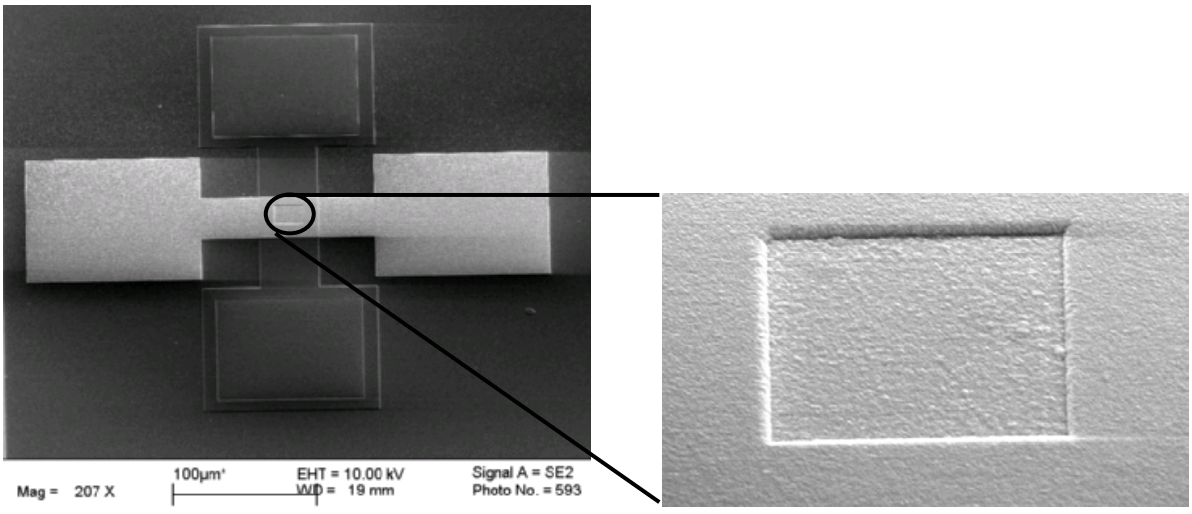

Figure 3: Scanning electron micrographs of **(a)** Kelvin test structure used for contact resistance measurements, and **(b)** close-up view of poly-$Si_{0.4}Ge_{0.6}$/metal contact (5μm x 5μm). The poly-$Si_{0.4}Ge_{0.6}$ was deposited at 450^{o}C and 600 mT for 50 minutes, using SiH_4, GeH_4 and B_2H_6 source gases; it is ~1 μm thick and has ~1 mohm-cm resistivity.

Integrated poly-SiGe MEMS process

The fabrication of p-type poly-SiGe microstructures on top of standard CMOS electronics has already been successfully demonstrated [19]. The thermal budget for the MEMS process was approximately 3.5 hours at 450°C for the p-type poly-SiGe layers and 3 hours at 375°C for the poly-Ge sacrificial layer. No significant changes in the CMOS transistor characteristics or in the Al-2%Si interconnects were observed. Figure 4 shows a scanning electron micrograph of a audio-range poly-SiGe resonator fabricated on top of its transresistance sense amplifier. This integrated device was verified to be functional; its mechanical quality factor was measured to be ~31,000 at 20 kHz [13].

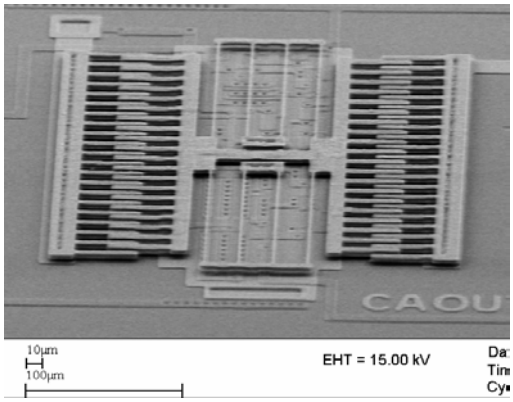

Figure 4: Scanning electron micrograph of a 3 µm-thick, p-type poly-SiGe comb-drive resonator fabricated on top of a CMOS transresistance amplifier with Al-2%Si interconnects [19].

DISCUSSION

Although a 0.35 µm CMOS technology with aluminum interconnects and tungsten plugs has been found to be able to withstand significant thermal processing (temperatures up to 525°C for more than 1 hour) [20], duration limits for various "annealing" temperatures (*e.g.*, 400-450°C) are not known for modern CMOS technologies employing copper metallization and low-permittivity inter-metal dielectrics. This information is needed in order to establish the thermal budget allowance for a post-CMOS MEMS technology, which may involve multiple LPCVD steps for multiple structural layers. If allowable, rapid thermal annealing at moderate temperatures (~600°C) can be used to improve the mechanical properties of low-temperature-deposited poly-SiGe films [13]. Pulsed (~30 ns) excimer-laser annealing can minimize the thermal exposure of the underlying electronics and is also effective for improving the mechanical properties of poly-SiGe films [16].

CONCLUSION

MEMS technology promises to enhance the functionality and/or performance of IC devices, to dramatically expand the semiconductor market. Low-temperature MEMS fabrication processes are being developed for modular integration with electronics. In particular, surface-micromachining technology using p-type poly-SiGe as a structural material and poly-Ge as a sacrificial material is attractive because it can leverage existing MEMS manufacturing and design infrastructure. "MEMS-last" process compatibility should be a consideration for research and development of interconnect technology in the future.

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