

# GPS SAW Filter Using A Wafer level Technique

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**Abstract**— A wafer-level assembled SAW filter on 36Y-X LiTaO<sub>3</sub> with a size of 1.6x0.8 mm<sup>2</sup> is presented. The SAW filter has six solder balls with a size of 0.25 mm diameters. The reason of the use of the 0.25 mm balls is that it is easy to mount the devices onto a printed circuit board using a conventional placement machine. The SAW filter is designed for a GPS RF stage application and has a center frequency of 1.5 GHz. The frequency characteristics of the SAW filter are almost the same as the ceramic packaged SAW filter. An insertion loss of 1.1 dB was obtained. Furthermore, a smaller SAW filter with 1.0x0.8 mm<sup>2</sup> in size is demonstrated.

*Keywords*; Assembly, Wafer Level, SAW filter, GPS;

## I. INTRODUCTION

Miniaturization is one of the driving design goals for large number of wireless applications. Such designs have called for small size radio frequency (RF) stage SAW devices. In order to achieve miniaturization, some assembly technologies have been studied. The assembly technologies for RF stage SAW filters have been changed from wire-bonding to face-down-bonding and the size of SAW filters has been dramatically reduced. In 1994, a thermo-sonic face-down-bonding technique for SAW devices was published and a 950MHz SAW filter with 3.2x2.5x0.9 mm<sup>3</sup> in size was released [1]. A chip with 2.1x1.4x0.35 mm<sup>3</sup> in size was placed in a ceramic cavity package. This technology enables to attach the gold bumps of the SAW chip on gold metallized pads of the ceramic package at a temperature below 200 degrees centigrade [1,2]. Since then, the size of SAW filters has been reducing to 2.5x2.0mm<sup>2</sup> [3], 2.0x1.6mm<sup>2</sup> and 1.4x1.1mm<sup>2</sup> [4]. However, in general, ceramic cavity packages or ceramic substrates have been still needed for SAW filters. On the other hand, some wafer-level assembly techniques which do not need any package substrates have been developed for not only silicon based integrated circuit devices but also SAW devices [5-8]. The wafer-level assembly enables package-less SAW filters and has a great advantage of eliminating some conventional complex die-by-die processes [9].

This paper describes a wafer-level assembly technique for RF stage SAW filters. In a wafer-level assembly, we can get the completed devices after a dicing process. The completed devices have an air-cavity above the interdigital transducers (IDTs) and some lead-free solder bumps to mount the devices onto printed circuit boards (PCBs) directly. There are two important processes for our wafer-level assembly. One is a sacrificial layer technique to achieve air-cavities above the

active area on the device. The other is an electroless plating technique to mount solder balls on bonding pads of the wafer.

## II. WAFER-LEVEL ASSEMBLY TECHNOLOGY

### A. Assembly process

A conventional assembly process and a wafer-level assembly process are shown in Fig.1 and Fig. 2, respectively. In a conventional assembly, after dicing, we need to admit die-by-die processes such as die-bonding, wire-bonding and encapsulating processes. The die-by-die process needs a long process time to complete the products. On the other hand, in wafer-level assembly, we can handle the products on wafer level in all processes including encapsulating and bumping of electrical terminals. So the wafer-level process needs a short process time to complete the products. After dicing process, there are no other complicated manufacturing processes.

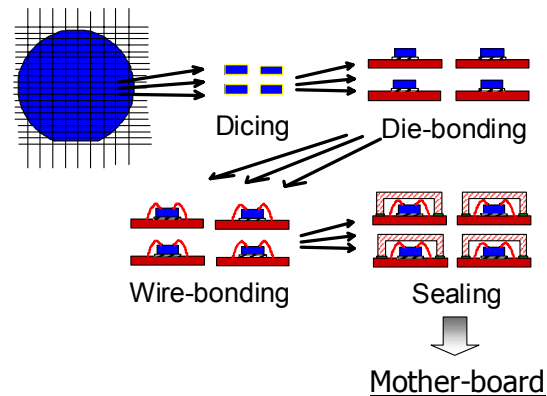


Fig.1. Conventional assembly process.

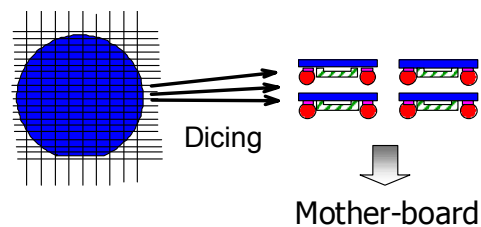


Fig. 2. Wafer-level assembly process.

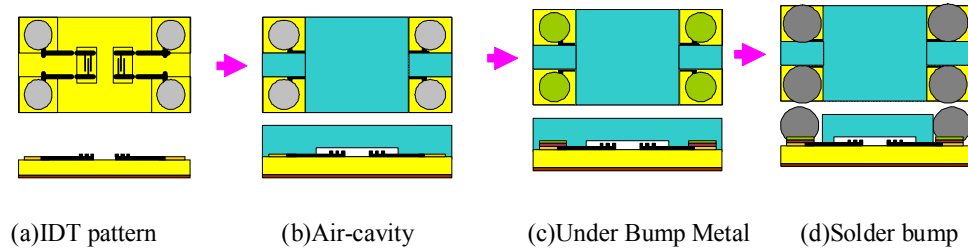


Fig. 3. Wafer-level assembly process using sacrificial layer and solder bump.

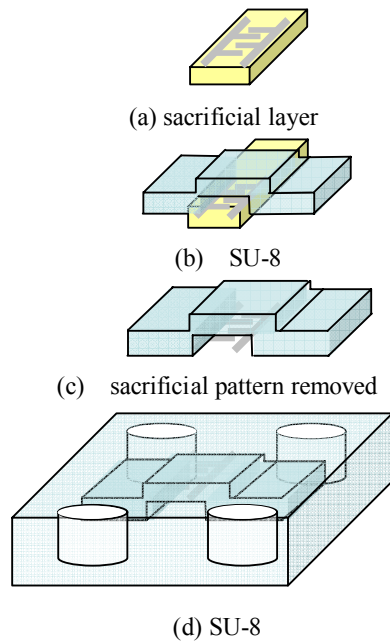


Fig.4. Process flow for air-cavity.

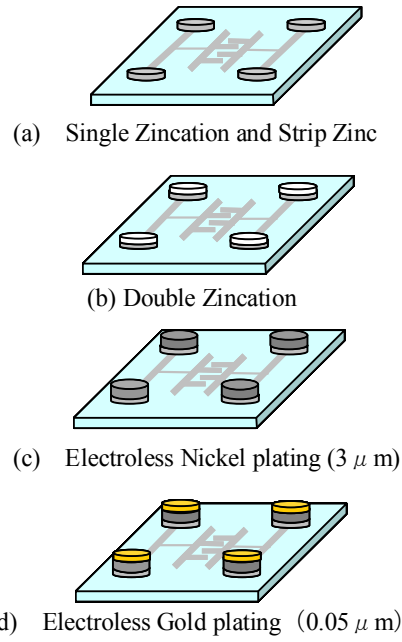


Fig.5. Process flow for Under Bump Metal.

The wafer-level process is shown in Fig. 3; (a) conventional photo-lithography for IDT patterns, (b) air-cavity by a sacrificial layer technique, (c) under bump metal by an electroless plating technique, (d) bumps using Sn/Ag/Cu solder balls.

### B. sacrificial layer technique

No package material may touch the active area of the SAW devices because this would damp the acoustic waves. So ceramic cavity packages were used in flip-chip SAW devices [1,3]. Sacrificial layer techniques on wafer-level have been widely used in MEMS devices to realize air-gap or air-cavity. There are some reports of SAW and BAW devices utilizing a sacrificial layer technique [6,8]. In order to achieve an

air-cavity above the active area of a device on wafer-level, we developed a sacrificial layer technique for SAW devices.

A sacrificial material was spun onto the structured wafer where the IDTs have already been patterned. A standard photo-resist was spun onto the sacrificial layer. Then the desired sacrificial patterns were obtained by a conventional photo-lithography technique. The sacrificial patterns were covered with the photo-epoxy SU-8 from Nippon Kayaku Co.,Ltd. by a photo-lithography technique, as shown in Fig. 4 (b). Then the sacrificial patterns were removed by an organic solvent and air-gaps above the IDTs were obtained as shown in Fig. 4 (c). Then the air-gaps were covered with another photo-epoxy SU-8. The areas for the solder bumps were opened and the air-cavities above the active areas of the SAW device were obtained as shown in Fig. 4 (d).

### C. Under bump metal

In conventional flip-chip assembly for SAW devices, gold stud bumps have been widely used. The gold stud bumps can provide some advantages, it is easy to form the bumps using conventional gold-wire bonding machines and it is perfectly dry and clean process. However, the gold stud bumping process needs a long process time in the case of a large number of bumps on a wafer. On the other hand, solder bump process can provide an advantage of a short process time even though for a large number of bumps. Furthermore, if the finished wafer-level SAW devices have solder bumps, we can handle SAW devices as well as other components such as chip inductors, capacitors and resistors using a conventional placement machine. It is a great advantage on wafer-level SAW devices with solder bumps.

In order to utilize solder bumps, we need an under bump metal on the aluminum bonding pads of the SAW wafer. In our wafer-level process, we utilized an electroless plating technique [10] on aluminum bonding pads on SAW wafers. Aluminum is the popular metal in SAW devices but aluminum oxide is easy to form on the aluminum surface. The direct plating of electroless nickel on aluminum surface can be difficult. We utilized an under bump metal process as shown in Fig. 5. The zincation process aims to activate the surfaces of aluminum bond pads. After the double zincation, a nickel layer with a  $3 \mu\text{m}$  thickness was obtained by electroless nickel plating. Then a gold layer with a  $0.05 \mu\text{m}$  thickness was obtained by electroless gold plating.

### D. Solder Bumps

A metal mask which has a large number of apertures was used. The apertures of the metal mask are positioned to correspond to the bonding pads of the wafer. The metal mask is aligned with the wafer and the Sn/Ag/Cu solder balls are placed onto the bonding pads of the wafer through the apertures of the metal mask. After an IR reflow, we can get solder bumps on the wafer as shown in Fig. 6.

## III. GPS SAW FILTER WITH $1.6 \times 0.8 \text{ mm}^2$ IN SIZE

In the first stage, we tried a GPS SAW filter with  $1.6 \times 0.8 \text{ mm}^2$  in size using our wafer-level assembly process. In general, a conventional placement machine can handle the dies having the solder bumps of larger than  $0.25 \text{ mm}$ . So the die size was designed with  $1.6 \times 0.8 \text{ mm}^2$ . A photograph of the completed SAW device using the wafer-level process is shown in Fig. 7 (a). The SAW device with solder bumps was directly placed onto the evaluation PCB and reflowed. The photograph is shown in Fig. 7 (b). The measured frequency responses are shown in Fig. 8. The insertion loss of  $1.1 \text{ dB}$  was obtained and the insertion loss was almost the same with a ceramic packaged SAW filter. On the other hand, stop-band characteristics around the center frequency are different due to parasitic impedances as shown in Fig.8 (b). The stop-band characteristics are strongly affected by the evaluation PCBs as well as the IDT design [3]. Even though we molded the die on the PCB by an epoxy resin, no significant change of the frequency responses was observed.

## IV. GPS SAW FILTER WITH $1.0 \times 0.8 \text{ mm}^2$ IN SIZE

The active area including the IDTs is too small for the die area of the  $1.6 \times 0.8 \text{ mm}^2$  sized SAW filter. So we can reduce the size. A photograph of the  $1.0 \times 0.8 \text{ mm}^2$  sized SAW filter is shown in Fig. 9. There are four solder bumps with  $0.2 \text{ mm}$  diameter. Since the SU-8 can be transparent, we can see the IDT pattern through the SU-8 layer above the IDTs. The frequency responses of the completed wafer-level GPS SAW filter with  $1.0 \times 0.8 \text{ mm}^2$  in size were almost the same as the SAW filter with a ceramic package with the same die.

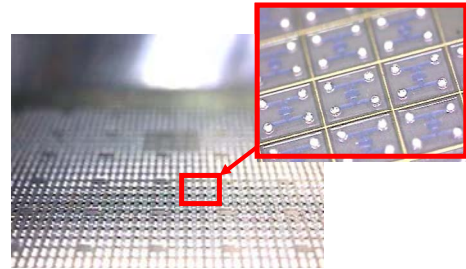
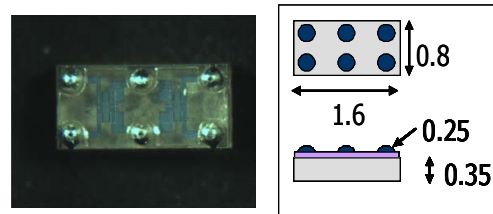
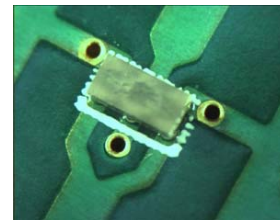


Fig. 6. Photograph of solder bumps on wafer.

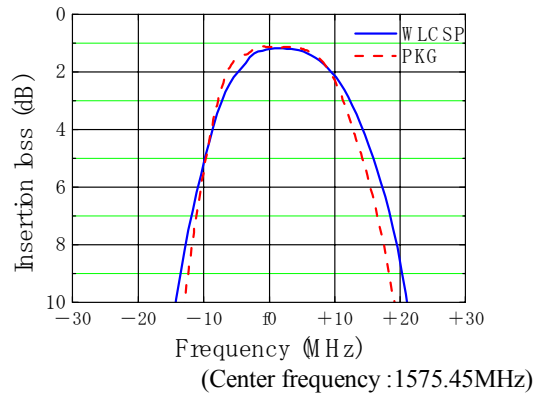


(a) Wafer-level SAW device with solder bumps.

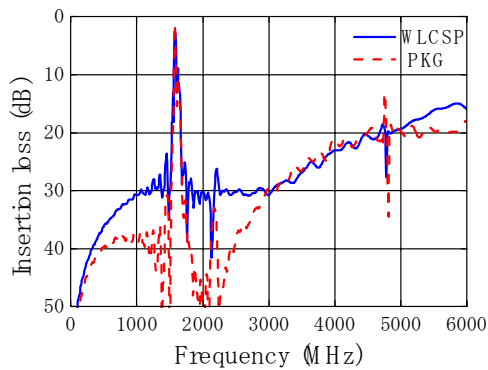


(b) Wafer-level SAW device on evaluation PCB.

Fig. 7. Photographs of  $1.6 \times 0.8 \text{ mm}^2$  wafer-level SAW.



(a) Narrow-band frequency response.



(b) Wide-band frequency response.

Fig. 8. The measured frequency responses.

Figure 10 shows the SEM photographs of the bumps with a diameter of 0.2 mm and 0.1 mm on the wafer-level SAW device. Since the thickness of SU-8 layer is thin enough, we can use solder bumps with a diameter of 0.1 mm. Then we can reduce not only the foot print area of SAW devices but also thickness. If we used a substrate with a thickness of 0.2 mm and solder bumps with a diameter of 0.1 mm, we could realize a SAW device with a thickness of 0.3 mm.

## V. CONCLUSION

A wafer-level GPS SAW filter with a center frequency of 1.5 GHz on 36Y-X LiTaO<sub>3</sub> with a size of 1.6x0.8 mm<sup>2</sup> is presented. The SAW filter has six solder bumps with a size of 0.25 mm diameters. An insertion loss of 1.1 dB was obtained. Furthermore, a smaller wafer-level assembled SAW filter with 1.0x0.8 mm<sup>2</sup> in size is demonstrated. The smaller SAW filter has only four solder bumps with 0.2 mm diameters. The wafer-level assembly technique can be a strong driving force to expand SAW applications and suitable to system-in-package applications.

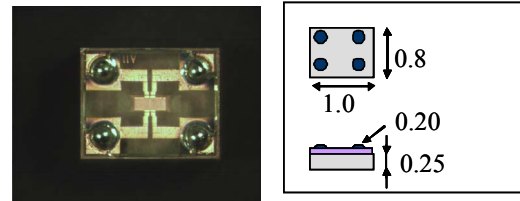


Fig. 9. Photographs of 1.0x0.8 mm<sup>2</sup> wafer-level SAW device.

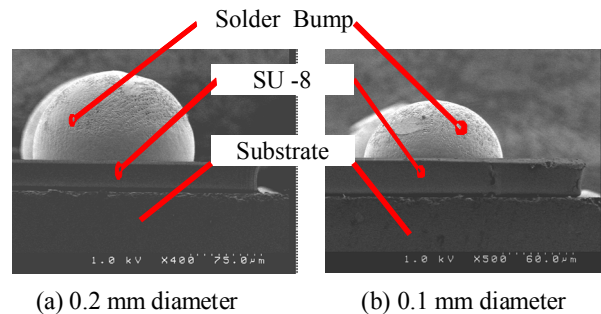


Fig. 10. SEM photographs of solder bumps.

## REFERENCES

- [1] H. Yatsuda, T. Horishima, T. Eimura and T. Ooiwa, "Miniaturized SAW filters using a flip-chip technique", in Proc. IEEE 1994 Ultrason. Symp., pp. 159-162, 1994.
- [2] H. Yatsuda and T. Eimura, "Flip-chip assembly technique for SAW devices", Intl. Journal of Microcircuits and Electronic Packaging, vol. 19, 3, pp. 238-244, 1996.
- [3] H. Yatsuda, "Modeling of parasitic effects for flip-chip SAW filters", in Proc. IEEE 1997 Ultrason. Symp., pp. 143-146, 1997.
- [4] O. Kawachi, K. Sakinada, Y. Kaneda and S. Ono, "Packaging of SAW devices with small, low profile and hermetic performance", in Proc. IEEE 2006 Ultrason. Symp., pp. 2289-2292, 2006.
- [5] J. Lim, J. Hwang, J. Kwon, S. Ham, W. Kim, T. Kim, W. Jeung, S. Yang, S. Choi and J. Park, "An ultra small SAW RF filter using wafer level packaging technology", in Proc. IEEE 2006 Ultrason. Symp., pp. 196-199, 2006.
- [6] B. Wilkins, "Wafer level packaging of SAWs enables low cost 2.5G and 3G Radio Modules", in Proc. Third Int. Symp. on Acoustic Wave Devices for Future Mobile Communication Systems, pp. 179-184, 2007.
- [7] R.C.Ruby, A.Barfknecht, C.Han, Y.Desai, F.Geefay, G.Gan, M.Gat, T.Verhoeven, "High-Q FBAR Filters in a Wafer-Level Chip-Scale Package", IEEE ISSCC 2002 conference, Feb.2002
- [8] M.Franosch, K.-G.Oppermann, A.meckes, W.Nessler, R.Aigner, "Wafer-Level-Package for Bulk Acoustic Wave (BAW) Filters" IEEE MTT-S-SD gest 2004, pp.493-496.
- [9] H. Yatsuda, "SAW device assembly technology", in Proc. Int. Symp. on Acoustic Wave Devices for Future Mobile Communication Systems, pp. 189-194, 2001.
- [10] Xiao-Chen Fu, Guo-Wei Xiao, Pui-Chung Law, Philip Ching Ho chan, "The Effect of Pretreatment Process on Electroless Nickel Bumping for Different Al Pads", Solid-State and Integrated Circuits Technology, 2004. Proceedings. 7th International Conference on, Vol.1, Oct. 2004, pp. 603-606.