AN ULTRA-LOW COST DEEP REACTIVE ION ETCHING (DRIE) TOOL FOR FLEXIBLE, SMALL VOLUME MANUFACTURING

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ABSTRACT

Our goal is to demonstrate that we can achieve a radical reduction in the capital cost of micro/nano-manufacturing without sacrificing performance by scaling production throughput. As a demonstration of this concept, we show for the first time a DRIE system that processes small substrates ($\sim$1 in^2) with performance comparable to commercial systems for a capital cost below $32K. We have designed, built and tested this system, which currently can achieve silicon etch rates up to 2.8 μm/min with vertical sidewall profiles, an estimated photoresist selectivity greater than 50:1, and etch depth non-uniformity to less than 2% across the substrate.

KEYWORDS

Fabrication, MEMS, Dry Etching, DRIE, Bosch Process, Low Cost, Accessibility

INTRODUCTION

A general rule of thumb for new semiconductor fabrication facilities (fabs) is that revenues from the first year of production must match the capital cost of building the fab itself. With modern fabs routinely exceeding $1 billion to build [1], this rule serves as a significant barrier to entry for small entities seeking to develop or commercialize new semiconductor devices. This barrier is especially formidable for those groups whose devices are targeted towards smaller market segments or those which require exotic materials or nontraditional process sequences. Even if one chooses to exploit an older, fully depreciated fab, the economics of maintaining the facility can outweigh the market being served by the product.

The foundry fab model has arisen partially to overcome this inefficiency, but to remain profitable, these foundries typically offer only a few standardized processes that limit customer customization. The limited diversity afforded by these foundries can make some devices with smaller market sizes economically viable, but many devices (particularly in the MEMS sector) require process customization beyond the level currently offered by commercial foundries. Lastly, product development time can be significantly lengthened when the fabrication occurs remotely from the product development team.

To address these problems, we are working to create a suite of tools that processes 1-2" (25-50 mm) diameter substrates, or approximately a 1 in^2 area. By moving against the trend of larger and larger substrates we will be reducing throughput, but gaining significant advantages in capital costs and flexibility. Our overall goal is to accept a reduction in throughput that is proportional to the reduction in capital costs while maintaining comparable performance to a larger tool. Thus, the $\sim$50x reduction in area incurred in moving from modern day MEMS substrate sizes (8" wafers) to 1 in^2 substrates would be offset by a similar reduction in capital costs (i.e. going from a $\sim$$1M tool to a $\sim$$20K tool). This suite of small substrate tools (known colloquially as the 1" Fab) will enable modern processing techniques, but do so at a fraction of the cost of tools aimed at larger substrates. We anticipate a full set of tools for product development and small-scale production to cost $\sim$$1M and require less than 50 ft^2 of space (thus fitting in a large laminar flow hood). This is compared to >$1B and more than 50,000 ft^2 for a new 8" (200 mm) fabrication facility. In addition to the reductions in equipment cost and required space, a 1" Fab will also use significantly less materials and reagents, require far less energy to operate, and have lower environmental impact.

The total throughput possible in the 1" Fab certainly cannot compete with a typical MEMS fab, but for the vast majority of devices that currently struggle to find a cost-effective solution for development and small-scale production, the throughput advantages of large fabs are not needed. For these devices, the cost savings of the 1" Fab platform and its ability to quickly prototype designs far outweigh any expansion in future production schedules. Furthermore, by using standard process technologies, there is a path to transfer production to large scale facilities should future product volumes demand it.

THE 1" FAB DRIE

As a step towards demonstrating the viability of the 1" Fab concept, we chose to develop a deep reactive ion etcher (DRIE). We chose a DRIE tool because it is arguably one of the most complex pieces of fabrication equipment, requiring precise control of both deposition and etching within a single process in a vacuum environment. In addition, with the use of a modularized tool design, a DRIE tool could be easily adapted to produce other plasma-based fabrication tools (like PECVD and RIE). Our DRIE system, shown in **Figure 1**, is $\sim$10" $\times$ 10" $\times$ 24" (25 cm $\times$ 25 cm $\times$ 60 cm) (not including the peripherals or electronics).

SYSTEM DESIGN

As its name suggests, the 1" Fab DRIE has been designed to etch substrates with an area on the order of 1 in^2. This substrate size was chosen for the 1" Fab because many MEMS devices, which are the initial target of the 1" Fab platform, have die sizes less than 1 in^2 (645 mm^2). Additionally, accounting for future expansion into conventional semiconductor processing, most CMOS dies
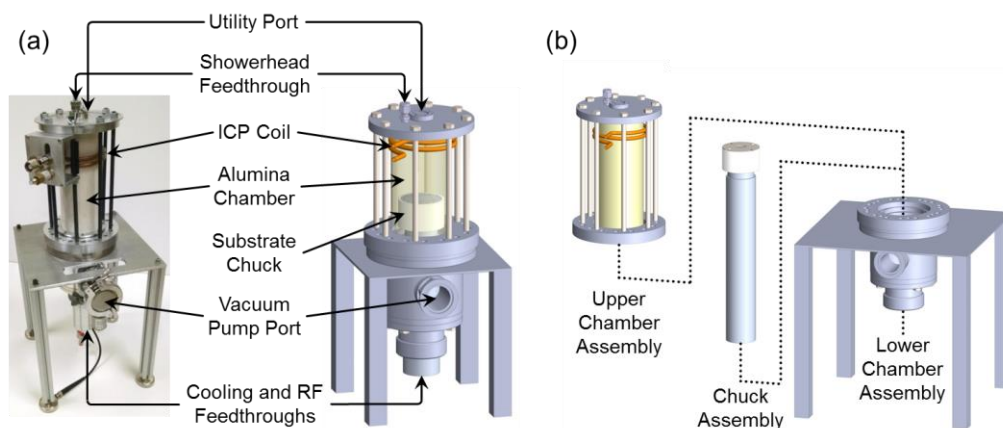
Figure 1: The 1" Fab DRIE. (a) shows a picture and rendering of the system (RF shielding removed for viewing purposes). (b) shows the three modules of the vacuum chamber platform and how they connect to one another.

also fall into the sub-1 in^2 category, as the largest common exposure fields for 8" (200 mm) i-line steppers are on the order of 1 in^2.

The 1" Fab DRIE was designed as part of a modular platform for vacuum-based fabrication tools. The three main modules of this platform are the upper chamber assembly, the lower chamber assembly, and the chuck assembly. **Figure 1b** shows these three modules as designed for the 1" Fab DRIE. As a whole, the etcher is built in a traditional ICP-RIE configuration, with the etching and deposition plasmas generated by an ICP coil and then selectively accelerated toward the substrate using a powered lower electrode (as in an RIE system). A high-level block diagram of the 1" Fab DRIE system is shown in **Figure 2**.

The upper chamber assembly for the 1" Fab DRIE houses the gas showerhead for distributing the process gas, and a two turn helical coil for generating inductively coupled plasma. A central utility port in the uppermost flange is included for monitoring and diagnostic purposes. We have used it for Langmuir probe measurements of plasma density and as a viewport for making spectroscopic measurements. For other tools, the upper assembly could include PVD sources like a sputtering target or alternative

plasma generation sources like a planar ICP coil.

The lower chamber assembly provides mechanical support for the system as well as the vacuum port and a compression fitting-based feedthrough for the substrate chuck assembly. The upper and lower chamber assemblies mate together with a ConFlat-style knife-edge-on-gasket seal. Rugged elastomeric gaskets are used to allow multiple open and close cycles without loosening or tightening bolts. This mating system also allows the easy incorporation of a load lock and transfer arm, which can be inserted at the interface between the upper and lower assemblies to allow samples to be loaded without breaking vacuum in the chamber.

The chuck assembly is designed such that process connections are isolated from the vacuum in the chamber. The 1" Fab DRIE chuck assembly has connections for RF power, chilled water, helium (unused thus far), and temperature measurement. The type or number of these connections can be modified to fit different applications, such as heating instead of cooling for certain CVD applications. Substrates are mounted mechanically on the top of the assembly, which can accommodate square, round, and irregularly shaped wafers up to 2" (50 mm) across.

The use of a compression fitting in the lower chamber assembly also conveniently enables the chuck assembly to be translated up and down within the vacuum chamber, enabling variable spacing between the plasma generation zone and the substrate, as well as allowing the chuck to be easily retracted fully into the lower chamber assembly for the load-lock configuration described above.

System Cost

Our current version of the 1" Fab DRIE was built for less than $32,000 in parts and labor. This number comprises ~$5,800 for the materials (and labor) associated with building and assembling the physical etching chamber and vacuum system, and ~$25,800 for all of the associated peripherals like RF generators, pumps, and mass flow controllers. The dominance of this cost by peripherals, particularly in the RF power and impedance matching section, is something we are actively working to decrease
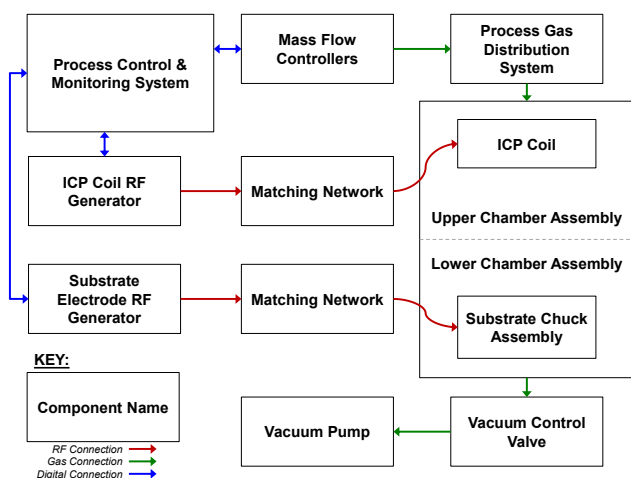

Figure 2: Block diagram of the 1" Fab DRIE System.

through targeted development of generators and matching networks that more closely fit the requirements of the 1" Fab tools. These savings would be partially offset by additions of critical features like the load lock assembly and further improvements to the system's overall conductance and gas throughput, but overall, we are confident that we can attain a total system cost that approaches a tool price in our target range of $20K (we do not account for potential licensing costs).

RESULTS

In order to characterize the performance of the 1" Fab DRIE, a variety of experiments have been performed to test the stability and practical limits of the system. Measurements of the system's etching performance using SF_6+O_2 and time-multiplexed Bosch Process dry etching recipes are reported on specifically below.

SF_6+O_2 Etching

The first step taken to understand and quantify the etching performance of the 1" Fab DRIE system was to construct a response surface model for the simple, yet well understood SF_6+O_2 silicon etching recipes. In this system, an SF_6 plasma is generated to produce a source of fluorine radicals and ions, which chemically etch silicon through the formation of volatile silicon tetrafluoride (SiF_4) molecules and physically etch via sputtering [2]. After exploratory testing to establish a realistic process window, a three parameter, five level response surface test structure was constructed and carried out. The mass flow rates of SF_6 and O_2, and the applied power to the substrate electrode (base power) were the three parameters chosen for the test sequence. The response surface for etch rate as a function of SF_6 and O_2 flow is shown in **Figure 3**.

This response surface shows that the etch rate increases with increasing amounts of SF_6, and increases up to a point with the addition of O_2. These results match well with the existing literature on SF_6+O_2 etching [3–5]. The synergistic
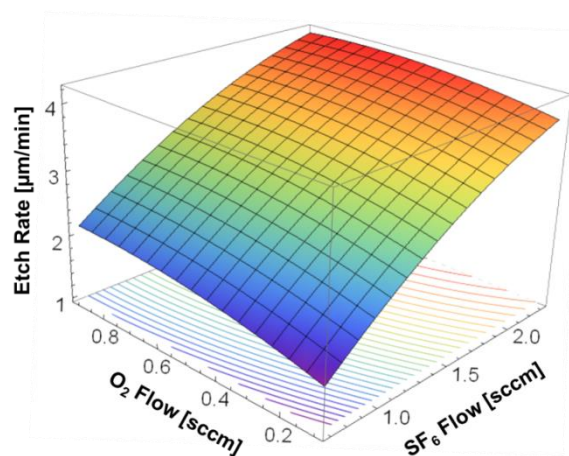
Figure 3: The response surface for etch rate in the 1" Fab DRIE using the SF_6+O_2 chemistry. The surface was plotted using the base power center point value of 10 W.

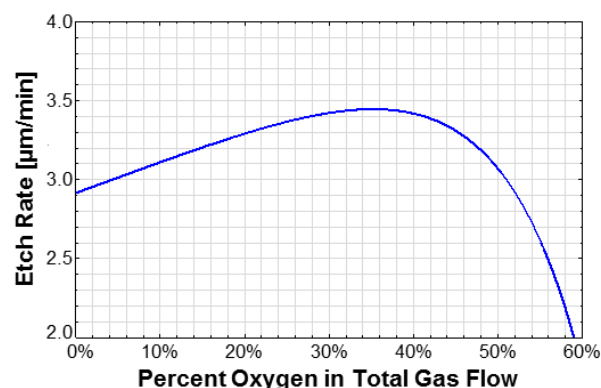Figure 4: The etch rate in the 1" Fab DRIE as a function of the percentage of O_2 in the SF_6+O_2 etch gas mixture. The curve was formed by evaluating the fitted response surface equation at the center point values of 1.5 sccm SF_6 and 10 W base power.

effect of adding O_2 to an SF_6 plasma, which increases the number of fluorine radicals, has been well documented [3,5] and can be seen in **Figure 4**, which plots the fitted response surface equation for etch rate as a function of the percent oxygen in the total process gas (relative mass flows).

Bosch Process DRIE

After gaining an understanding of the capabilities and limits of the 1" Fab DRIE using SF_6+O_2 etching recipes, tests of the system's etching performance using the time-multiplexed Bosch Process were conducted. The Bosch Process is a technique for achieving high-aspect ratio features with a vertical sidewall profile. These etch profiles are achieved by alternating between etching using SF_6 and depositing a conformal passivation layer using C_4F_8. The passivation layer inhibits etching of the sidewalls, encouraging an anisotropic profile [6].

A variety of initial tests have been performed to begin narrowing the process window for Bosch Process etching in the 1" Fab DRIE. The results of these tests are described below.

To determine the repeatability and uniformity of the system, a series of five samples were etched using the same parameters for a total of 30 minutes each. The samples used were patterned to expose ~52 µm wide features and had a total open area of ~40%. This high open area was used to stress uniformity, as higher open areas have been observed to produce greater cross-wafer non-uniformity [7,8]. **Figure 5** shows a profile and cross-sectional view of one of the five samples. The average etch rate observed across the five samples was 1.6 µm/min, with sample to sample variations up to 7% from this average. The variation of etched depths within an individual sample was observed to be much lower, on the order of 1-2% over the middle 85% of the substrate. The sidewall profiles for each sample were reasonably uniform, with angles ranging from 90° to 92° (slight over-etch). Accurate measurements of photoresist selectivity have not yet been made, but we estimate it to be in the range of 50:1 to 100:1.
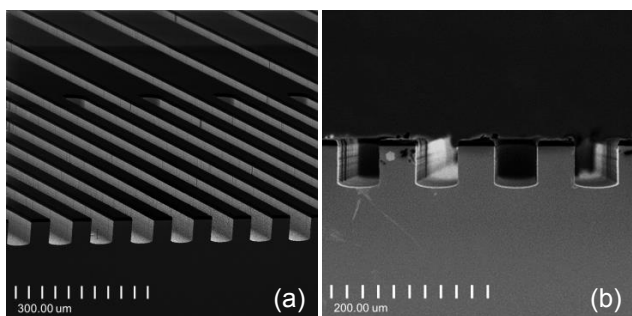
Figure 5: (a) Profile and (b) cross-sectional views of a sample from the DRIE repeatability test.

Figure 7: Profile views of samples with (a) >50% open area (1.1 μm/min) and (b) ~5% open area (2.8 μm/min).

Several etches were also performed to explore the system's ability to maintain anisotropic profiles over higher aspect ratios. The sample shown in **Figure 6** has ~8 μm wide gaps and was etched to a depth of 55 μm (1.65 μm/min) for an aspect ratio of ~7:1. We are currently exploring longer etch times and larger aspect ratio etches.

Looking a bit closer at **Figure 6**, it is clear that the shape and size of the DRIE scallops is reasonably consistent over the full depth of the trench, but local variation still exists from scallop to scallop. We attribute much of this to some observed variability in our C_4F_8 MFC, which we are currently retuning.

Through our early tests we have also encountered two of the phenomena inherent to dry etching, RIE lag and loading [7,9]. The samples reported on thus far have all had large fractions of open, etchable area, which due to the loading effect resulted in decreased etch rates. To contrast the results of these high open area samples, we etched several patterns that have ~5% open area. These wafers etched much faster, with rates of up to 2.8 μm/min using similar parameters. **Figure 7** compares two samples with very different loading fractions.
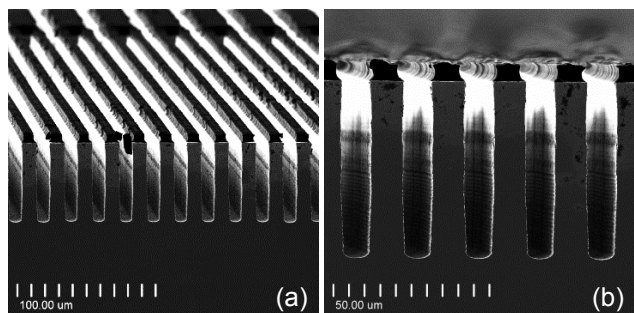

Figure 6: (a) Profile and (b) cross-sectional view of a higher aspect ratio (~7:1) etch.

CONCLUSIONS

We have demonstrated a 1" DRIE which costs less than $32K. The modular and inexpensive design of the tool itself provides a level of flexibility and interchangeability that will be helpful for the development of processes and devices using different materials and unique etch and deposition processes. There is still much that can be done to improve 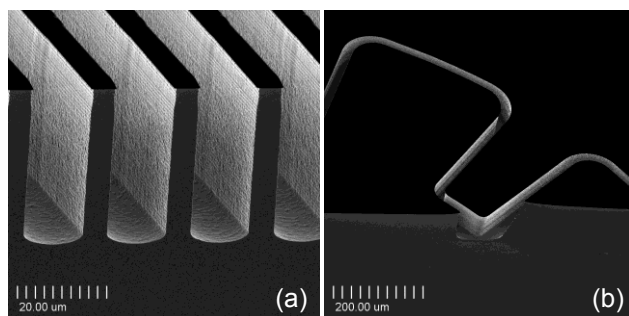the tool's performance, namely optimization of the vacuum system and improvements to the stability of the gas delivery system. We also believe that further reductions to the overall system cost can be realized by developing new lower cost RF power delivery systems that better match the power requirements of a small system like the 1" Fab DRIE. Overall, we believe this demonstrates a viable path for achieving radical reductions in the capital costs for micro/nano-manufacturing.

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