COMPACT NEMS FPGA DESIGN FOR HARSH ENVIRONMENT AND LOW POWER REQUIREMENT

Sijing Han[1], Vijay Sirigiri[1], Daniel G. Saab[1] , Faisal K. Chowdhury[2], and Massood Tabib-Azar[2]
[1] EECS Case Western Reserve University, Cleveland, Ohio 44106
[2] EE University of Utah, Salt Lake City, Utah 84112

ABSTRACT

We present implementation of field-programmable gate array (FPGA) using new NEMS devices that can be configured to implement any 2-input basic logic gates using a single structure [3]. This enables the implementation of 2 mechanical delays for 4-input compact Configurable Logic Block (CLB). These NEMS CLBs use only nine NEMS, instead of 150 switches used in CMOS, and provide a programmable interconnect that minimize power. NEMS devices are generally larger, slower, and less reliable than their CMOS counter parts. Our approach of realizing a logic gate within a single device structure reduces the number of switches needed to implement logic gates improving reliability, reducing the real estate and delay. In FPGA's the programming is usually done once and the resulting functionality constitute the desired outcome. Thus, the NEMS mechanical delay is minimized and given the reduced leakage power of NEMS, it presents a considerable advantage over CMOS.

KEYWORDS: FPGA, Radiation, High Temperature, NEMS.

INTRODUCTION

Field Programmable Gate Array (FPGAs) with faster time to market, simpler design cycle, ability to reprogram and low (non-recurring) cost are evolving continuously. FPGAs dates back to the evolution of programmable read-only memory (PROM) and programmable logic devices (PLDs) and can implement any logic that can be implemented using application specific ICs (ASICs). Increasing IC cost, technical complexity and less reliability issues are among the primary concerns which are motivating the research to develop sophisticated FPGAs. FPGAs have high logic density and sophisticated features such as embedded processors, DSP blocks, to name a few. However, it is well known that FPGA offers flexibility in design at the cost of lower performance, larger area and higher power consumption when compared to their ASIC counterparts. It was observed that in FPGA programmable interconnection [1] and routing resources consumes significant energy at the cost of offering design flexibility. The work by Kuon and Rose [2] compared 90nm FPGAs to ASICs and found FPGAs consume 7-14 times more dynamic power and 5-87 times more leakage power than ASICs. The focus of this paper is to introduce a new ultra-low power FPGAs based on new NEMS switches capable of efficient realization of both the logic and rounting blocks. Because of our innovative NEMS switch [3], we are able to implement a logic block using only nine NEMS switches that can be configured to realize any of the four inputs basic gates (AND, OR, NAND, NOR, XOR, XNOR, NOT) with 2 mechincal delays. A 4 input CLB requires more than 150 CMOS traditional switches. By reducing the number of devices, our approach improves yield, reproducibility and speed and simplifies implementation. NEMS switches are actuated electrostatically and have very low leakage current ($<10^{-9}$ A), very low On resistance (0.1-1 Ω), and moderate speed (1-10 ns) and have turn-on voltages of 1-3V.

In this study, the impact of using NEMS devices in realizing FPGAs is investigated. NEMS provides very compat LUT and extreemly efficient programmable interconnect. NEMS FPGA power is studied at both spice and architectural levels using VPR[18].

In section 2 we discuss background work. In section 3 we presents NEMS device structures followed by section 4 where NEMS digital logic gates and memory designs are discussed. In section 5 we discuss FPGAa followed by section 6 where experimental setup and results are discusse. Conclusions are presented in section 7.

BACKGROUND

Designing energy efficient FPGAs has become quite important in FPGA-based portable systems whew low power and energy consumption can lead to increased battery life and reduced costs of cooling. FPGA's growing logic density and the possibility of usage in high-speed applications and more complex designs coupled with FPGAs high power consumption have resulted in a need for better FPGAs with lower power consumptions. It is reported that routing resources consume significant amount of power at the cost of offering programmability to the design [2]. Past research work had presented several low power FPGA solutions which can be primarily categorized in to device-level and circuit-level optimization effort. Device level optimization includes triple-oxide approach, dual V_{th} process, low-k dielectric. On the other hand, circuit level optimization include clock and power gating, dual V_{dd} etc. Each of these techniques has its own implications on area and performance [4-15].

It is very hard to design CLB's using traditional NEM replacing each CMOS switch with a NEM switch. NEMS switches require large area (10's of μm^2 as opposed to sub-micron sizes of CMOS), and have excessive delay (μs to ms as opposed to ps-ns) during computation cycles. This is why work reported in [14,15 and 6] limits the use of NEMs to the design of routing blocks and [6] uses them for power gating in CMOS. In our proposed FPGAs, NEMS are used for both the switching and the CLB blocks. Using our devices, a four-input CLB requires only nine switches and at most

two mechanical delays per computation. This CLB requires more than 150 traditional switches/devices and much more than 2 mechanical delays per computation. By reducing the number of devices, our approach improves yield, reproducibility and speed and simplifies implementation. But the most important contribution of our single-device logic gate is its improved reliability in the context of mechanical switches.

NEMS DEVICE DESIGN

The NEMS devices developed in our groups is a

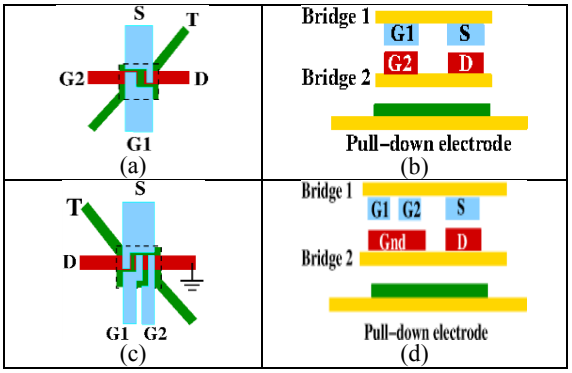

Figure 1: (a) Top view of XOR NEMS; (b) Cross sectional view of XOR NEMS; (c) Top view of AND NEM; (d) Cross sectional view of the AND NEMS.

metallic switching device shown in Fig. 1 with two Gates (G1 and G2), a drain electrode (D), a source electrode (S), and a test electrode (T). Figure 1 (a) and (b) depicts the top-view and cross sectional view of

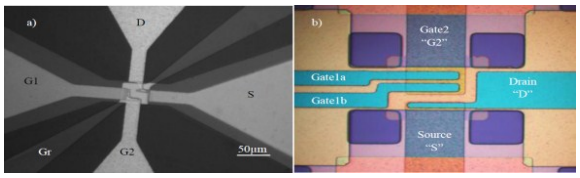

Figure 2: Fabricated NEMS gates (a) XOR. (b) AND.

basic XOR NEMS switch. The switch consists of two bridges, *bridge 1* and *bridge 2*. *Bridge 1* is on the top and *bridge 2* is on the bottom. The input gate G1 and the source switch source S are on bridge 1. The input gate G2 and the drain of the switch are on bridge 2. The Source and Drain are not connected when potential difference applied between G1 and G2 is less than s less than pull-in voltage $V_{pull\text{-}in}$. In this state, the switch is considered to be OFF as there is no conducting path between Source (S) and Drain (D). The switch conducts when the potential difference between G1 and G2 is greater than the $V_{pull\text{-}in}$ voltage. In this state as there is a low resistance connection path between Source and Drain terminals. This switch is ON or conducting, when the voltage on (G1,G2)={(low, high),(high,low)}. The switch is OFF or non-conducting when the voltage on (G1,G2)={(low,low), (high,high)}. This switch conducts when the inputs voltages on G1 and G2 are exclusively different (XOR function).

Figure 2 (a) and (d) depicts the top-view and cross sectional view of the basic AND NEMS switch. The switch consists of two bridges, bridge *1 and bridge 2*. The input gates G1, G2 and the source are on *bridge 1*. The ground (Gnd) and the drain of the switch are on *bridge 2*. The source and drain are not connected when potential difference between G1 and the Gnd or G2 and

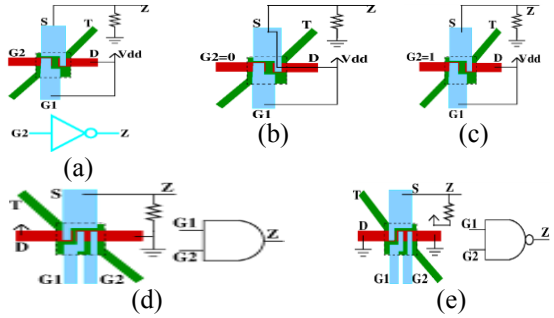

Figure 3: NEMS basic gates; (a) Inverter; (b) Inverter input=0; (c) Inverter input=1; (d) AND; (e) NAND.

the Gnd is less than the pull-in voltage $V_{pull\text{-}in}$. In this state, the switch is considered to be OFF as there is no conducting path between source(S) and drain(D). The switch conducts when the potential difference between G1 and Gnd (V_{G2}) and the potential difference between G2 and Gnd (V_{G2}) are greater than the $V_{pull\text{-}in}$ voltage. In this state as there is a low resistance connection path between source and drain terminals. This switch is ON or conducting, when the voltage on (G1,G2)={(high, high)}. The switch is OFF or non-conducting when the voltage on (G1,G2)={(low, low), (low,high),(high,low)}. This switch conducts when the inputs voltages on G1 and G2 are both high which is an AND function. These AND and XOR switch forms the basis building blocks for the NEMS FPGA.

Dimension of NEMS, coupled with material properties determines NEMS characteristics. In this work we used NEMS which are manufactured to operate

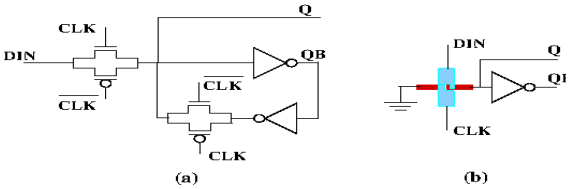

Figure 4:D-latch (a) CMOS; (b NEMS

between 1 and 3V with respective leakage currents of 1e-10 and 1e-16; $V_{pull\text{-}in}$ voltages between 0.75V and 2.6V respectively and switching speeds of between 1ns and 10ns.

The fabrication process flow is described in [16]. Figure 2 shows an SEM image of the XOR and a microscope image of the AND gate. The common implementation of XOR uses 8 individual switches. The factor 8 reductions in device count and associated reduction in number of moving parts and areas lead to 8 times better reliability, at least 4 times faster gate speed and proportionately higher yields.. A 4-input XOR gate compresses the device count by x24.

DIGITAL NEMS DESIGN

Using the XOR and AND NEMS switches, we have designed basic logic gates such as AND, NAND, INV, XOR, XNOR, BUFF. These gates are designed using a single NEMS switch as oppsed to 4 or more with CMOS. As a result, the design area is reduced and the system reliability is improved.

An inverter can be constructed from one XOR NEMS switch. As shown in Figure 3(a), and XOR NEMS switch and pull-down resistor are used to construct the inverter. Input G1 of the XOR NEMS switch is connected to V_{dd} and the output Z is connected to a pull-down resistor and to the source (S) of the switch. When the input G2=0 F, G1 and G2 are at a potential difference causing and electrostatic force that makes the two bridges attracts. This attraction causes the source and the drain to be connected. In this case, the output Z is connected to V_{dd} and the output is '1'. This is shown is Figure 5(b). When the input G2=1, the output is pulled-down to zero (Z=0) by the resistor. This case is shown in Figure 3(c).

The AND gate can be constructed from a single AND NEMS switch and a resistor. The structure of the AND gate is shown in Figure 3(d). In this figure, the drain of the AND switch is connected to V_{dd} and the output Z is connected to the source (S) and the pull down resistor to Gnd. Note, that in this configuration, when both G1=G2=1 causes an electrostatic force that attracts the two bridges. In this case, the output is connected to V_{dd} (Z=1). In all other cases, the drain (D) and the source (S) are not connected and the output is pulled down to zero (Z=0) by the resistor. The NAND gate is shown in Figure 3(e). Similarly, OR, NOR, XOR and XNOR gates can be constructed.

NEMS offers indefinite latching capability. NEMS, once configured to be ON or OFF, can remain in that state indefinitely. This facilitates high integration density and low power by getting rid of (a) any feedback circuits present in latches; (b) SRAM cells in FPGA which holds the configuration bits. The 'ON' resistance of NEMS switches is much lower than the 'ON' resistance of CMOS which reduces delay. Moreover, the absence of SRAM configuration switches reduces area and power. Figure 4(b) illustrates a D latch design using NEMS constructed out of an Inverter and one NEMS switch. This D-latch design does not require any feedback network and transmission gates as in Fig. 4(a).

FPGA BACKGROUND

Figure 5 shows an island style FPGA consisting of islands of logic blocks, switch blocks and connection blocks and routing tracks. Routing tracks are the individual vertical and horizontal line segments that run throughout the FPGA architecture. These routing tracks are grouped together in channels and number of routing tracks present in each channel is determined by the channel width (W_c) which remains identical in X and Y directions in uniform FPGAs. Connection blocks connect the logic blocks to F_c number of tracks in the channel. Switch blocks connect the logic elements by connecting appropriate horizontal and vertical tracks. F_s specify max number of other tracks that each track can connect to. A logic block (as in Figure 6(a)) is made up of interconnection switch matrix and N number of basic logic elements (BLEs). Interconnection matrix performs connections between BLEs during logic implementation. A BLE (Figure 6(b)) whose size is

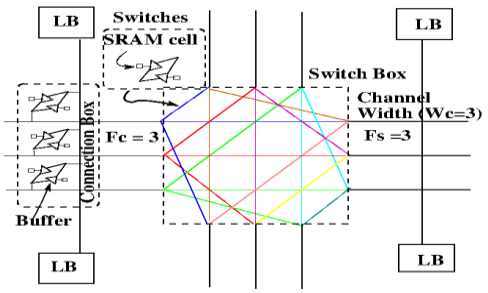

Figure 5: Uniform, Bi-direction island style FPGA

given by K is constructed out of a K-input LUT and a DFF to generate a registered and unregistered output.

FPGA COMPONENT DESIGN

We have constructed an island style FPGA

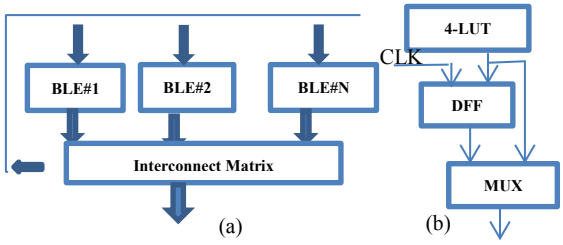

Figure 6: (a) Logic block design and (b) BLE

framework containing logic blocks, switch boxes, connection boxes and configuration registers made up of SRAM cells in order to perform accurate comparative evaluation of NEMS FPGA with CMOS FPGA at the circuit level. Design Architect of Mentor Graphics has been used design the FPGA components and ELDO simulator is used for simulations of the CMOS design

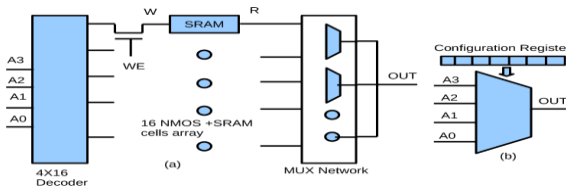

Figure 7: (a) Modeling of 4 input LUT and (b) LUT block

and NEMSIM [16] is used to simulate the NEMS FPGA. Figure 7 illustrates a 4 input LUT design used in BLE which consists of a decoder, 16X1 SRAM cells and a multiplexer network.

The NEMS CLB is depicted in Fig. 8(a). This CLB does not require a decoder, SRAM, configuration registers or MUX output networks. This NEM CLB requires minimal number of switches. The CLB shown in Figure 8(a) can be reconfigured to implement, using six switches, the AND, OR, NAND, NOR, XOR, XNOR gates. The CLB (Fig. 8(a)) is able to realize all the functions in a single interface. The operation of this circuit is controlled by configuring VDD and GND to the interface of the switch using the control signals C0,

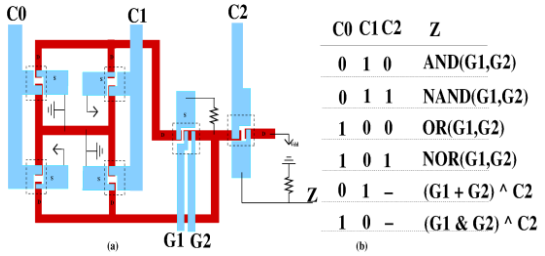

Figure 8: (a) 2 inputs NEMS CLB; (b) Available Functions

C1 and C2. By configuring the correct connection required by the gates shown in Figure 4, the NEMS CLB is able to realize these gates. The input-output behavior of the circuit is shown in Figure 8(b). Four inputs reconfigurable NEMS CLB can be realized by two additional switches. Four inputs CMOS CLB in Fig. 9(a) requires 10 times more switches.

EXPERIMENT

To perform circuit level simulation, we developed a CMOS FPGA spice model with K (LUT size) = 4, N (Number of logic blocks in a CLB). Power analysis for varying number of logic blocks in FPGA is performed using ELDO spice and 180um technology. For NEMS architectures, an equivalent circuit level NEMS netlist is derived and NEMS circuit simulator NEMSIM [17] is used to analyze NEMS FPGAs power.

For large FPGA, VPR 5.0 [18] framework with an integrated power, area and delay model is used. The VPR 5.0 power model uses transition density and static probability information of a signal to compute the dynamic power. To account for NEMS FPGA characteristics, VPR modules concerning leakage and switching power are modified and the NEMS switch R_{on} resistance (75Ω), input capacitance C_{in} (8.4e-16F), the output capacitance C_{out} (0F) are introduced. In the evaluation, we used NEMS switches with 2V operating voltage and leakage currents of 1e-16. We found using VPR that the average routing energy was reduced by 86%, the total energy by 75% and leakage power by 99.9% when compared to CMOS FPGA.

CONCLUSION

In this paper, we presented a new type of NEMS switches that can be configured to implement one of seven basic functions, a nine switches compact look-up table and programmable interconnect to manage leakage current and power. The NEMS FPGA switch block overcomes the mechanical speed degradation. NEMS, once configured, offers zero leakage, zero parasitic capacitance, and low ON resistance results in low power FPGA designs. Traditional based CLBs require more than 150 switches and more than 2 mechanical delays. Our four-input CLB requires only nine NEMS switches and at most two mechanical delays. By reducing the number of devices, our approach improves yield, reproducibility, speed, power and simplifies implementation.

REFERENCES

[1] V. George, H. Zhang and J. Rabaey, "The design of a low energy FPGA," in *ISPLED*, 1999.

[2] J. Kuon and I. Rose, "Measuring the gap between fpgas and asics.," EEE Trans. On CAD of Integrated Circuits and Systems, vol. 26, no. 2, pp. 203-315, 2007.

[3] F. K. Chowdhury, K. N. Chappanda, D. G. Saab and M. Tabib-Azar, "Novel Single-Device "XOR" and "AND" Gates for High Speed, Very Low Power LSI Mechanical Processors," in *Int. Conf. on Solid-State Sensors, Actuators and Microsystems*, Beijing, China, 2011.

[4] M. Hasan, A. Kureshi and T. Arslan, "Leakage reduction in fpga routing multiplexers," in *IEEE ISCAS*- 2009.

[5] S. Srinavasan., et al., "Leakage control in FPGA routing fabric," in *ASPDAC*., 2007.

[6] R. Muller and C. Thakkar, "Use of Nanomechanical relays for fpga power reduction," in *UC Berkeley, EECS*, 2008.

[7] F. Li and L. He., "Circuits and architecture evaluation for field programmable gate array with configurable supply voltage," *IEEE Trans. on VLSI Systems,* vol. 13, no. 9, pp. 1035-1047, 2005.

[8] A. Gayasen, K. Lee, N. Vijaykrishnan, M. Kandemir, M. J. Irwin and T. Tuan, "A dual-vdd low power FPGA architecture," in *Proc. of Int. Conf. on FPL*, 2004.

[9] A. Rahman, et al., "Determination of power gating granularity for fpga fabric," in *CICC*, 2006.

[10] Y. Zhu, S. Thekkel, and S. Bhunia, "Low power fpga design using hybrid cmos-nems approach," in *ISLPED*, 2007.

[11] T. Rueckes, et al, "Carbon nanotube-based nonvolatile random access memory for molecular computing.," *Science,* vol. 289, no. 5476, pp. 94-97, 2000.

[12] M. Liu, H. Yang, S. Tanachutiwat and W. Wang, "FPGA based on integration of carbon Nanorelay and cmos devices," in *IEEE/ACM Int. Symp. on Nano scale Architectures*, 2009.

[13] S. Bhunia, M. Tabib-Azar and D. Saab., "Ultralow-Power Reconfigurable Computing with Complementary Nano-Electromechanical Carbon Nanotube Switches," in *ASP-DAC*, 2007.

[14] C. Chen, P. Roozbeh, et al., "Efficient FPGA using nanoelectromechanical," in *FPGA*, Monterey, CA., 2010.

[15] V. K. Sirigir, K. Alzoubi, D. G. Saab, F. Kocan and M. Tabib-Azar, "Ultra-low-Power Ultra-fast Hybrid CNEMS-CMOS FPGA," in *Int. Conf. on FPL*, Milan, Italy., 2010.

[16] F. K. Chowdhury, D. Saab and M. Tabib-Azar, "Single-device "XOR" and "AND" gates for high speed, very low power LSI mechanical processors Original Research Article," Science Direct: Sensors and Actuators A: Physical, In Press..

[17] K. Alzoubi, S. Han, D. G. Saab and M. Tabib-Azar, "Complementary Nano-Electro-Mechanical Switch For Ultra-Low-Power Applications: Design and Modeling," in *The ISQED*, Santa Clara, CA., 2011.

[18] K. K. W. Poon, "POWER ESTIMATION FOR FIELD," Master Thesis, ECE Dpet. The University of British Columbia, 2002.

[19] S. Bhoj and D. Bhatia, "Early stage FPGA interconnect leakage power estimation," in *ICCD- 2008*.