A 3V CMOS-MEMS OSCILLATOR IN 0.35UM CMOS TECHNOLOGY

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ABSTRACT

This paper presents the design, fabrication and characterization of a fully monolithic 11-MHz oscillator circuit operating with a low voltage MEMS resonator biased below the nominal 3.3V operation of the commercial 0.35-µm CMOS technology used to fabricate the device. The CMOS-MEMS oscillator comprises a polysilicon double-ended tuning fork (DETF) resonator embedded in a differential Pierce oscillator scheme. The device is suitable for RF applications and ultrasensitive mass sensing.

KEYWORDS

CMOS-MEMS, MEMS-based Oscillator, Radio-Frequency MEMS, Sensing System On-Chip.

INTRODUCTION

Microelectromechanical systems (MEMS) based oscillators are significant elements in system on-chip applications that should allow further increase integrated systems functionality. In this sense, MEMS-based oscillators are currently displacing quartz solutions in a growing number of electronic systems such as clock generators in RF systems [1-3]. On the other hand, sensing system on-chip applications (SSoC) demand the integration not only of the resonator signal conditioning circuitry but also the electronics for driving the MEMS at resonance and continuously tracking its resonance frequency (self-tracking circuit). The use of an oscillator circuit has additional advantages since its inherent nature of the quasi-digital output signal [4].

Monolithic integration opens new perspectives in the miniaturization of RF transceivers as well as ultrasensitive resonant sensing. The fabrication of MEMS devices using fully standard and commercial CMOS technology enables a drastically reduction of fabrication costs. Unfortunately, the resonator performance of MEMS implemented using CMOS technology is limited by both the material properties of the CMOS available layers to fabricate the mechanical structures, as well as the technological design rules to define the device dimensions. The current tendency to decrease the size of the mechanical transducer in the new generation of micro/nanoelectromechanical systems based sensors represents a decrease of the capacitive coupling and an increase of the resonant frequency. These design constraints usually translate to high voltages requirements for resonator biasing to achieve a sufficiently low motional resistance to enable self-sustained oscillations that in any case are close to the MΩ range [3-7].

In next section the design and monolithic integration of the CMOS-MEMS oscillator circuit is described. Then, the experimental results obtained from electrical characterization of the device are reported and discussed, and finally, some conclusions are disclosed.

DESIGN AND FABRICATION

The oscillator circuit has been optimized in terms of area, noise and power consumption with respect to the work we reported in [4, 8]. In this work, the oscillator circuit comprises dual-MEMS vibrating micromechanical resonator embedded in a differential Pierce oscillator scheme that allows parasitic feedthrough current cancellation. The design has been performed using a commercial 0.35-µm CMOS technology (AMS C35).

The scheme depicted in Fig. 1 allows applying independent bias voltage to each resonator (V_{B1}, V_{B2}) that regulates the motional current amplitude (I_{M1}, I_{M2}) generated by resonator oscillation. On the other hand, both resonators share the excitation driver voltage (V_O) and thus the parasitic feedthrough currents, between excitation and readout electrodes due to electrostatic excitation, becomes the same ($I_{P1}=I_{P2}$). Each resonator output current is converted to a voltage (V_{S1} or V_{S2}) through the corresponding capacitors (C_{I1} or C_{I2}) acting as signal integrators. In this sense, the use of a differential input amplifier allows to drastically reduce the common-mode signal consisting of the MEMS parasitic current.

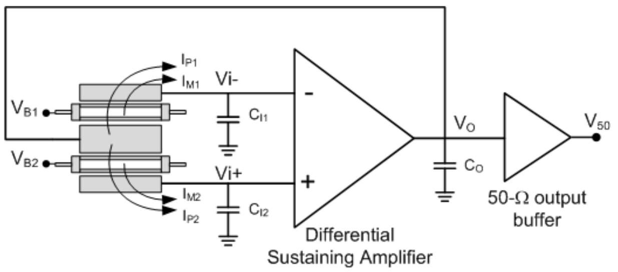

Figure 1: Conceptual circuit schematic of dual-DEFT resonator into a differential Pierce oscillator topology.

Resonator Parameters

The resonant element is a polysilicon dual double-ended tuning fork (DETF). The two identical resonators are defined under the same pad cut to reduce the MEMS area and mismatching due to fabrication processes.

The resonators dimensions are L=12.8µm, W=0.5µm, Wda=1.2 µm, d=2µm, Ls=5.3 µm with a 40 nm gap between the resonator and the excitation and readout electrodes that enable low bias voltage operation (Fig. 2).

One of the resonators is the frequency-determining element of the oscillator circuit while the second one acts as dummy resonator to enable parasitic current subtracting.

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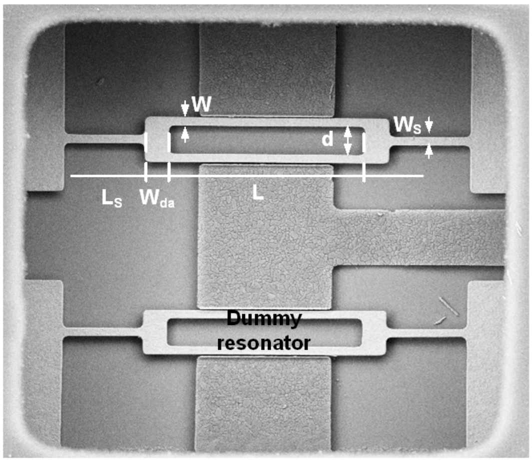

Figure 2: SEM image of the fabricated dual-DEFT resonator.

CMOS Oscillator Circuit Design

As previously introduced, the main design challenge of adapting an oscillator circuit for a CMOS resonator is the very large equivalent motional resistance that has to be compensated by the sustaining amplifier, along with the parasitic capacitance that reduces the phase shift. The noise of any micromechanical oscillator depends on both the circuitry and the resonator noise performance. In particular, the far-from-carrier noise (or noise floor) is determined by the sustaining amplifier noise in the oscillator loop, while the close-to-carrier noise is limited by the electromechanical MEMS performance. A Pierce oscillator topology is used since it is superior to the transresistance amplifier in terms of the oscillator noise figure for high transimpedance gains. The reason is due to the fact that most of the gain is provided by a noiseless capacitive input element rather than a loss resistive element.

The sustaining amplifier has been conceived with the purpose of exhibit a transimpedance gain of ~5 MΩ at 24 MHz with the best trade-off between power consumption and noise. The circuit scheme, depicted in Figure 3, is a differential cascode amplifier with single-ended output buffered by a source-follower output stage. The amplifier inputs (sense nodes) are DC self-biased at 1.3 V by means of two NMOS transistors, in anti-parallel configuration, working in their sub-threshold region and consequently exhibiting an extremely high resistance.

The input-referred current noise of the circuit is as low as 80 fA/√Hz at 24MHz being the best value previously reported in the literature. The use of this compact differential sustaining amplifier results in a drastically reduction (~85%) of the layout area over previous designs (see Table 1 for a comparative). Power consumption has been also reduced from 5.2 mW down to 1.5 mW.

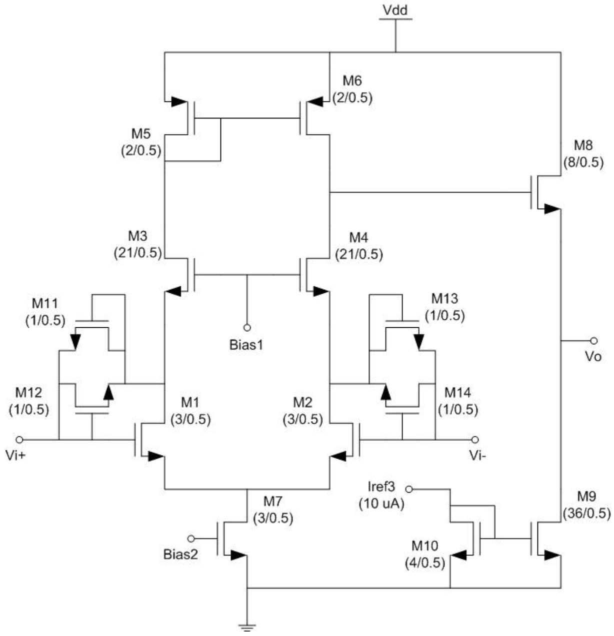

Figure 3: Transistor-level circuit scheme of the differential sustaining circuit based on a cascode voltage amplifier.

Table 1: Specifications (at 24 MHz) of the reported sustaining amplifier circuit in comparison with a previous design.

	Sustaining Amplifier Circuit	
	Design used in [4, 8]	***This work***
Technology	AMS 0.35µm CMOS	
Input configuration	Single-ended	Differential
Transimpedance Gain	11 MΩ at 6 MHz	4.9 MΩ
Output voltage noise	0.93 µV/√Hz at 6 MHz	0.39 µV/√Hz
Input-referred current noise	87 fA//√Hz at 6 MHz	80 fA//√Hz
Oscillator noise floor	-94.3 dBc/Hz at 6 MHz	-115 dBc/Hz
Power	5.2 mW	1.5 mW
Layout area	140×150 µm^2 (0.02 mm^2)	54×66 µm^2 (0.003 mm^2)

Fabrication

The MEMS device is completely defined along the AMS C35 process by using the polysilicon capacitance module available in the technology. In particular, Poly1 layer is used to define the DEFT resonator, while Poly2 layer is used for driver electrodes by means of using the spacer technique as in [6, 8]. The silicon oxide underneath the resonator is used as sacrificial layer that is removed after the standard CMOS process by means of a one-step mask-less wet etching.

Figure 4 shows an optical image of the monolithic CMOS-MEMS oscillator circuit fabricated with AMS C35 technology. In addition to the dual-DETF resonator and the sustaining amplifier, an output buffer has been integrated for testing purposes on 50Ω loads with some loss of signal amplitude and voltage swing.

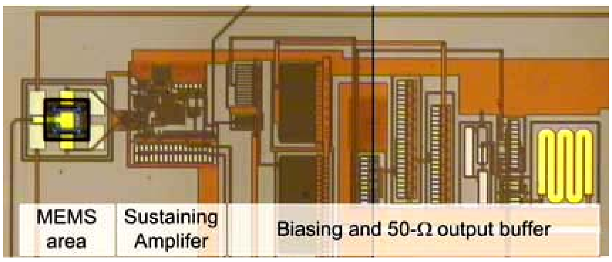

Figure 4: Optical image of the monolithic CMOS-MEMS oscillator circuit fabricated in AMS 0.35µm commercial technology.

EXPERIMENTAL AND DISCUSSION

Open-loop experimental measurements confirm the parasitic feedthrough current cancellation as shown in Figure 5. The parallel resonance has been removed in the frequency response that exhibits for really low bias voltages (V_{B1}) a large resonance peak (~30 dB) as well as ~180º phase shift around ~11 MHz frequency. Note from Fig. 1 scheme that the effective resonator bias voltage (V_{BIAS}) is V_{B1}-1.3V.

The oscillator output signal characteristics (closed-loop measurements) are depicted in Figure 6. The oscillator works properly with biasing voltages as low as 2.8V generating an 11 MHz signal of 90 mV amplitude. In this sense, the CMOS-MEMS oscillator device reported here is superior than the best performance CMOS-MEMS oscillator reported in the literature as shown in Table 2. The phase noise floor (-110 dBc/Hz), that is determined by the electronic circuit, is also 15 dB better than the reported in [9]. In addition, the fabrication process of the oscillator device can be easily supplemented by a zero-level packaging of the MEMS resonator enabling on-chip vacuum operation and sealed against external contamination as has been demonstrated in [10].

On the other hand, the small volume of the DETF resonator (polysilicon single layer), together with its relative high frequency resonance makes the device suitable for ultrasensitive resonant mass sensing applications. A mass sensitivity as low as 9.5 pg/cm^{2}Hz has been determined by FEM simulations that is more than three times better than the metal CC-beam resonator used in our previous work as indicated in Table 3, with the additional advantage of operating at very low voltages. Assuming a similar Allan deviation parameter of the oscillator circuit (<10^{-6}), a device mass resolution value of ~100 pg/cm^2 is obtained, being similar to the best quartz crystal microbalances (QCM) but with an extremely higher spatial resolution, due to the small dimensions of the sensor, and the benefits of device portability [11].

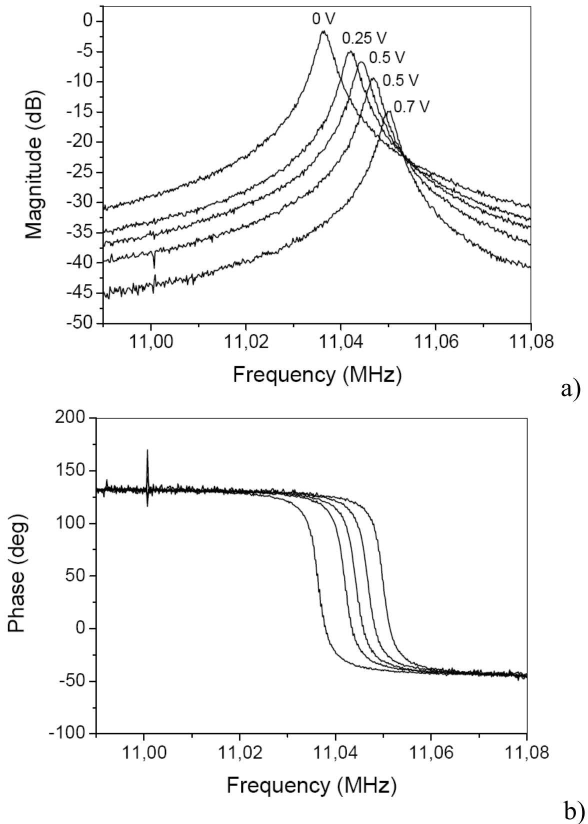

Figure 5: Measured open-loop frequency response of dual-DETF resonator for different bias voltages V_{B1}: a) magnitude and b) phase.

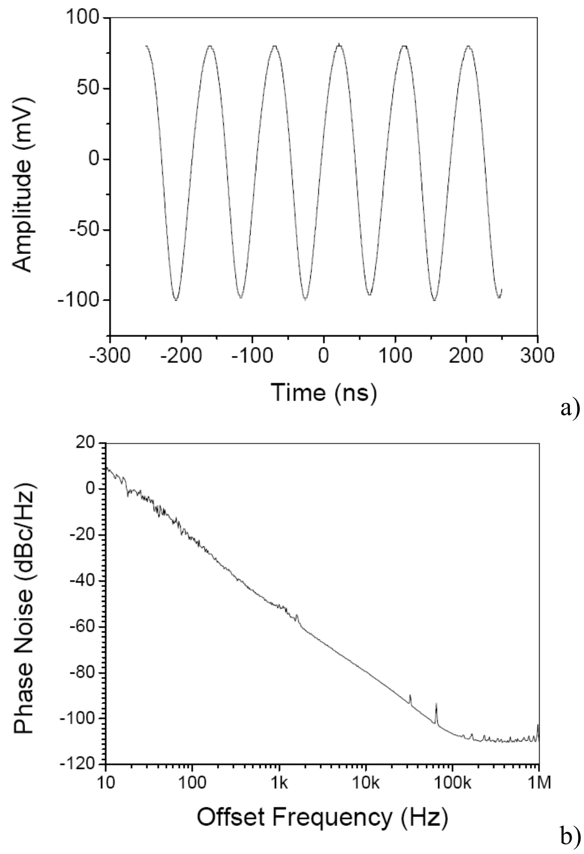

Figure 6: Measured oscillator output characteristic signal with V_{B1} = 2.76V: a) time response and b) phase noise plot.

Table 2: Specifications of the reported CMOS-MEMS oscillator in comparison with the best reported in the literature.

	CMOS-MEMS oscillator	
	Ref. [9]	***This work***
Technology	AMS 0.35µm CMOS	
Transduction gap	100 nm	40 nm
Frequency	10.92 MHz	11 MHz
MEMS Bias voltage	5 V	1.5 V (2.8 V)
Carrier Power	-22 dBm	-17 dBm
Phase Noise (@1kHz)	-80 dBc/Hz	-50 dBc/Hz
Noise Floor	-95 dBc/Hz	-109 dBc/Hz

Table 3: Specifications of the reported CMOS-MEMS oscillator acting as mass sensor in comparison with a previous design developed in the group.

	Ultrasensitive Resonant Mass Sensor	
	SMALL'09 [11]	***This work***
Technology	AMS 0.35µm CMOS	
Resonator	Metal CC-beam	Polysilicon dual-DETF
Transduction gap	600 nm	40 nm
Resonance Frequency	14 MHz	11 MHz
MEMS Bias voltage	45 V	< 3.3 V
Mass Sensitivity	34 pg/cm^2Hz	9.5 pg/cm^2Hz

CONCLUSIONS

We have reported on a fully monolithic 11-MHz CMOS-MEMS oscillator device based on a polysilicon DETF. Although oscillator specifications are not comparable with those obtained from non-monolithic devices, this work represents an important breakthrough among monolithic CMOS-MEMS oscillators mainly thanks to its reduced biasing voltage requirements (CMOS compatible) and its simple and low-cost fabrication process. Moreover, the inherent very high mass sensitivity of the reported DETF resonator and relative high frequency, together with the fully monolithic integration of the oscillator circuit that provides a highly stable quasi-digital output signal, makes the device also suitable for resonant mass sensing in sensing system-on-chip applications improving previous works.

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