# POST-CMOS ON-CHIP INTEGRATION OF 3D MEMS INDUCTORS USING A NOVEL CHIP EMBEDDING TECHNIQUE

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## ABSTRACT

This letter reports the integration of high-Q vertical ring inductors on individual small CMOS chips using a novel chip embedding technique. A small CMOS voltage controlled oscillator (VCO) chip which has 2×2mm$^2$ in size and 5.8 GHz of operating frequency was used for post integration. The chip embedding technique enables the post-CMOS processing on such a tiny individual chip. The integration of vertical ring inductor on the CMOS chip was completed by Plastic Deformation Magnetic Assembly (PDMA). Both numerical simulation and experimental characterization of the inductor performance have been conducted. The vertical ring inductor manifests a stable inductance value over a wide frequency range (45MHz~8 GHz) and a high quality factor of 110 at the operation frequency of the VCO (5.8 GHz).

## KEYWORDS

On-chip integration, Post-CMOS integration, Chip embedding, Plastic Deformation Magnetic Assembly (PDMA), RF-MEMS inductor, Vertical inductor, Voltage-controlled oscillator (VCO), SU-8.

## INTRODUCTION

On-chip integration of high performance RF passive components is critical for the development of next generation wireless communication systems with higher operating frequencies, lower noise level and reduced power consumption [1-2]. However, it has always been a challenging issue to achieve efficient integration due to incompatibilities of MEMS fabrication with standard IC foundry processes. To overcome this problem, a post-CMOS integration strategy is often adopted, in which CMOS circuits are first fabricated and the MEMS components are built onto the finished CMOS substrates as add-on components [3-8]. However, current CMOS chips are dramatically shrinking in size for higher component density and lower fabrication cost. This miniaturization makes a finished CMOS chip extremely difficult to handle and further process, thus preventing effective post-CMOS integration of MEMS components. To address this issue, we report a novel chip embedding technique which is capable of significantly extending the effective processing surface area of the originally small CMOS chip. This enables efficient post-CMOS integration of various MEMS components, including three-dimensional RF-MEMS inductors (Figure 1); which are otherwise very complex to integrate due to having dimensions comparable to or even larger than the CMOS chip itself.

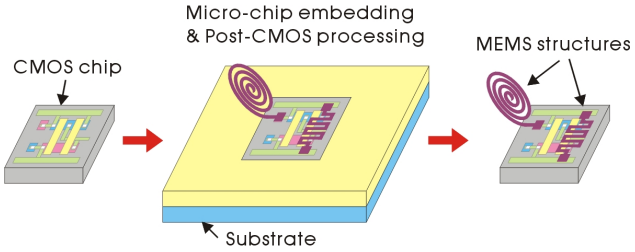


*Figure 1: Schematic diagram of post-CMOS integration technique using chip embedding technique*

## CHIP EMBEDDING TECHNIQUE

Embedding techniques utilizing silicon supporting pieces surrounding a small CMOS chip were introduced earlier [9]. This approach could effectively avoid the edge-bead phenomenon in the spin coating process which is a serious problem for the small chip substrate [10]. However, there are still critical issues in terms of surface planarization. First, the height of the CMOS chip might be different from the silicon pieces slightly since each silicon wafer has a few micrometers of variance in height. In addition, several micrometers of gap between the CMOS chip and silicon pieces are inevitable in practical applications. These height mismatches and gap make it impossible to fabricate large micro structures across the boundary of the chip.

To extend the small chip processing area with reasonable surface planarity we developed a novel and straightforward polymer-based chip embedding technique (Figure 2). SU-8 epoxy series resist (Microchem, MA) was chosen as the polymer filling material due to its simple processing, excellent mechanical strength and chemical stability. In order to test the small chip embedding process, we used a dummy silicon chip which has the same dimension with a real CMOS chip. As shown in Figure 2, the silicon chip was embedded as the following steps:

1) Approximately 1 mL of SU-8 100 was applied on the first glass substrate (1×1 in$^2$) and spin-coated (Figure 2a). The spin coating was performed in two steps, beginning with a spread cycle (7 s at 500 rpm with 100 rpm/s acceleration) to ensure uniform resist distribution and surface coverage; followed by a spin cycle (30 s at 1500 rpm with 300 rpm/s acceleration) which resulted in a coating thickness of ~ 180 µm.

2) The dummy silicon chip (2×2 mm$^2$) to be embedded was placed on the SU-8 coated glass substrate (Figure 2b).

3) On a second glass substrate a sacrificial layer (MicroChem's OmniCoat) was spin-coated (30 s at 1000

rpm with 100 rpm/s acceleration) and soft baked on a hotplate at 200 °C for 1 min, followed by spin coating an SU-8 100 layer on top using the same conditions in step 1 (Figure 2c).

4) Then, the two glass substrates were soft baked at 65 °C for 20 min, followed by 95 °C for 1 hr; after which the substrates were contacted face to face and pressed together to squeeze the silicon chip inside (Figure 2d).

5) The front side of the entire stack was exposed to UV light (12 mW/cm$^2$ for 1 min), and a two-step post-exposure bake (PEB) was conducted at 65 °C for 1 min and 95 °C for 20 min. By etching the sacrificial layer using MicroChem's Remover PG, the second substrate could be detached from the silicon chip and the first glass substrate. Any SU-8 residues on the surface of the embedded silicon chip were cleaned by oxygen plasma in a reactive ion chamber (Figure 2e).

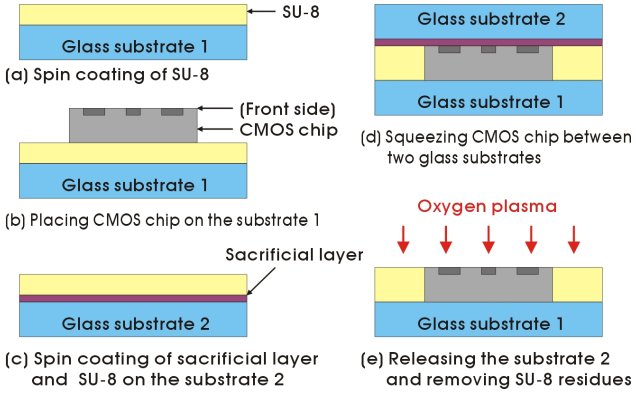


*Figure 2: Schematic process flow of the new micro-chip embedding technique using SU-8 as the filling material.*

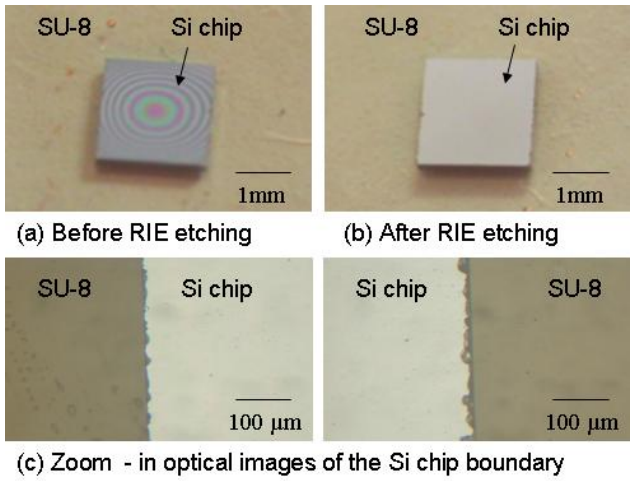


*Figure 3: Optical images of a dummy silicon chip (2×2mm$^2$) embedded in SU-8*

Figure 3 shows images of the silicon chip embedded in SU-8 before and after oxygen plasma cleaning. To check the planarization of SU-8 surface with the silicon chip, the surface profile was measured with the Dektak surface profiler. Excellent smoothness and height match (≤ 0.2 µm) between the SU-8 and silicon surfaces were achieved, which make the extended, new chip surface area suitable for microfabrication purposes (Figure 4).

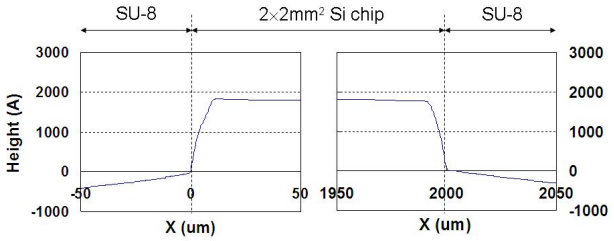


*Figure 4: Surface profiles at the interface between the embedded silicon chip and SU-8 after plasma cleaning.*

## INDUCTOR DESIGN

As an application of the novel micro-chip embedding technique, a high-Q vertical ring inductor was developed and integrated onto a small CMOS VCO chip to reduce the loss of the LC tank, which is expected to result in a stronger oscillation, lower phase noise in the frequency domain and result in smaller jitter in the time domain [11]. The vertical ring inductor was designed to realize an inductance value of 1 nH with minimum substrate parasitics and loss. Different from conventional 2D inductor design, trade-offs among electrical performance, mechanical stability and ease of fabrication were considered. The ring inductor consists of both circular and straight portions. The circular portion forms the ring inductor, while the straight one separates the ring inductor from the substrate to increase electrical isolation.

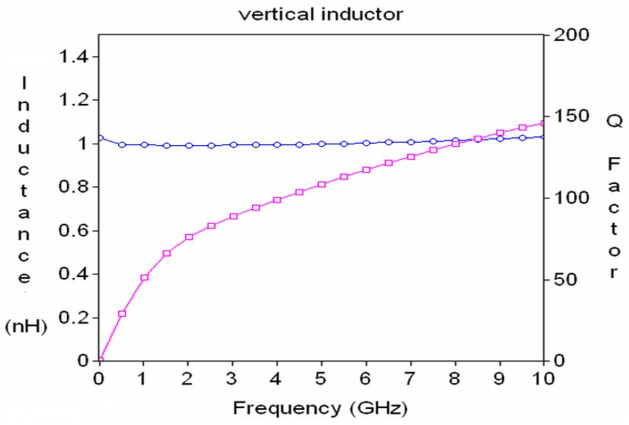


*Figure 5: Simulated inductance value and quality factor of an optimal vertical ring inductor design.*

Due to its high electrical conductivity and mechanical ductility, copper was chosen as the structural material of the inductor. Ring inductors with different geometric parameters were designed. While the total inductance value of the inductor is mainly determined by the total length and circular/straight ratio of the conductor line, its width and thickness are critical factors to affect the Q factor. Generally, a wider and thicker (up to certain extent limited by the skin depth) conductor line would result in lower resistance and thus higher Q factor. This also leads to a stiffer inductor structure with better mechanical

stability. However, if the inductor structure becomes too stiff, it will be difficult to realize the vertical placement of the inductor on chip. Based on our previous experience, a thickness of 6 µm was chosen for the inductor fabrication.

The $S_{11}$ parameters of different inductor designs were simulated with Sonnet® and the inductance and quality factors were extracted. The structural stability of the vertical ring inductor under mechanical shock occurring in the most vulnerable direction (perpendicular to the inductor plane) was also estimated using cantilever beam theory [12]. Based on both the electrical and mechanical simulation results, optimal ring inductor designs were determined.

Figure ***5*** shows the inductance and Q factor of an optimal inductor design (250µm of radius with 100µm of width, 250µm of length with 60µm of width).

## FABRICATION AND TESTING

To achieve vertical ring inductors, planar ring inductors were first fabricated on the substrate and then bent vertically using plastic deformation magnetic assembly (PDMA) [13]. PDMA exploits the behavior of magnetic materials in a transverse magnetic field and uses it to raise materials off the substrate. It provides a robust and controllable method to build vertical microstructures in a parallel and batch-scale fashion. However, the original PDMA process involves a "blanket" etching of either silicon oxide or aluminum as the "sacrificial" material for the implementation of PDMA. Although this is compatible with bare silicon substrates, it will cause problems with CMOS substrates since silicon oxide and aluminum are construction materials for on-chip CMOS circuits and the etching will inevitably destroy the prefabricated circuit components.

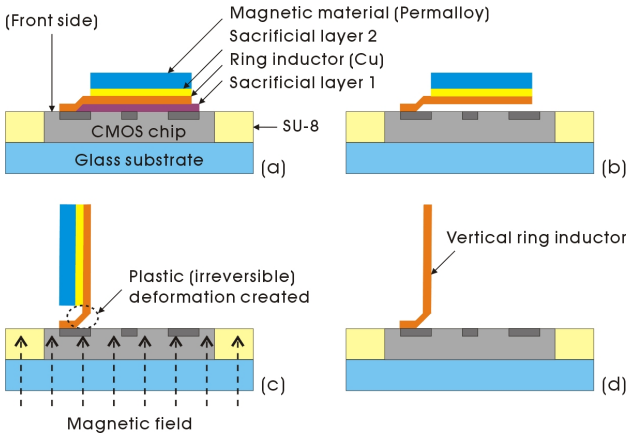


*Figure 6: Schematic illustration of the fabrication process of vertical inductors.*

To address this issue, we have tested different materials and finally chose zinc oxide as the "sacrificial" material, since it can be easily deposited and etched, which is compatible with CMOS substrates. The entire on-chip integration process of the vertical ring inductor has been conducted as the following steps (Figure 6):

1) The CMOS VCO chip was embedded in SU-8 using the novel chip embedding technique for enabling semiconductor process and extending possible processing area (Figure 2)

2) The ring inductor (6-µm-thick copper layer) was fabricated on the chip substrate using thermal evaporation and electroplating. The inductor structure was separate from the substrate by the first sacrificial layer (zinc oxide) (Figure 6a).

3) To implement PDMA, a magnetic Permalloy layer was deposited onto the ring inductor structure. The Permalloy piece was separate from the ring inductor structure by the second sacrificial layer (photoresist) (Figure 6a).

4) After completely removing the zinc oxide layer (Figure 9b), a magnetic field was applied underneath the substrate to conduct PDMA. The magnetization of the Permalloy piece created a torque to lift the ring inductor structure and created bending to hold the ring inductor in its vertical position (Figure 6c).

5) After PDMA, the second sacrificial layer was completely removed to detach the Permalloy piece leaving behind the vertical ring inductor (Figure 6d).

Figure 7a shows the layout design of the VCO circuit, and Figure 7b shows the microscopic image of the complete VCO circuit integrated with the vertical ring inductor. Here, two contact pads were designed to interface with the vertical ring inductor. Based on our previous experience and EM simulation, a pad size of 50 µm × 50 µm and separation of 220 µm were selected to ensure both satisfactory mechanical and electrical performance of the vertical ring inductor.

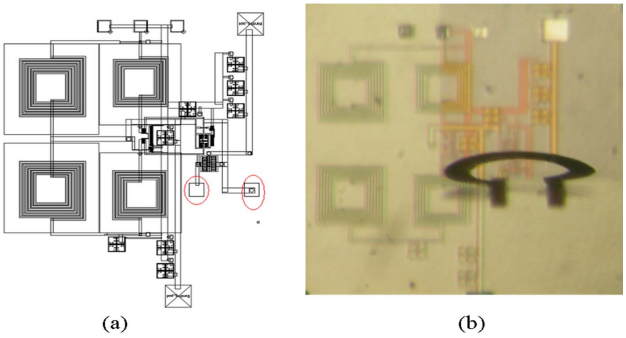


*Figure 7: (a) Layout design of the 5.8 GHz VCO. The two contact pads circled in red were used to interface with the vertical ring inductor. (b) Optical microscopic image of the integrated vertical ring inductor on the VCO chip.*

To characterize the performance of the vertical ring inductor, the $S_{11}$ parameters of the fabricated inductor were measured up to 8.1 GHz using HP® 8510 network analyzer. After de-embedding the contact pads, both the inductance and Q factor were extracted from the $S_{11}$ measurement results. Figure 8 shows the extracted inductance value and Q factor for the ring inductor based on the optimal design, which closely match the simulation results shown in Figure 5. The inductor achieves and inductance of 1nH over a wide range of frequency and its Q factor reaches ~ 110 at 5.8 GHz, indicating a superior performance over conventional on-chip 2D inductors with Q factors around 10 [14].

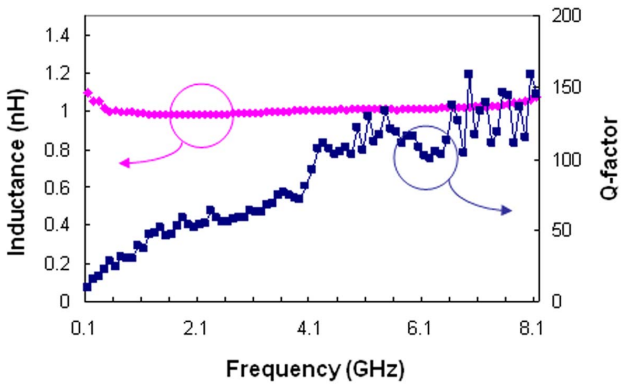


*Figure 8: Inductance and Q factor extracted from $S_{11}$ measurement results.*

## CONCLUSION

A novel chip embedding technique was developed for efficient post-CMOS integration of MEMS components. We also presented a novel post-CMOS integration of the 2×2 $mm^2$ VCO chip using the SU-8 embedding system. The vertical ring inductor with superior performance and much smaller substrate occupancy was successfully fabricated and integrated on the CMOS VCO chip. The novel chip embedding technique developed in this work could be readily adapted to achieve efficient BEOL, post-CMOS integration of large and complex MEMS components with tiny CMOS circuit chips.

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