ACTIVE CMOS-MEMS CONDUCTIVE PROBES AND ARRAYS FOR TUNNELING-BASED ATOMIC-LEVEL SURFACE IMAGING

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ABSTRACT

This paper reports on development of AFM-like active CMOS-MEMS conductive probes and arrays. The active probes are aimed for scanning tunneling microscopy (STM) imaging and field-emission (FE) assisted nanostructure formation. Two kinds of STM tip approaches compatible with CMOS-MEMS process — Electron-Induced Beam Deposition (EBID) and Spindt tip method — are presented, and their functionality is examined. Atomic-level resolution is achieved using tips in an ultra-high vacuum (UHV) STM. The MEMS probe working in ambient STM is also demonstrated. The active probe is equipped with a transimpedance amplifier (TIA) for tip FE current measurement around a nominal value of 1 nA.

KEYWORDS

CMOS MEMS, probe array, thermal actuation, SPM

I. INTRODUCTION

Scanning Probe Microscopy (SPM) techniques, such as Scanning Tunneling Microscopy (STM) and Atomic Force Microscopy (AFM), are powerful tools to study local surface properties with atomic resolution. SPM also allows nano-scale modification of surface topography, such as the famous IBM individual atomic manipulation [2]. These developments motivate SPM-based bottom-up tools for nanofabrication, where probes are mechanically moved across the surface, and the nano-patterns are formed by highly spatially confined reactions, physical or chemical, depending on the specific sample materials, between the stylus and substrate, with the smallest feature size down to 4 nm [3-4]. In these applications, however, nanofabrication is discrete and of low throughput. Rapid, direct fabrication of nanostructures becomes possible by implementing a batch fabricated AFM-like nanofabrication probe array (*e.g.,* the IBM 'Millipede' probe array for data storage [5]).

In our work, we envision STM-based nanofabrication using an array of probes. This approach makes use of tip-directed, field-emission (FE) assisted reaction to locally modify the materials surface (*e.g.*, by oxidation, deposition, or removal) where the nanostructure geometry is controlled by FE beam size, and can be real-time examined via *in situ* SPM imaging using the same tip. Above all, a compact multi-probe array offers the possibility for parallel device fabrication: each probe has its own servo control and thus is individually addressable, which is of greatest significance in terms of allowing sub-nanometer control for each tip to substrate gap.

For this independent probe control, on-chip servo circuitry approach has been adopted [6], to significantly relieve the need for large numbers of off-chip interconnections and the associated parasitic effects. This is particularly important when operating in an ultra-high vacuum system, where only a handful of electrical interconnections are possible (6 for our system). In our work, a CMOS-MEMS process is used to fabricate the probe array. This technique promises to support a high level of integration on a single chip with actuation, sensing and feedback control circuitry as well as the mechanical structure, and hence greatly reduces the external wiring. Further, while most probe array research up to now is limited to AFM mode, the CMOS-based multi-probe array is intended for STM application featuring an order of magnitude smaller scale manipulation than AFM, and where the MEMS integration with CMOS minimizes the design complexity of external controller and system setup in conjunction with a traditional STM.

The present work describes an improved design of active CMOS-MEMS conductive probes and probe arrays. Our last designed probes [1] suffer snap-in issues during STM imaging due to strong attractive electrostatic (ES) forces between the probe cantilever and the scanned surface. This is addressed by having a stiffer probe structure and adding electrostatic shielding. Nanometer-sized tips are integrated on active probe array and are applied in an STM system for imaging. A preliminary on-chip TIA for current measurement is also designed and characterized.

II. PROBE DESIGN AND CHARACTERIZATION

Probe and Array Design

The designed active CMOS-MEMS probe array is shown in Fig. 1. A 1-D array of 5 cantilevers is designed on one side of the 2.4 mm by 2.4 mm chip (Fig. 1(a)). The probes are designed identically for the purpose of matching the curl-up height among the probe array after structure release of the residual stress. Each probe is equipped with vertical z-axis electro-thermal (ET) actuation and thermal isolation structures (TIS) for high driving efficiency. Each probe has a separately driven actuator dedicated bond pads. The 5 μm-diameter circular tip platform made from top-most CMOS metal-4 (m4) provides a flat area on which a platinum tip is located. For the current generation of probes, one on-chip TIA is connected to a single probe to test its current sensing ability.

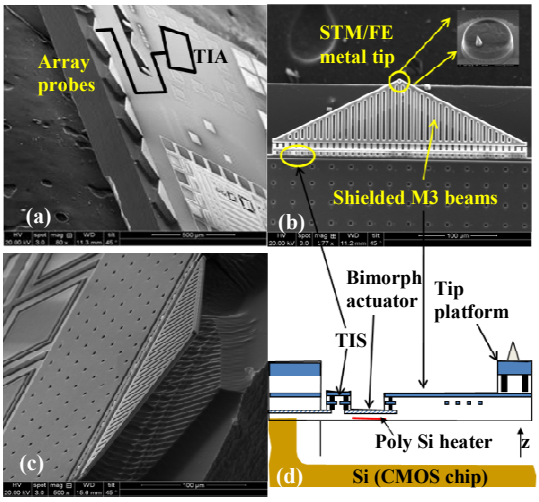

Fig. 1: Active probe array design: (a) 5x1 Probe array; (b) Probe top view; (c) Probe tilted view; (d) Probe schematic

Probe Process and Mechanical Characterization

The active MEMS probe array is made using post-CMOS MEMS processing. The custom-designed CMOS chip from the foundry (TSMC 0.35µm CMOS) is processed with an anisotropic oxide etch, and then a directional silicon etch followed by an isotropic silicon etch to undercut the structure for the release.

The fully released array probes purposefully curl up, because the 7 µm-long metal-1 (m1) "hinges" act as a stress bimorph, which are made of a top aluminum layer and a bottom oxide layer. Beam curling results in a 7.6 µm upward tip deflection after release (Fig. 2(b)). The deflection difference among array probes is smaller than 0.2 µm. Upon actuation, the probe is displaced downward (*i.e.,* toward the probe substrate) by 1.6 µm at 17.4 mW drive, representing a driving sensitivity of 92 nm/mW in air. Each probe may be actuated separately to different height using different actuation voltages, as demonstrated in the interferometer image of Fig. 2(d). The probe thermal cut-off frequency is 370 Hz; the mechanical resonant frequency is 87 kHz.

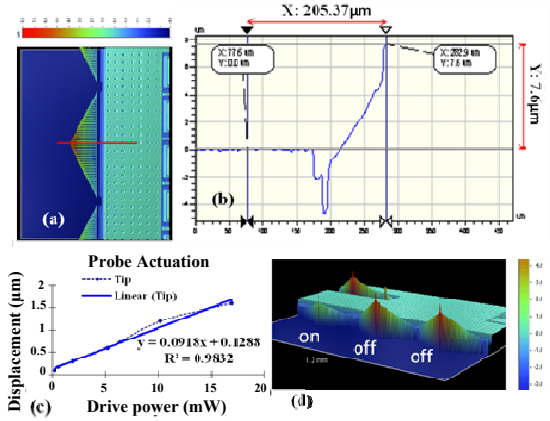

Fig. 2: Interferometer image of CMOS-MEMS probes: (a) & (b): ~7.6 µm self curl-up up release; (c) Actuation displacement vs. drive power; (d) Independent actuation of array probes

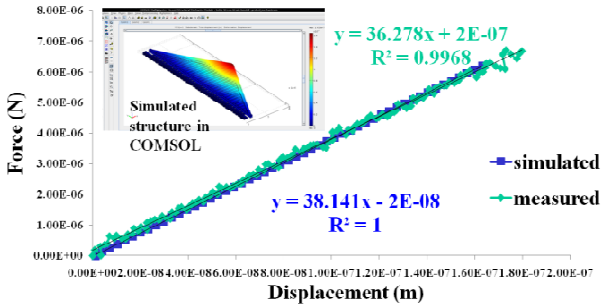

Fig. 3: Active probe mechanical spring constant measurement

The current probe is 329.1 µm in width, with a practical spring constant of 36.3 N/m measured by a nanoindenter, and matched well with the finite-element simulation result of 38.1 N/m, as shown in Fig. 3. This is six times stiffer than the previous design. Only one row of TIS is put in the structure compared to two rows previously. Further, the main cantilever body, which is made from the metal-3 (m3) dielectric metal stack in the CMOS process, is set to the same voltage as the scanned sample surface so that there is minimal ES attraction between tip and sample. The m4 tip platform is electrically isolated from the cantilever body and the signal line is shielded by routing it down the cantilever in a lower CMOS metal layer.

On-Chip TIA Characterization

In STM equipment, the tunneling current is amplified by an external TIA with the gain as high as 10^8, realized by a 100 MΩ resistor. This conventional design is difficult to implement in CMOS with adequate bandwidth due to large resistor area and the accompanied huge leakage current and parasitic capacitance. This issue is partially resolved by using a T-feedback resistor network for our preliminary version of the TIA, illustrated in Fig. 4(a), which halved the layout area to 0.03 mm^2. The TIA performance is shown in Fig. 4(b). A current of 1 to 10 nA is applied as a test signal to the TIA input. The circuit performance matches well with the simulation, with a measured transimpedance gain of 73.7 MΩ and bandwidth of 1.56 kHz.

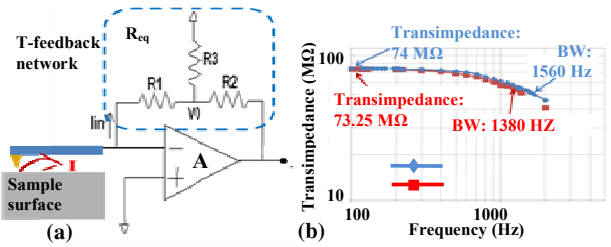

Fig. 4: TIA Performance: (a) T-feedback network; (b) simulated and measured BW and transimpedance gain of the TIA.

III. TIP FABRICATION ON CMOS PROBES

A good STM/FE tip requires ultra-sharp geometry, tip rigidity and stable chemical composition [7]. This is especially important for an AFM probe used in STM mode,

where the two main snap-in forces that can cause inelastic instability, the Van Del Waals force and ES force, are proportional to tip radius and related to tip shank shape [8]. With a probe stiffness of 40 N/m, necessary tip radius is calculated to be smaller than 20 nm. Here we present two approaches of fabricating a nanometer-sized platinum tip on CMOS-MEMS probes. The focused Electron-Induced Beam Deposition (EBID) method has great precision and is suitable for rapid prototyping; the Spindt tip process is able to batch fabricate tips and will be necessary for large probe arrays.

EBID Tip Process

Focused EBID is a widely used technique for fabricating nanostructures of various kinds, such as the tip end of tungsten cold field emitters, nanosoldering and nanostructuring, and plasmonic gold nanopatterns for optical application [9-10]. We applied this approach to make STM probes on CMOS chips. Fig. 5(b) shows a series of EBID Pt tips made with different e-beam scanned area. Tips with radius of 10 nm are obtained. To obtain a high aspect-ratio tip, we adopt a "layer-by-layer" technique: a circular Pt layer of several μm^2 is first deposited on the m4 tip platform followed by a series of depositions on the same location, each with gradually shrinking e-beam scanned area, also illustrated in Fig. 5(b).

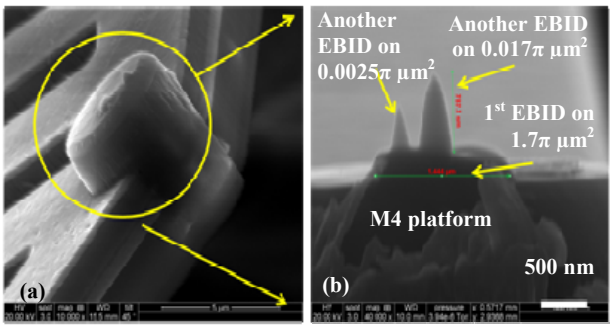

Fig. 5: EBID Pt Tips (a) Tips on m4 platform; (b) Tips with different focused deposition area. A 'layer-by-layer' EBID is also demonstrated.

Spindt Tip Process on MEMS Probes

An initial Spindt tip process was reported in [1]. A Spindt nickel tip is firstly made on the Al m4 tip platform, and Pt coating of tips is performed after structure release. Ni tips have been made with tip radius down to 10 nm. However, the subsequent dielectric oxide etching blunts the tips, but with different severity depending on the etch approach. The original 4-5 hr long RIE oxide in a PlasmaTherm 790 system resulted in substantial milling and dulling of the tip (Fig. 6(b)). Advanced Oxide Etch (AOE) in an STS ICP system requires 30 to 40 min to etch the 9 μm thick CMOS dielectric stack. The resulting Ni tip sharpness is thus little changed in AOE (Fig. 6(a)). However, all of the AOE tips were detached after the following Si DRIE MEMS release etch. The Ti adhesion layer between nickel tip layer and CMOS aluminum is attacked by the SF_6 DRIE plasma. A different adhesion layer, such as chromium, must be used in a future modification to the process that is expected to lead to viable batch-fabricated tips.

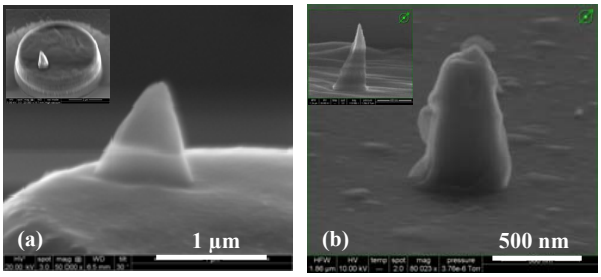

Fig. 6: Spindt tip after (a) STS AOE; (b) PlasmaTherm RIE. Inserted SEMS show the tips before oxide etching.

For Spindt tip functionality examination in STM, a passive MEMS probe was prepared, the procedures summarized in Fig. 7. The probe will have no pull-in issue thanks to the stiffness of the 300 μm-thick silicon cantilever structure.

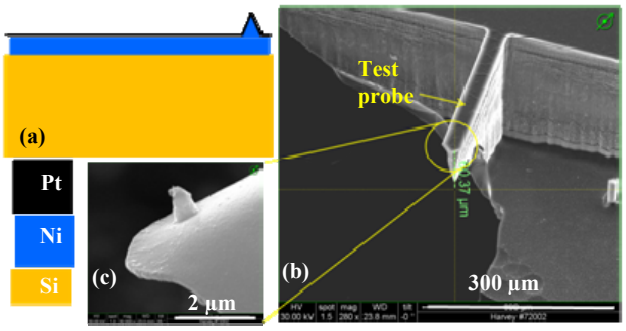

Fig. 7: Test probe for Spindt tip verification: (a) Probe cross-sectional schematic; (b) SEM probe structure after MEMS processing; (c) Enlarged SEM of Spindt tip

IV. STM IMAGING

The passive MEMS probes with Spindt tips are tested in an RHK UHV STM system. The imaging sample is a Si (100) 2×1 reconstruction surface. Atomic-level resolution imaging was obtained, as shown in Fig. 8, where the dimer rows are clearly observed with the ones on the adjacent terraces perpendicular to each other.

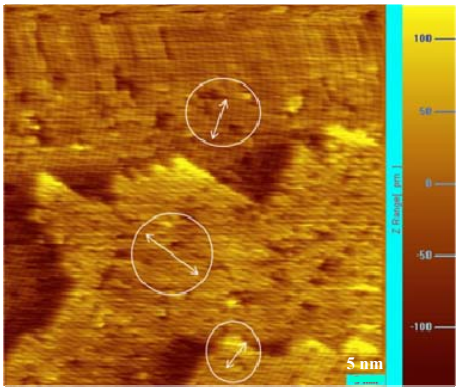

Fig. 8: STM image of Si (100) via test probe. Dimer rows on adjacent terraces are perpendicular to each other.

CMOS-MEMS active probes with EBID tips are also tested in an RHK STM, but in ambient conditions. As the chip holding the active probe is wider (2.4 mm) then that of commercial AFM tips (1.5 mm), it cannot be inserted into scan head using the exchange holder in UHV, and must be mounted manually in ambient. Fig. 9(a) is the STM imaging on highly ordered pyrolytic graphite (HOPG). The AFM-like MEMS probe scans successfully in STM mode, with the terrace on the surface resolved. Fig. 9(b) shows an I-V characteristic of the Pt-HOPG junction: a linear voltage-dependence for small voltages and an exponential characteristic for larger voltages.

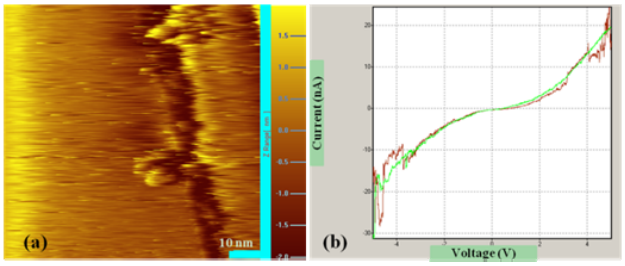

Fig. 9: (a) Ambient STM image of HOPG using the CMOS-MEMS probe with an EBID Pt tip. (b) I-V characteristic curve of the Pt tip – HOPG junction

A test involving MEMS probe actuation in STM mode was carried out on a Veeco SPM system in air. (Currently, the RHK STM system has just one electrical connection that is needed for tip current. The Veeco enables multiple connections.) The active probe is mounted on a modified probe holder with four signal communication lines connected outside: tunneling current drawn out to home-made TIA installed on Veeco, amplified voltage fed back to system control-loop, the probe actuation drive line and the shielding line fixed to sample voltage. The MEMS probes with EBID tips work normally in the Veeco STM without actuation, with set current varying from 300 pA to up to 20 nA.

V. CONCLUSION

An active CMOS-MEMS array of five probes is successfully fabricated with adequate stiffness of 36 N/m and 1.6 µm stroke to handle STM operation in air without experiencing snap-in. The probe actuator thermal cut-off frequency of 370 Hz is low for tip-based nanomanufacturing applications, however this bandwidth can be increased in future closed-loop operation at the expense of more power. EBID is good for rapid prototyping sharp Pt tips, made down to 10 nm radius, on the CMOS-MEMS probes. The MEMS tips work properly in both UHV and ambient STM systems, and atomic resolution imaging is obtained in UHV system. Probe actuation involvement in real-time STM imaging is work in progress. An off-chip external feedback loop is being designed, and will be co-work with on-system control loop to demonstrate simultaneous imaging/writing of parallel active probes.

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