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A BROADBAND 3D PACKAGE FOR RF MEMS DEVICES UTILIZING THROUGH SILICON VIAS (TSV)

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ABSTRACT

Packaging RF-MEMS devices require the parasitic effects of packaging to be minimal on the RF performance. In this paper, a 0-level packaging structure which utilizes TSVs in the cap wafer for electrical connection is proposed. To determine the RF performance of the package, transmission lines (CPW) were fabricated on high resistivity silicon (HRSi) substrates, and the grounding configuration optimized for. The package structures were based on actual RF-MEMS device layouts, which include test pads for DC biasing. A package loss of 0.1 dB was measured at 10 GHz. The RLGC parameters of TSVs in a GSG configuration were also extracted up to 12 GHz. Based on the transition, a 94-GHz antenna was also designed and characterized for.

KEYWORDS

Packaging, Grounding, RF MEMS, TSV, Antenna

INTRODUCTION

Packaging for RF-MEMS Devices

The proposed test vehicle for packaging RF MEMS devices is shown in Fig. 1. Solder sealing and TSVs in the cap wafer are used to achieve electrical connection while encapsulating the MEMS device.

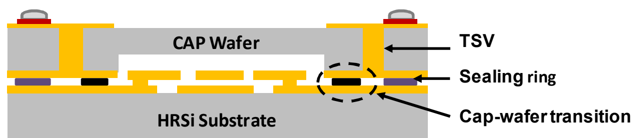

Fig. 1: Test vehicle for 0-level package

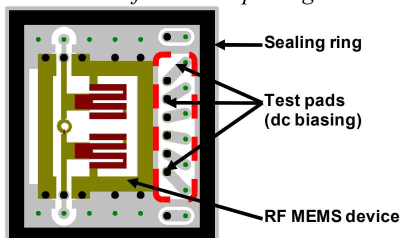

Fig. 2: Typical RF-MEMS package

With the TSVs located within the boundary of the sealing ring, a small form factor can be achieved with the proposed test vehicle. While literature exists on designing packages for RF devices [1-2], to our best knowledge, none has considered package design based on the actual layout of a RF MEMS device. This work seeks to minimize the package loss by optimizing the grounding configuration of the package. The package configuration is based on an actual RF-MEMS layout with test pads for dc biasing. The RF performance of the package is ascertained through transmission lines designed on high resistivity silicon substrates (1000 Ω.cm).

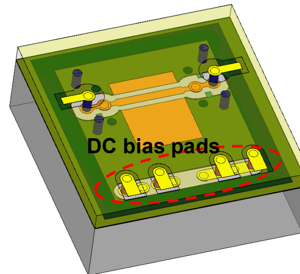

Fig. 3(a): TSV Model 1

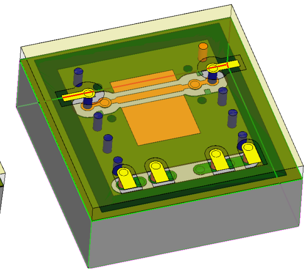

Fig. 3(b): TSV Model 2

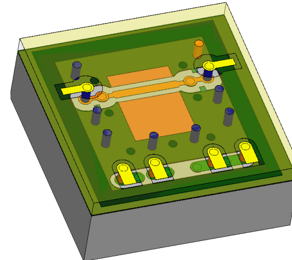

Fig. 3(c): TSV Model 3

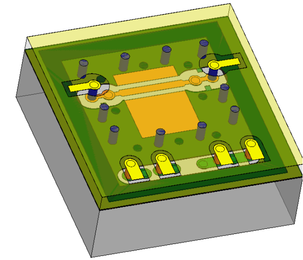

Fig. 3(d): TSV Model 4

A typical RF-MEMS package is shown in Fig. 2. To determine the package performance, the RF-MEMS device is replaced with a coplanar waveguide (CPW) transmission line. As shown in Fig. 3, the overall structure involves multiple ground planes. As such, ensuring for proper ground return paths becomes paramount in order for the package to operate up to high frequencies. In optimizing for the grounding configurations, 4 different models were considered. Fig. 3(a) considers for a typical CPW-to-CPW transition in a back-to-back configuration (Model 1). In subsequent Models 2 and 3, the grounding vias are gradually increased in the lateral dimension. The optimum configuration is shown in Model 4 of Fig. 3(d), where the grounding is closest to the signal for the return current path (least inductance). The overall length of the model is 2 mm, including two TSV transitions. The CPW line is 1 mm long. The TSV pitch is 350 μm with via diameters of 100 μm. The other key parameters pertaining to the test vehicle are shown in Table 1.

Table 1: Parameters of RF-MEMS test vehicle

Parameters	Value
Cap wafer thickness	200 μm
Sealing ring height	8-9 μm
Substrate thickness	750 μm
Substrate resistivity	1k-10kΩ.cm
Sealing ring width	200 μm
RDL thickness	1.5 μm

FABRICATION PROCESS

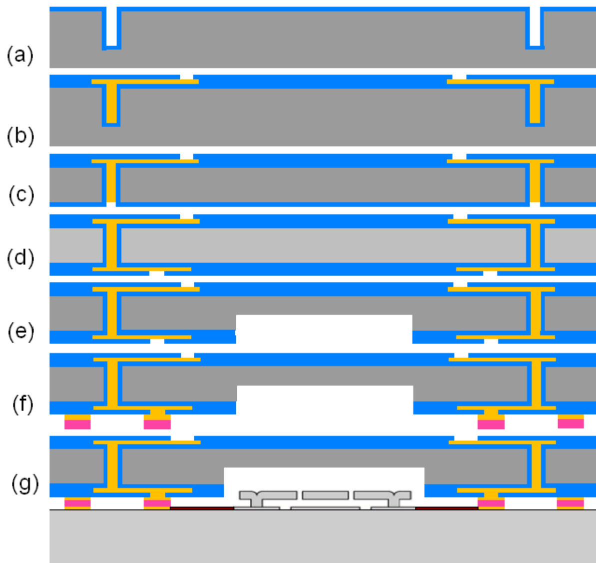

Fig. 4: Process flow of wafer level packaging with TSV

The fabrication of the test vehicle for RF-MEMS packaging involved a TSV cap wafer with CPW transmission lines on the substrate wafer. The key aspect lies in the fabrication of the TSV interconnects and redistribution layers (RDL). Fig. 4 shows the process flow of the wafer level packaging with TSV. 700 µm-thick 8" high-resistivity silicon wafers were used in the process. (a) The cap wafer was firstly etched with vias by DRIE and passivated with thermal oxide; (b) The vias were fully filled with copper by electroplating, and then the top side RDL was fabricated and passivated; (c) The cap wafer was grinded from backside to expose the vias and then passivated; (d) Backside RDL was fabricated and passivated; (e) A cavity was fabricated by DRIE to accommodate the MEMS devices (the cavity was not etched for our test vehicle); (f) UBM/sealing-ring solder were fabricated on the wafer backside; (g) Lastly, the cap wafer was bonded to the MEMS substrate wafer.

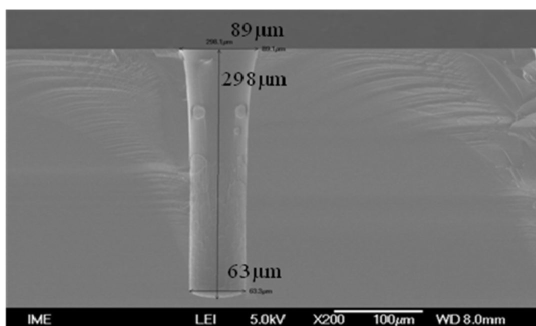

Fig. 5: SEM image of fabricated TSV (300 µm deep)

Fig. 5 shows the SEM image of fabricated TSV. The dimensions of TSV are 300 µm in depth, 60 µm in diameter at via bottom and 90 µm in diameter at via opening. The vias were then passivated with thermal oxide and fully filled with copper by electrolyte plating after depositing a seed layer of Ti/Cu. The seed and electroplating processes are very critical for TSV fabrication. Fig. 6 shows the close-up of seed layer deposited on TSV. It is observed that the entire TSV surface was well covered with seed. The minimal thickness of seed was measured to be more than 200 nm at the bottom of via, which was sufficient for electroplating process.

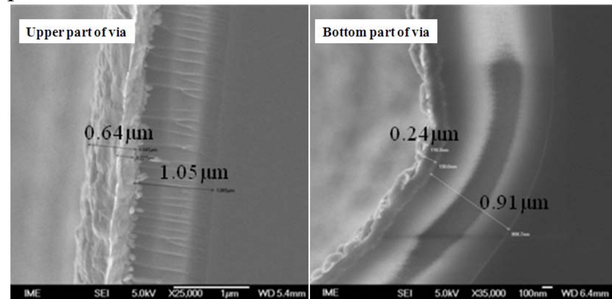

Fig. 6: SEM image of Ti/Cu seed on the sidewall of vias

In the cap wafer, double side RDL and passivation was processed to realize the TSV interconnection from bottom to top of the cap. Wafer level capping was achieved with optimized AuSn transient liquid phase (TLP) bonding method with void free sealing ring. Fig. 7 shows the cross section view of the bonded cap and substrate wafer, with TSV interconnects and solder. The 9 µm-thick Au/Sn solder formed the interrmetallic compound (IMC) after bonding process. The close up shows the copper TSV filling, and there were no voids in the via or the interface between the copper and barrier layer.

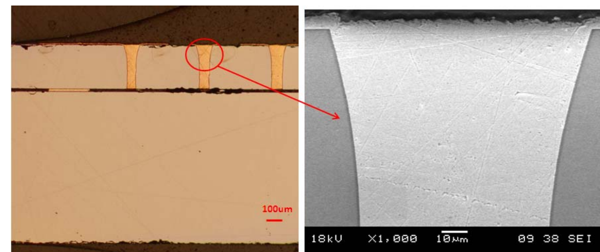

Fig. 7: Cross section view of package structure with TSV and sealing ring solder.

MEASUREMENT RESULTS

The different models were fabricated and characterized. Figs. 8(a)-(b) show some of the fabricated designs. RF measurements were performed from 0.1-40.1 GHz, with 201 data points. A Short-Open-Load-Through (SOLT) calibration was done using Infinity GSG-250 µm probes. From the results in Fig. 9, a slight resonance is observed at 13 GHz for Model 1. Improving the grounding further extends the resonance to 16 GHz and 17 GHz (Models 2 and 3). The *S21* for Model 4 yields a wideband 3D package with a bandwidth up to 26.5 GHz. In general, good correlations were obtained between measurement and simulation results (Figs. 10-11). The correlation could be improved by considering higher conductivity values of the HRSi used for the substrate and cap, due to the presence of surface charges [3]. With respect to Model 4, the measured insertion loss is 0.6 dB and 0.7 dB at 2.5 GHz and 10 GHz respectively. By considering the loss of a CPW line of the same length, the

de-embedded loss per TSV transition is 0.04 dB and 0.05 dB at frequencies of 2.5 GHz and 10 GHz (Fig. 12).

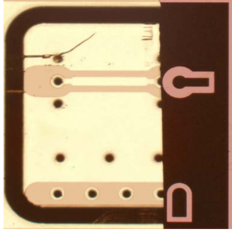

Fig. 8(a): View of cap wafer and 1mm line

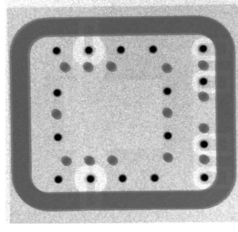

Fig. 8(b): X-ray image of TSV Model 4

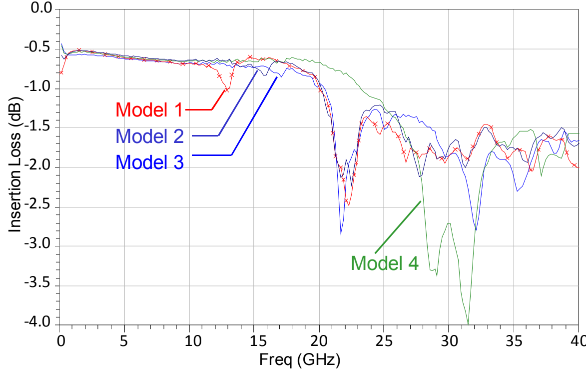

Fig. 9: Measured loss for TSV Models 1 to 4

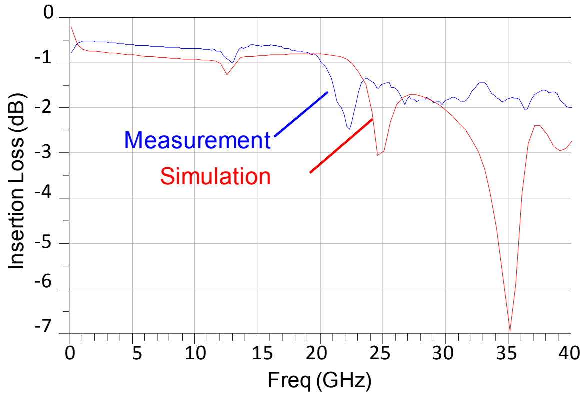

Fig. 10: Correlation of results for TSV Model 1

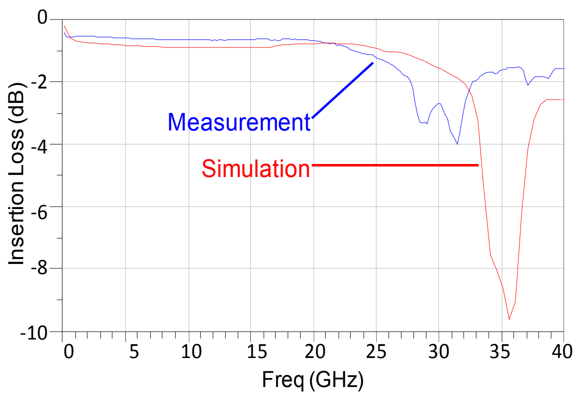

Fig. 11: Correlation of results for TSV Model 4

TSV CHARACTERISTICS

Without designing for any special test structures, the RLGC parameters [4] for the TSV transition were also

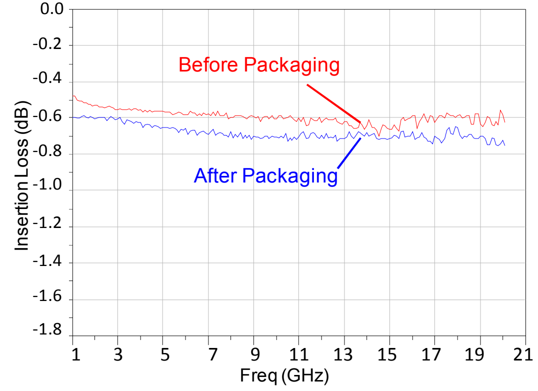

Fig. 12: Loss before and after packaging (TSV Model 4)

extracted. This is done by utilizing an equivalent circuit model of the TSV transition represented by its RLGC parameters. The structure in Model 1 having the TSV transition in a GSG configuration was considered for the extraction (Fig. 3(a)). In the equivalent circuit, L_{via} refers to the self-inductance of the via, and the resistance is represented by R_{via}. C_{via_oxide} refers to the oxide capacitance between the via and the silicon while the capacitance between the vias is represented by $C_{silicon}$. $R_{silicon}$ refers to the conductance of the silicon substrate.

Prior to extraction, the RLGC values were first estimated using empirical formulas. These calculated values serve as ballpark figures for the extraction. From the measurements, the results for a plain CPW line were cascaded with the equivalent RLGC circuits representing the TSV transitions. To obtain the actual TSV characteristics, the overall cascaded circuit was fitted to the measured S-parameters of the full structure (Fig. 13). The final RLGC values obtained from the matching are shown in Table II. From the table, the matched values were observed to be within proximity of the calculated values, with the same order of magnitude. In addition, a good correlation was obtained between the equivalent circuit and the measured results for the S-parameters *S11* and *S21*, up to the linear region of 12 GHz (Figs. 14-15).

Table II. Extracted parameter values from equivalent circuit

	L_{via}	C_{oxide}	$C_{silicon}$	$R_{silicon}$	R_{dc}	R_{ac}
Calc.	0.35 nH	3.37 pF	17.3 fF	-	0.047 Ω	0.053 Ω
Equiv. Ckt.	0.21 nH	2.2 pF	95 fF	231.5 kΩ	0.045Ω	0.058Ω

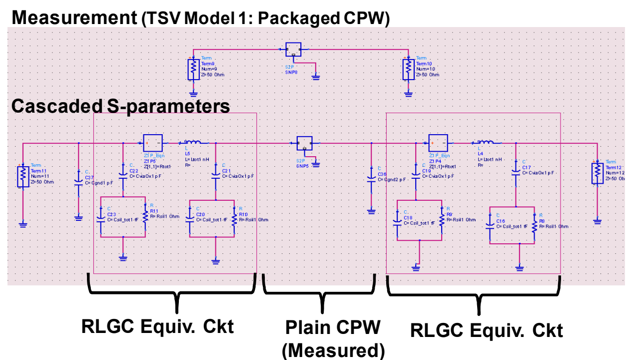

Fig. 13: Equivalent circuit used for RLGC extraction

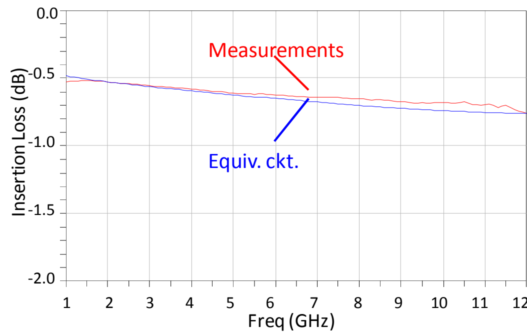

Fig. 14: RLGC extraction using TSV Model 1(S21)

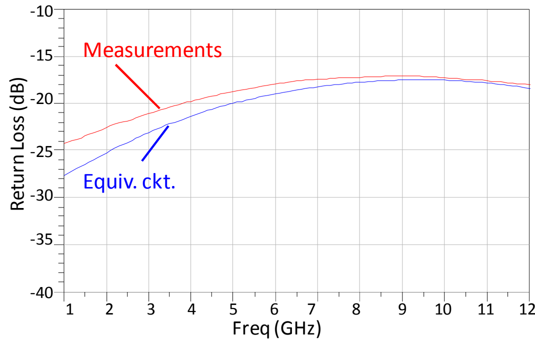

Fig. 15: RLGC extraction using TSV Model 1 (S11)

MILLIMETER WAVE ANTENNA

The TSV transition was also utilized to design a CPW-to-microstrip aperture coupled antenna [5] operating at 94 GHz. The energy is coupled electromagnetically from the CPW feed to the patch antenna. The design was done with the aid of a 3D electromagnetic simulator. The antenna dimensions for resonance are 550 µm x 260 µm, with the 3D model shown in Fig. 16(a). The antenna performance was determined by probing on the pads on the top metal layer (cap wafer). This leads to a CPW feed line through the TSV transition, which is joined to a slotline section positioned underneath the patch.

The fabricated structure as shown in Fig. 16(b) and was characterized from 60 GHz to 110 GHz using LRRM (Line-Reflect-Reflect-Match) calibration and 100 µm pitch probes. From the results in Fig. 17, the measured -10 dB impedance bandwidth spans from 86 GHz to 100 GHz. A good correlation trend is achieved between simulation and measured results, with a maximum gain of 2.9 dBi.

CONCLUSIONS

The main points of this work are summarized below:

- Wideband MEMS packages were achieved by optimizing the grounding configuration in the TSV packages. To our best knowledge, this is the first time the RF performance based on an actual device layout in a TSV package is studied. The optimized model has a bandwidth of 26.5 GHz and a package loss of 0.1 dB at 10 GHz.

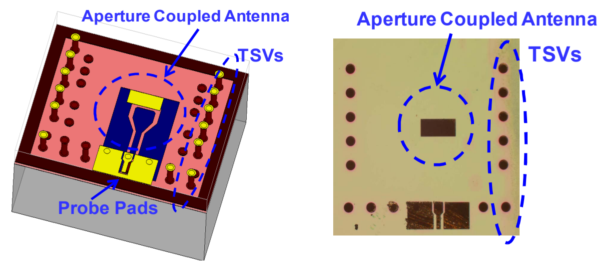

Fig. 16(a): Antenna Design *Fig 16(b): Fabricated antenna (Top view)*

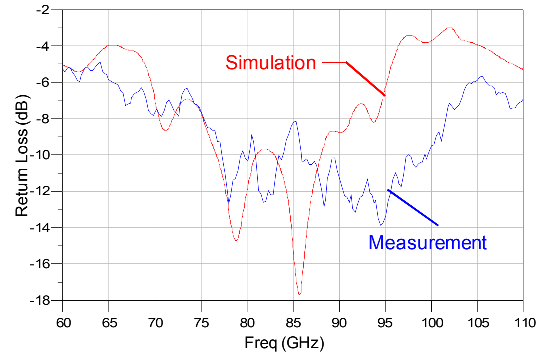

Fig. 17: Return loss of millimeter wave antenna

- The RLGC parameters of TSVs in a GSG configuration were extracted from measurements up to 12 GHz.
- Based on the TSV transition, a 94 GHz antenna was fabricated. The measured -10dB bandwidth is 14 GHz with a maximum gain of 2.9 dBi.

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