T3P.007

DESIGN AND IMPLEMENTATION OF A NOVEL CMOS MEMS CONDENSER MICROPHONE WITH CORRUGATED DIAPHRAGM

Chien-Hsin Huang[1,2]*, Ming-Han Tsai*[3]*, Chien-Hsing Lee*[4]*, Tsung-Min Hsieh*[4]*, Jhyy-Cheng Liou*[4]*,*
Li-Che Chen[2]*, Ming-Chuen Yip* [1]*, and Weileun Fang*[1]
[1]Power Mechanical Engineering, National Tsing Hua University, Hsinchu, Taiwan
[2]United Microelectronics Corp., Hsinchu, Taiwan
[3]Institute of NanoEngineering and MicroSystems, National Tsing Hua University, Hsinchu, Taiwan
[3]Solid State System Corporation (3S), Hsinchu, Taiwan

ABSTRACT

This study reports a CMOS-MEMS condenser microphone implemented using the standard thin films stacking of 0.35μm UMC CMOS 3.3/5.0V logic process, and followed by post-CMOS micromachining steps without introducing any special materials. The corrugated diaphragm for microphone is designed and implemented using the metal layer to reduce the influence of thin film residual stresses. Moreover, silicon substrate is employed to increase the stiffness of back-plate. Measurements show the sensitivity of microphone is -42±3*dBV/Pa* at 1kHz under 6V pumping voltage, the frequency response is 100Hz-10kHz, and the *S/N* ratio >55*dB*. Table1 summarizes detail specifications.

KEYWORDS

CMOS-MEMS, condenser microphone, corrugated, sensitivity, diaphragm

INTRODUCTION

Presently, the microphone becomes an important component for various portable consumer electronics. In these applications, size and cost are two critical concerns for the microphone. Silicon based MEMS microphones offer small size, low cost, and ease of integration with CMOS, while its fundamental challenges in acoustic applications are to increase performance, reliability, and capability. The less interference, better sound quality, higher sensitivity, higher signal to noise ratio, less current drain, and low distortion are the goals to achieve MEMS microphones.

There are various small size and low cost microphones realized by different MEMS technologies have been reported in [1]. Moreover, the MEMS microphone is also compatible with the surface mount process [2]. The mature and foundry available CMOS process is also considered as a promising approach to implement the MEMS microphone. In this regard, the MEMS microphone and its signal processing IC can be monolithically integrated on a single chip. Thus, the parasitic capacitance can be reduced to enhance the signal-to-noise ratio of a condenser microphone. The IC/MEMS monolithic integrated condenser microphone implemented by available CMOS foundry has been demonstrated in Akustica [3]. However, the deposition of polymer film is required. This is not a standard material for CMOS process.

In general, the CMOS-MEMS microphone design, such as the shape and dimensions of the diaphragm, backplate, and air gap are limited by the standard CMOS process. Thus, the performance of CMOS-MEMS microphone is also restricted by the process. This study presents the design and implementation of a novel CMOS-MEMS condenser microphone based on the standard UMC (United Microelectronics Corp., Taiwan) CMOS process on 8-in wafer. In addition, the post-CMOS bulk and surface micromachining processes are also performed in foundry. Such condenser microphone consists of a corrugated diaphragm [4-6] and a stiff back-plate to improve its performances.

CONCEPT AND DESIGN

Fig.1 shows the schematic illustration of the proposed CMOS-MEMS capacitive microphone which consists of the diaphragm, air gap, silicon back-plate, vent holes, back chamber, and sensing circuits. The movable electrode on diaphragm and the stationary electrode on back-plate form a parallel capacitor. The sound pressure on microphone will cause the deformation of diaphragm, and leads the capacitance change of parallel capacitor. The corrugated diaphragm is designed to reduce its stiffness and also release the thin film residual stresses [4-6]. Moreover, the thick back-plate is designed to increase its stiffness. Thus, the deformation of stationary electrode by the sound pressure can be prevented. The vent holes are also prepared on the thick back-plate. The key parameters of the microphone design are listed in Table 1.

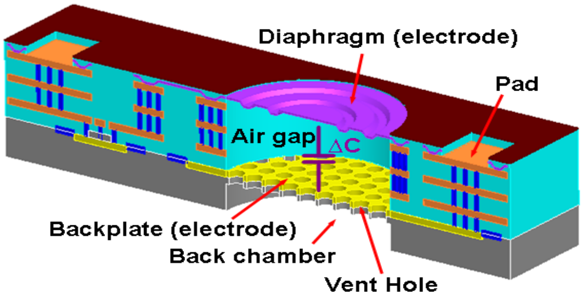

Figure 1 The proposed CMOS MEMS microphone design.

Table 1 Microphone critical dimensions and parameters

The parameter of microphone simulation			
Diaphragm diameter	*800μm*	*Air hole*	*20μm*
Diaphragm density	*2500kg/m^3*	*diameter*	*350*
Diaphragm thickness	*1.1μm*	*Air hole quantity*	*22%*
Elastic of diaphragm	*21.2Gpa*	*Hole ratio*	*1.8 kg/m^3*
Diaphragm stress	*41.63MPa*	*Air density*	*1.73×10^{-5}N-s/ m^2*
Diameter of backplate	*800μm*	*Viscosity of air*	*6V*
Backplate thickness	*40μm*	*Bias voltage*	*0.7pF*
Initial air gap	*4.2μm*	*Parasitic cap.*	

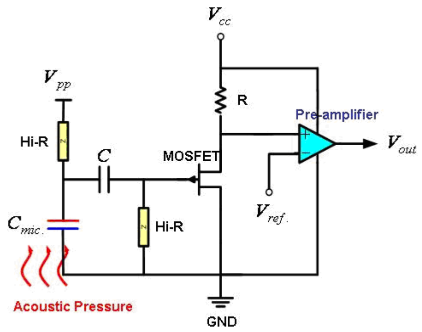

Figure 2 Schematic of the amplifier circuit of fabricated condenser microphones.

The device is designed based on the standard 0.35μm UMC CMOS 3.3/5.0V logic process. The metal-4 layer is employed to fabricate the diaphragm. The corrugate diaphragm structure is designed to release the residual stress of metal film. Note that such large area corrugate metal diaphragm violates the design rule of the UMC process. The silicon substrate is used to increase the thickness and stiffness of the back-plate, so as to prevent its deformation caused by the sound pressure. As indicated in Fig.1, the amplifier circuit is monolithically integrated with the microphone. Fig.2 shows the amplifier circuit design. The capacitive microphone is charged by an external pumping voltage V_{pp} from V_{cc}. As the acoustic pressure introduced to the microphone, the vibration of diaphragm will cause the capacitance change between diaphragm and back-plate.

FABRICATION PROCESS

Fig.3 shows the process steps to fabricate the CMOS MEMS microphone in the foundry UMC on 8-in wafer. The processes consist of the standard UMC 0.35μm 1-poly 4-metals 3.3V/5.0V logic device process and the post-CMOS MEMS structure releasing process. Fig.3a indicates the layers stacking prepared by the UMC CMOS process. In this process, there were totally four metal films, named metal-4 to metal-1. The metal-4 film was patterned as the corrugated structure to meet the design requirement for microphone diaphragm. Such corrugated structure also has the potential to prevent the stiction between the diaphragm and back-plate, as the air gap been reduced. Moreover, the dielectric films were employed as the sacrificial layers. Moreover, the rest three metal layers and tungsten vias are used as the electrical routings.

After completing the CMOS process, the backside of silicon substrate was thinned by grinding process, and then etched by DRIE, as shown in Fig.3b. Thus, the vent hole of the microphone was defined. In order to avoid the deformation due to the sound pressure in the back-plate, silicon is introduced into the back-plate to enhance the structure stiffness. As shown in Fig.3c, the 2nd DRIE was used to fabricate the back chamber and also define the thickness of the back-plate. Finally, the sacrificial dielectric layers were removed by wet etching to release the diaphragm from the silicon substrate, as illustrated in Fig.3d. In this process, the SiN was used as the protection layer for wet etching.

The SEM micrograph in Fig.4a shows the top view of a typical fabricated microphone chip. The diaphragm of 800 μm diameter and the bonding pads are observed. Fig.4b shows the associated CMOS circuit and MEMS layout for the chip in Fig.4a. It also indicates the monolithic integration of the MEMS microphone and the signal processing circuits. The cross section SEM micrograph in Fig.4c shows the thin corrugated diaphragm, air gap, thick back-plate with vent holes, and backside chamber of a typical fabricated microphone.

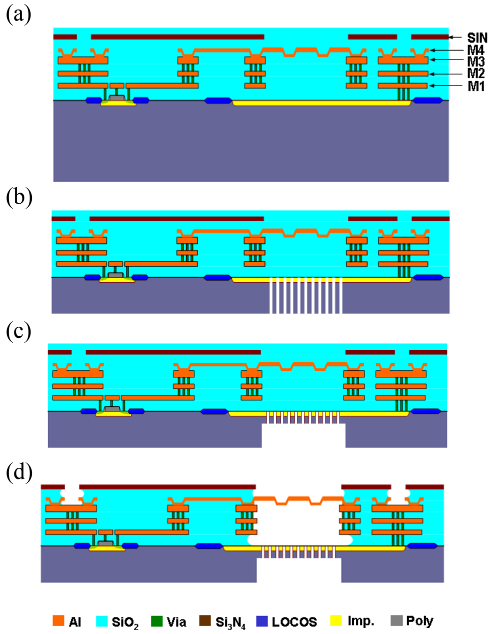

Figure 3 (a) Front-side UMC 0.35μm 1P4M standard CMOS process, (b) Back-side grinding and vent hole DRIE, (c) Back chamber DRIE, (d) Microphone sacrificial layer etching.

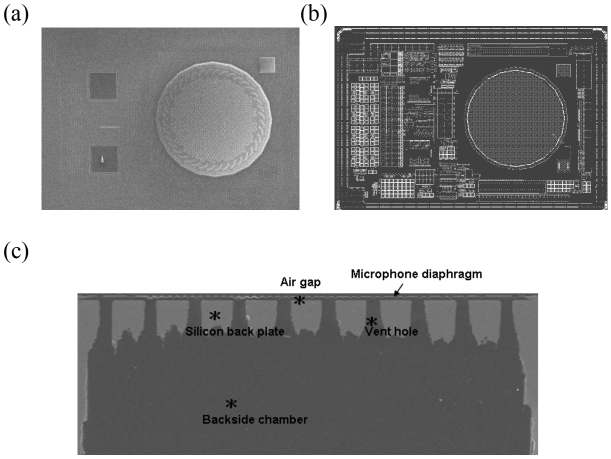

Figure 4 (a-b) The top view SEM micrograph of a typical fabricated CMOS MEMS microphone and its associated CMOS circuit and MEMS layout (c) The side view SEM micrograph of a fabricated microphone.

MEASUREMENT RESULTS

The microphone was characterized using the voltage driving test. Fig.5 shows the test setup for C-V measurement which contains a probe station, HP-4284A precision LCR meter and HP4156B semiconductor parameter analyzer. The typical C-V measurement results in Fig.6 show the capacitance change of microphone at different driving voltages. In addition, the microphone exhibits an initial capacitance of 1.48pF at zero bias.

The microphone was packaged as shown in Fig.7a, and then performed the sensitivity tests by the pulse electro-acoustics in an anechoic box. The measurement setup for sensitivity test is schematically illustrated in Fig.7b. Measurements show the typical sensitivity of microphone is -42dBV/Pa at 1 kHz and the bandwidth is larger than 10 kHz, as indicated in Fig.8 and Fig.9. The simulations agree well with the measurements. The microphone also has a preliminary *S/N* ratio of >55dB. Detail measured specifications are summarized in Table2.

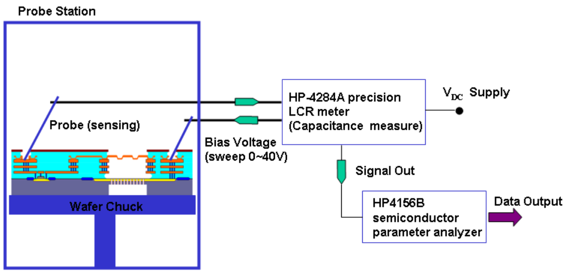

Figure 5 The test setup for C-V characterization.

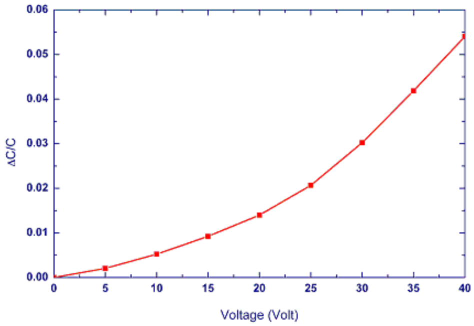

Figure 6 Measured capacitance sensitivity of a typical fabricated microphone

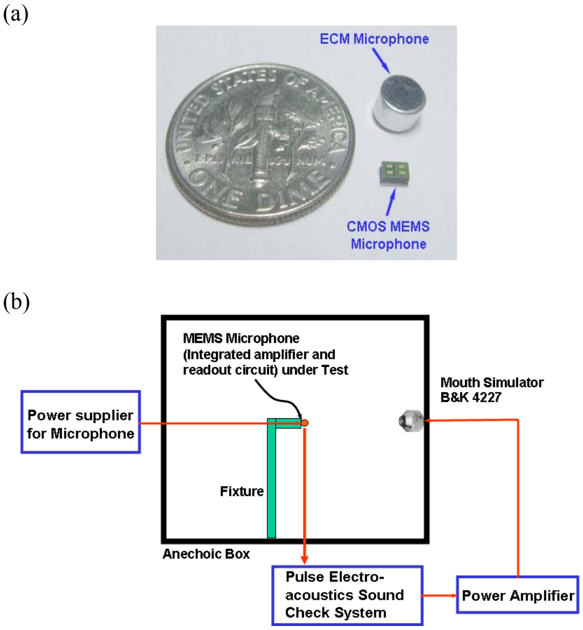

Figure 7 (a) The microphone after packaging, and (b) the setup of microphone sensitivity test.

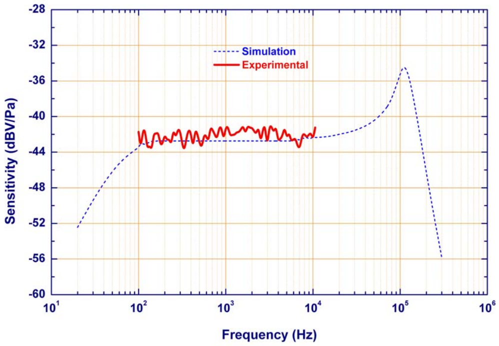

Figure 8 The predicted and measured frequency responses of the presented MEMS microphone

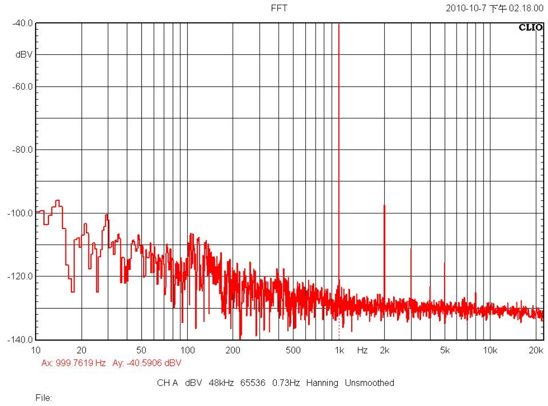

Figure 9 A fast Fourier transform (FFT) @ 1kHz.

Table 2 Measured specifications of packaged microphone

The measured specifications of the packaged microphone			
Size L×W×H	2.35×1.65×1.2mm	*Out impedance*	<350Ω
Operation voltage	1.65~3.6V	*PSRR*	-60dB
Sensitivity (1kHz)	-42±3dBV/Pa	*THD@115dB*	<10%
Frequency response	100~10kHz	*THD@100dB*	<1%
S/N ratio	>55dB	*Operation Temp.*	-40~85□
Current consumption	<200μÅ		

CONCLUSIONS AND DISCUSSIONS

This study presents the design of a CMOS-MEMS microphone consisting of corrugated metal diaphragm with 800μm in diameter, and rigid thick back-plate. Moreover, the tests demonstrate the performances such as sensitivity and frequency range of the device. The microphone has flat frequency response from 100Hz to 10kHz, and sensitivity of -42±3dBV/Pa at 1kHz (the reference sound-level is 94dB). Moreover, the microphone has current consumption of less than 200μÅ, the S/N ratio of over 55dB, and low distortion of <1% (refer to 100dB). In short, this study demonstrates the possibility of implementing the CMOS-MEMS microphone by establishing and integrating the standard CMOS and post-CMOS release processes in existing foundry. This could be a critical step for the mass production of MEMS devices in a CMOS foundry.

Nevertheless, it is not straightforward to integrate the proposed MEMS microphone with circuit by standard CMOS process on 8-in wafer. The design of MEMS devices is limited by the standard CMOS process. Moreover, various problems and limitations should be considered by using the standard CMOS process, (1) the materials available for MEMS structures are limited to the thin films for backend processes (i.e. metal1~4, dielectric, and tungsten); (2) wafer warpage will cause the handling problem during backend process; (3) large metal pattern could lead to electrical arcing during via etching and causing the wafer burned; (4) thermal budget for post-CMOS process has to be considered to avoid electrical shift of MOSFET; and (5) metal hard mask during sacrificial layer etching should be prevented to reduce the parasitic capacitance.

ACKNOWLEDGEMENTS

The authors would like to thank Professors M-H Peng and J.H. Wang of National Tsing Hua University for the suggestions of simulation, design and acoustic test.

REFERENCES

[1] P. R. Scheeper, A. G. H. Van der Donk, W. Olthuis, and P. Bergveld, “A review of silicon microphones,” *Sensors and Actuators A*, vol. 44, pp. 1-11, 1994.

[2] J. W. Weigold, T.J. Brosnihan, J. Bergeron, and X. Zhang, “A MEMS Condenser Microphone for Consumer Applications,” *IEEE MEMS'06*, Istanbul, Turkey, pp.86-89, 2006.

[3] J. J. Neumann, and K. J. Gabriel, “CMOS-MEMS membrane for audio-frequency acoustic actuation,” *Sensors and Actuators A*, pp. 175-182, 2002.

[4] P. R. Scheeper, and W. Olthuis, “The design, fabrication, and testing of corrugated silicon nitride diaphragms,” *J. of Microelectromechanical Systems*, Vol. 3(1), 36-42, 1994.

[5] Van Mullem, C. J., Gabriel, K. J., and Fujita, H., “Large deflection performance of surface micromachined corrugated diaphragms,” *Transducers'91*, pp.1014-1017, 1991.

[6] J. Chen, L. Liu, Z. Li, Z. Tan, Y. Xu, and J. Ma, “Single-Chip Condenser Miniature Microphone with High Sensitive Circular Corrugated Diaphragm,” *IEEE MEMS'02*, Las Vegas, NV, pp. 284-287, 2002.

CONTACT

*W. Fang, Tel：+886-3-5742923；fang@pme.nthu.edu.tw