WAFER RECONSTITUTION WITH PRECISION DRY FRONT-TO-FRONT REGISTRATION

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ABSTRACT

This paper demonstrates a dry heterogeneous integration process for embedding CMOS chips into a partially-complete MEMS silicon wafer. By using standard IC processing, we create passive alignment structures in backside cavities on the MEMS wafer. The precision dry assembly utilizes front-to-front registration, removing the need for sidewall slope control of the backside Deep Reactive Ion Etch (DRIE). With dummy dice emulating CMOS chips, we show better than ±3μm alignment in both the x- and y-directions after manual die insertion. This process allows formation of high density and low parasitic contacts between the embedded chips and wafer, by sputter deposition of metal to form vias and interconnects.

KEYWORDS

Wafer reconstitution, self alignment, heterogeneous integration, passive assembly.

INTRODUCTION

Integration of CMOS and MEMS not only promises smaller package sizes, but also shorter interconnects for increased sensor sensitivity or higher frequency performance. Compared to MEMS-first, MEMS-last, and CMOS-MEMS techniques, heterogeneous integration of CMOS and MEMS allows marriage of two fabrication processes that are often incompatible in terms of substrate material, substrate size, and thermal budget. However, without the lithographic alignment available in the co-fabrication route, another mechanism is needed to achieve comparably fine alignment, thus preserving the advantages of tight integration.

Work in [1] arrives at the fine alignment goal by means of capillary-based fluidic self-assembly. Motivated by the integration paradigm of backside insertion for a front-to-front alignment, we aim to rely on dry assembly instead. The goal is to maintain co-fabrication levels of low parasitic capacitance and high interconnect density, without fluidic self-assembly, while remaining amenable to batch parallel processing after insertion.

In Figure 1, we show the concept of this integration scheme. Foundry CMOS dice can be distributed on a pusher wafer, with their positions matching that of receiving pockets on the MEMS wafer. The entire collection could then be batch-assembled in one step, with passive self-alignment giving the final precision, resulting in favorable scale-up for production throughput.

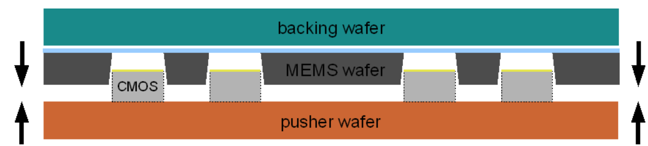


Figure 1: Concept of dry heterogeneous integration. CMOS chips are distributed on a pusher wafer. They are inserted into receiving cavities on the MEMS wafer in a batch step. The final precision is by passive self-alignment.

CONCEPT

A key part in this integration scheme is achieving precision dry assembly by using passive guide tabs, which protrude from the insertion cavity walls, as shown in Figure 2A. While the insertion cavities are backside features, the guide tabs are front-side features. This distinction allows us to decouple backside lithographic alignment and backside DRIE sidewall slope from alignment after assembly, giving precision comparable to that from front-side lithography.

As can be seen in Figure 2(a), this scheme assumes that CMOS foundry chips are precision-diced to micron accuracy or better. This may be achieved by utilizing chips from the same saw dicing lot, or by the various laser dicing techniques available. The dicing edges form the CMOS side of the alignment fit. Nevertheless, if precision dicing is not available, we can still create precision notches on the chips with DRIE or other micromachining steps, as shown in Figure 2(b).

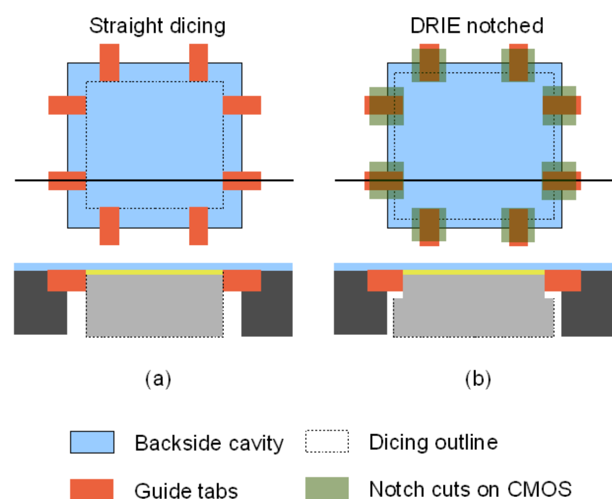


Figure 2: (a) Front-side precision alignment by guide tabs embedded in backside cavity sidewall, with precision dicing. (b) Alternative with notch etch on CMOS dice, for when dicing precision is not sufficient.

For demonstration of this integration scheme, we created dummy chiplets by DRIE to emulate precision commercial dicing. The dummy chiplets, shown in Figure 3, have aluminum traces for testing contacts and quantifying assembly alignment.

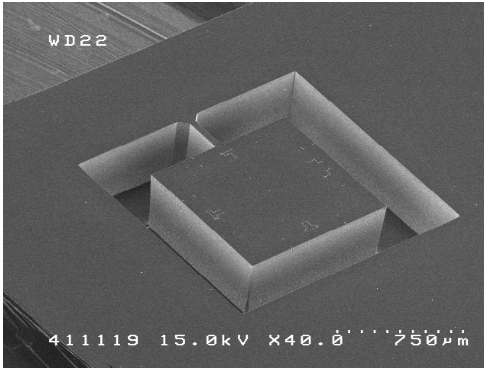


Figure 3: Dummy dice created by DRIE, with snap-out tethers.

A goal of this heterogeneous integration process is to minimize the overhead needed to provide the frontside registration features on the MEMS wafer, while achieving high-precision alignment. Compared to approaches where the backside DRIE sidewall is the sole alignment feature [2], our approach could yield sub-µm alignment precision. The cost is a single additional mask and the process steps to form the guide tabs. The resulting high precision allows the MEMS side to be partially or nearly complete before the assembly step. The tuning of the backside DRIE sidewall angle in [2] is no longer necessary. The sidewall assembly gaps after insertion can be sealed by backside PECVD of SiO_2, which has fast deposition rates over 1µm/minute. There are no requirements on the CMOS side, besides dicing precision or presence of precision notches. Integration of exotic non-CMOS circuitry chips for higher performance is also possible.

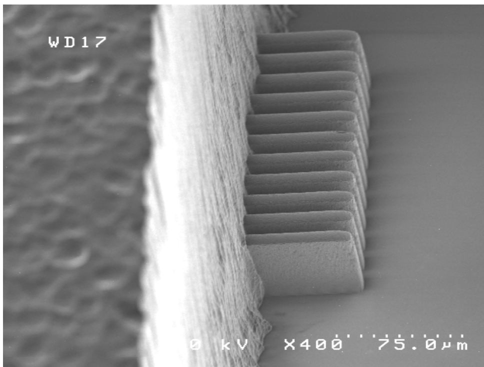
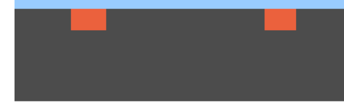


Figure 4: SEM photo of finished guide tabs, viewed from cavity opening. The fins are mainly polysilicon, with oxide cladding to withstand the backside DRIE.

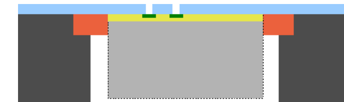
(a)



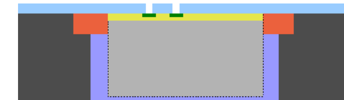
(b)

(c)

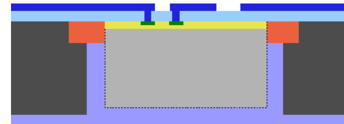
(d)



(e)



(f)



(g)

Guide gabs
CMOS pads
MEMS top metal
PECVD SiO_2 fill
MEMS membrane stack

Figure 5: (a)Trench etching, refilling, and etch back to form damascene guide tabs. (b) Fabricate membrane stack. (c) Etch contact holes. (d) Backside DRIE to form insertion cavities, also exposing guide tabs. (e) Insert CMOS chips or dummy chiplets. (f): Fill backside gaps with conformal PECVD SiO_2. (g) Sputter metal to form vias and pattern final metal.

FABRICATION

The fabrication process starts by DRIE etching of guide tab trenches into the MEMS wafer. The target trench depths

are 50-100µm. Instead of solitary trenches 100's of µm wide, the guide tabs trenches are composed from arrays of narrower high-aspect ratio (~10:1) trenches, to allow for damascene refill. The trench widths are chosen to be 6-8µm, a tradeoff between deposition thickness required for refill, and the fragility of the guide tabs.

The guide tab trenches are first clad with CVD oxide, and then refilled by un-doped CVD polysilicon, which is highly conformal. An isotropic silicon RIE is performed, stopping on oxide to create damascened guide tabs fins (Fig 4). The earlier oxide cladding will protect the guide tab fins in the later backside DRIE step. At this point the MEMS wafer has sufficiently flat topography for further lithography steps.

With the guide tabs completed and embedded (Fig. 5A), the wafer is ready for any high temperature or non-standard MEMS processing. The only requirement is that the membrane stack be substantial enough at and near the assembly cavity regions. For this demonstration, we use a membrane stack of oxide and nitride. (Fig. 5B)

Contact holes are then etched in the membrane stack (Fig. 5C). These will become the metal vias after assembly and the final interconnects are completed.

Backside DRIE, not-critically aligned to the front-side guide tabs, creates the insertion cavities (Fig. 5D), and exposes the guide tabs. The backside cavity features are about 25µm oversized, in relation to the guide tabs and intended chip size. The extra tolerance allows for any backside lithography misalignment (often 5-10µm on the un-calibrated contact aligner tool used), is insensitive to a DRIE sidewall taper, and facilitates manual assembly.

After insertion of dummy chiplets (Fig. 5E), backside gaps will be sealed by ~20µm of conformal PECVD oxide (Fig. 5F). Aluminum will then be sputtered and patterned [8], forming "rivets" connecting the chiplets to the wafer (Fig. 5G). Note that the need to sputter frontside contacts means that process does not achieve true vertical integration.

With the completion of this integration process module, the wafer can go through further MEMS processing if needed, for example, the MEMS structure release. However the thermal budget limit for the embedded CMOS dice needs to be observed.

CHIP INSERTION

During assembly, the MEMS wafer with insertion cavities is flipped over, and is given a backing wafer underneath to support the membranes (Figure 6). The dummy dice are made by DRIE, with snap-out tethers for on-demand use, as already shown in Figure 3.

The insertion is performed by hand tweezers working under a stereoscopic boom microscope at 10-15x magnification (Fig 7). This assembly setup in untrained hands has only enough precision to bring the chiplets just inside the cavity site openings, which have 25µm (1mil) of side clearance. Once the chiplets are engaged with the cavity opening, gravity drop-in completes the process, with about 300-500µm of drop, depending on wafer thickness. This intentionally crude manual assembly demonstrates feasibility of a batch parallel insertion, where a rough pick-and-place tool, or a self-assembly technique places chips on a pusher wafer in vicinity of the final alignment positions.

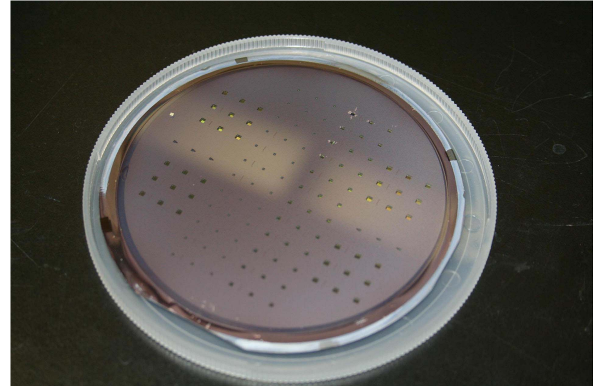


Figure 6: Photo of wafer with insertion cavities, backside facing up. Backing wafer is underneath but not visible.

Figure 7: Assembly experiment setup, with microscope and assorted tweezers for chip placement.

RESULTS AND DISCUSSION

Preliminary results of the precision assembly are shown in Figure 9. The dummy chiplet is 1mm×1mm, with a matching cavity. The guide tabs are ~55µm in depth. From the matching alignment marks on chip and membrane, the misalignment is less than 3µm in both x and y directions.

For contrast, Figure 8 shows example of an insertion cavity without guide tabs. The impressions of guide tabs (had they existed) have been etched into the membrane to illustrate alignment. The dummy chiplet can be seen to be constrained only by the cavity sidewall, which is not only oversized but with rounded corners from etching.

Note the jagged edges of DRIE cavity in Figure 9 are due to a leak in our etch chamber eroding the photoresist mask. This also degrades precise definition of chiplet edges and increases final misalignment. However, the edge

precision of guide tabs is not impacted, due to their shorter etch.

Currently there are two main sources of error that limit assembly precision. First is photoresist mask erosion in DRIE, which reduces the dimensions of the dummy chiplets. Second is the lithography misalignment from manual aligners. It remains to be seen whether tightening these tolerances will impact ease of assembly.

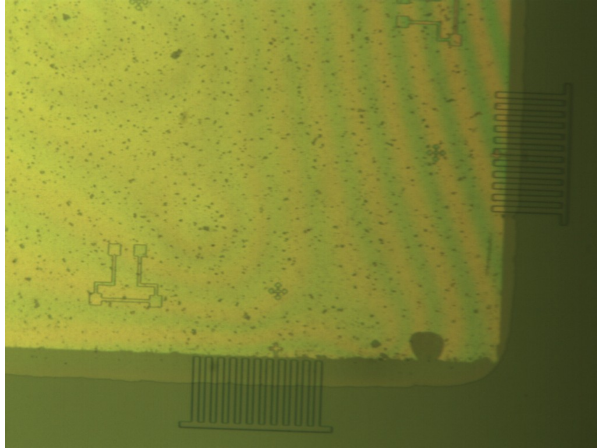


Figure 8: Example of assembly for cavity without guide tabs. Guide tab dimples are etched into membrane to show alignment.

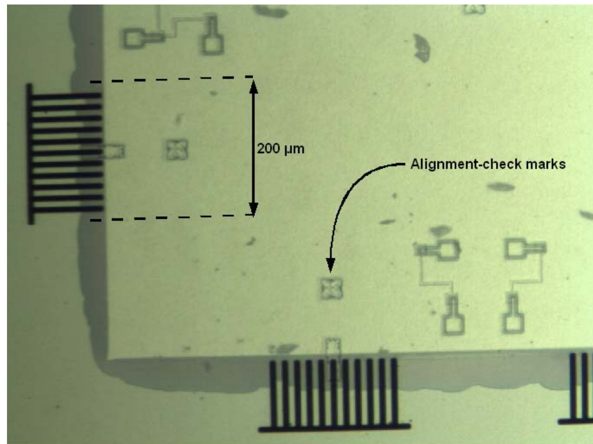


Figure 9: Example of assembly for cavity with guide tabs (dark combs). Alignment is well-constrained.

The final metal interconnects are currently in fabrication. We have confirmed metal bridging of up to 1µm gaps between the membrane and the chip.

CONCLUSION

We have demonstrated better than 3µm precision alignment of chips inserted into wafer cavities. By adding front-side guide tabs, this assembly process is dry and self-aligned.

Batch parallel embedding of CMOS for wafer-level heterogeneous integration, such as our approach, is attractive for MEMS to take full advantage of fine-line CMOS. With larger-scale integration of MEMS devices [4], the density and parasitics of the interconnects become a concern. In particular, RF MEMS resonators, due to motional impedances inherently higher than 50Ω, stand to benefit from smaller pads and shorter traces to supporting circuitry.

ACKNOWLEDGEMENTS

Device fabrication was done in the Stanford Nanofabrication Facility (a member of the National Nanotechnology Infrastructure Network) supported by the NSF under Grant ECS-9731293. The research is supported by Analog Devices, Inc., and the DARPA Center for Interfacial Engineering for Micro-electromechanical Systems (CIEMS) under DARPA grant HR0011-06-0049 (Dr. D. L. Polla, Program Manager).

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