WAFER LEVEL PACKAGING OF MEMS

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ABSTRACT

Wafer level packaging methods of MEMS are described. These play important roles to reduce cost and to improve reliability. MEMS structures on silicon chips are encapsulated with bonded caps or with shells fabricated by surface micromachining, and electrical interconnections are made from the cavity. Vacuum packaging methods are also described.

KEYWORDS

Wafer level packaging, MEMS, bonding

INTRODUCTION

Packaging to encapsulate and to make electrical interconnections is indispensable for practical applications of MEMS (Micro Electro Mechanical Systems). The process for the packaging prior to dicing is called wafer level packaging. It is recognized that major part of MEMS cost is in the packaging and testing. Because of moving parts of the MEMS, MEMS chips can not be molded directly with plastics. Furthermore MEMS can not be tested on a wafer in many cases and therefore packages lost in the defective MEMS increase the MEMS cost. These problems can be solved by the wafer level packaging [1] [2]. The concept of the wafer level packaging is shown in Fig.1.

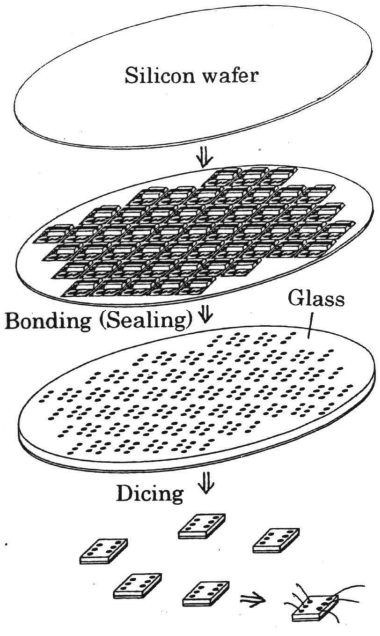


Fig.1: Concept of wafer level packaging.

MEMS are fabricated on a silicon wafer being encapsulated in cavities by bonding a lid wafer to the MEMS wafer or by covering the MEMS with shells. Electrical interconnections from the MEMS in the cavities to the outside are required. A lid wafer with holes for electrical interconnection is used in the case of Fig.1. Finally we get many packaged chips by dicing the bonded wafer. Since the MEMS in the cavity are protected mechanically they are not contaminated during the fabrication process, such as dicing. Many small packaged MEMS are fabricated in batch process and extra equipments for the packaging are eliminated.

Various wafer level packaging methods are summarized in Fig.2. Interfacial bonding methods are from (a) to (e), bonding methods with melting materials are (f) and (g) and deposition sealing methods are from (h) to (j). Examples of these wafer level packaging will be described in this paper.

Vacuum cavity is required for some MEMS devices as resonators or infrared sensors. The vacuum packaging method will be described as well.

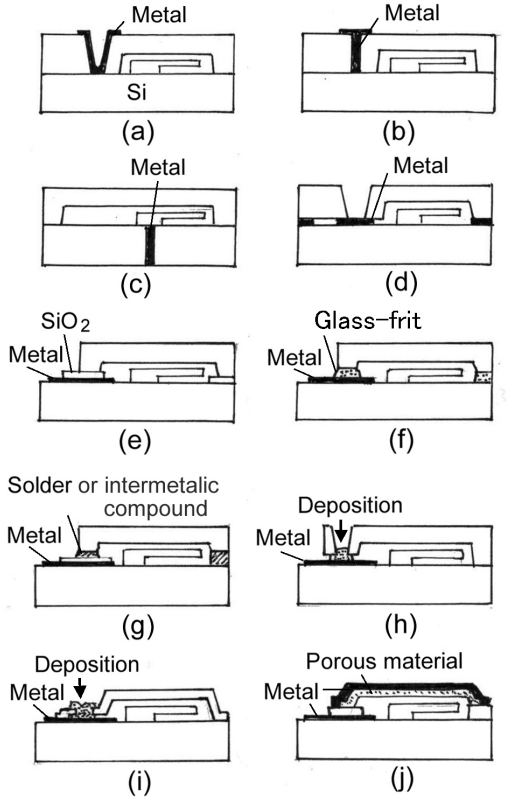


Fig.2: Various wafer level packaging methods.

ELECTRICAL INTERCONNECTION IN GLASS HOLES AFTER BONDING (Fig.2(a))

The fabrication process of an integrated capacitive pressure sensor is shown in Fig.3 [3]. A glass wafer which has holes in it is anodically bonded to the silicon wafer which has CMOS circuits. The glass holes are metalized after making diaphragms by etching the silicon. Finally the bonded wafer is diced into chips. Owing to the integrated CMOS circuit to convert the capacitance to a frequency output, small change of the sensor capacitance can be detected and the sensor has been used for low pressure measurement. Circuit which can stand the anodic bonding process condition with high electric field at 400℃ was studied [4]. It was found that an electrical shielding by metal film on the oxide of pn junction surface could reduce the junction leakage current effectively. Platinum on titanium was used for the metallization on the glass because conventional aluminum metallization causes hillocks during the thermal process of anodic bonding. The hillocks should be avoided for capacitors with a narrow gap. The glass metallization above the circuit was needed for optical shielding from ambient light.

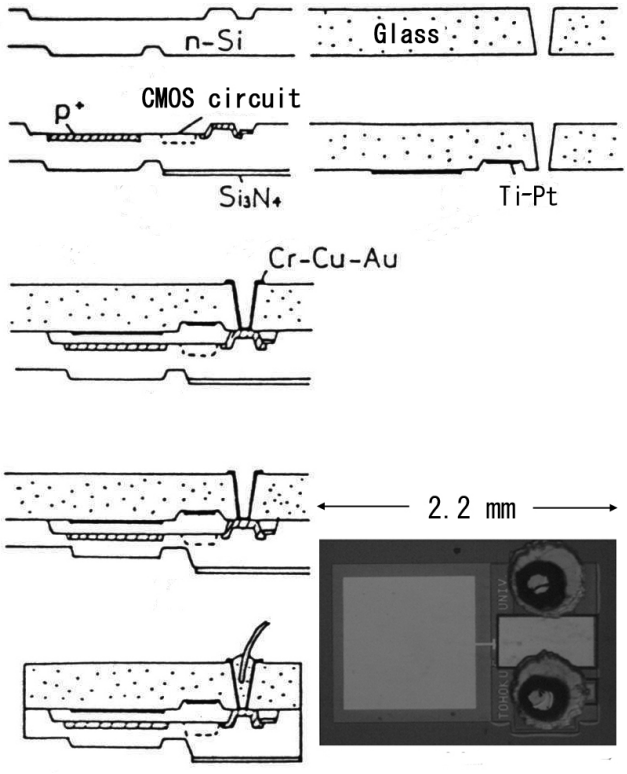


Fig.3: Process of integrated capacitive pressure sensor [3].

The wafer level packaging with holes in the glass was applied to a capacitive accelerometer. The fabrication process is shown in Fig.4 [5]. The etched silicon wafer in which all components are mechanically connected by support as in (Fig.4(a)). It is anodically bonded to a glass wafer (Fig.4(b)) and then the support is etched out by reactive ion etching (RIE) (Fig.4(c)). The wafer is bonded to another glass wafer which has holes for the electrical feedthrough and finally packaged chips are obtained by dicing the bonded wafer (Fig.4(c)). The structural distortion caused by the anodic bonding should be minimized to maintain a narrow gap of the sensor capacitors. Using thick glass symmetrically on both sides and optimizing the bonding temperature can reduce the distortion caused by the mismatch of thermal expansion of the silicon and the glass.

To prevent unexpected sticking of the silicon seismic mass to the glass due to electrostatic attraction, the metal on the glass is electrically connected to the silicon during the anodic bonding process. After the bonding the metal on the glass is disconnected by using YAG laser from the outside through the glass [6].

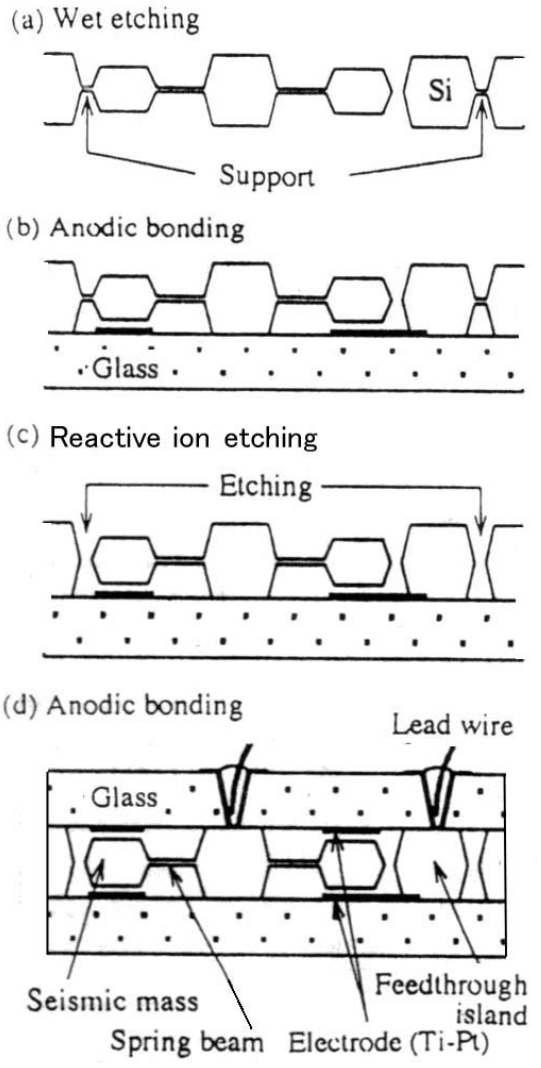


Fig.4: Wafer level packaging process of accelerometer[5].

ELECTRICAL FEEDTHROUGH IN GLASS AND CERAMICS BEFORE BONDING (Fig.2(b))

A glass lid having electrical feedthrough in it was bonded to the silicon wafer. MEMS switch fabricated using the wafer level packaging is shown in Fig.5 [7]. A thermal actuator using different thermal expansion coefficients of metal (cupper) and silicon dioxide was adopted for the switch. The surface of the electrical contact is kept clean because of the wafer level packaging, which results in high reliability and the switch has been used for the latest LSI tester [7].

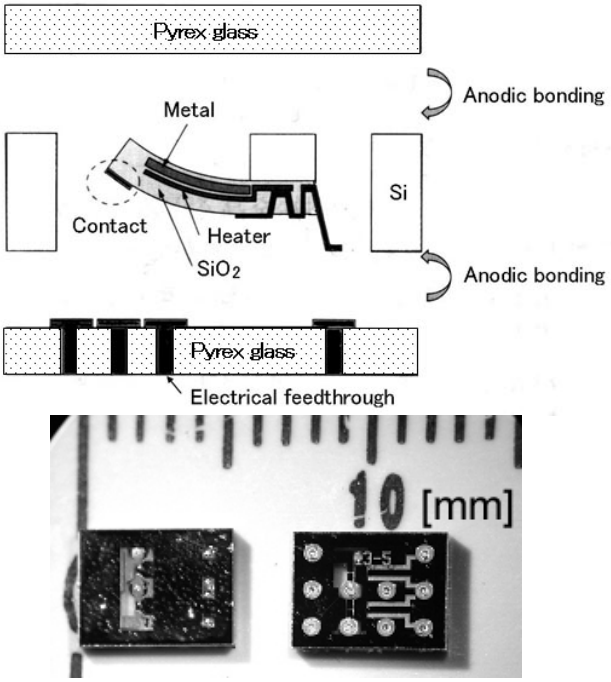
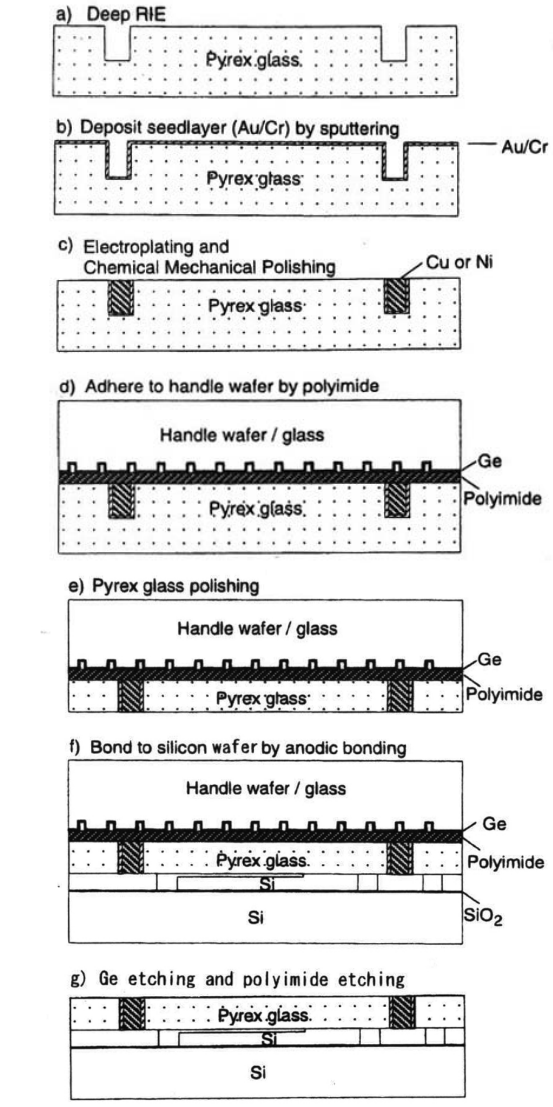


Fig.5: Thermal MEMS switch using electrical feedthrough in glass [7].

Sandblasting, electrochemical discharge drilling, laser drilling [8], ultrasound drilling or mechanical drilling can be applied to make through holes in the glass, however these methods are not batch processes. Deep RIE is suitable for making many holes in batch process, however it is difficult to make deep holes in a glass wafer because the glass etching rate is slow (~0.5μm/min). The deep RIE of the glass wafer has been applied to the wafer level packaging, using a temporary bonding which withstands the temperature for anodic bonding [9]. The process steps are shown in Fig.6. A glass wafer is etched by the deep RIE to make shallow holes (Fig.6 (a)) and the holes are filled with electroplated metal (Fig.6 (c)). After polishing the surface of the glass wafer, it is bonded to a handling wafer with polyimide (Fig.6 (d)). The handling wafer has grooves in it and germanium is deposited on the surface. By grinding and polishing the glass the metal is exposed (Fig.6 (e)) and the glass wafer is anodically bonded to the silicon wafer (Fig.6 (f)). Finally the handling wafer is detached in boiling hydrogen peroxide as shown in Fig.6 (g) and the photographs in Fig.6. This is because the hydrogen peroxide penetrates in the grooves of the handling wafer and the germanium is etched out.



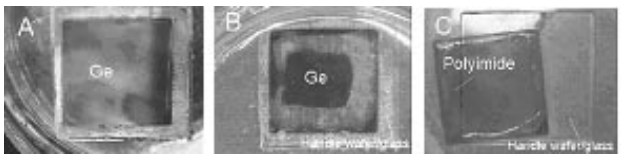


Fig.6: Wafer level packaging using glass RIE and temporally bonding [9].

Feedthroughs can be made in LTCC (Low temperature Co-fired Ceramics) as shown in Fig.7 [10]. The through holes are made by puncturing the soft green sheet and the holes are filled with a gold paste. A multilayered ceramic

wafer is fabricated by laminating the green sheets. The sheet is sintered to make a ceramic. The lateral dimension can be controlled by applying pressure or by using fixture during the sintering. This LTCC wafer can be anodically bonded to a silicon wafer because the thermal expansion of the LTCC is well matched with the silicon. The photograph of the cross section of the LTCC with feedthrough is also shown in Fig.7 [10].

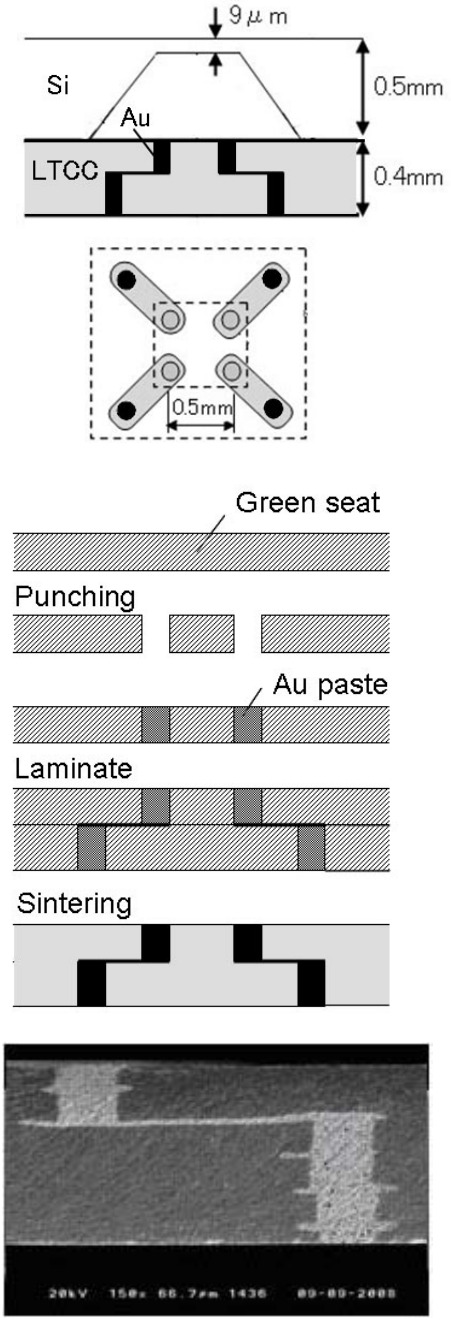


Fig.7 : Wafer level packaging using anodic bonding of LTCC and fabrication process of LTCC with electrical feedthrough [10].

ELECTRICAL INTERCONNECTION IN LID HOLES WITH METAL BONDING (Fig.2(d))

If silicon is used as the lid wafer the distortion caused by the different thermal expansions of the glass and the Si can be reduced and holes in the lid wafer can be made in the silicon by deep RIE. The fabrication process developed for a FBAR (Film Bulk Acoustic Resonator) is shown in Fig.8 [11]. Gold is electroplated using a photoresist as a mold and the silicon is etched by the deep RIE. The silicon lid wafer is bonded to the FBAR wafer by Au-Au thermo compression bonding and the etched holes are exposed by grinding the lid wafer. Finally the sealed wafer is diced into individual chips and wire bonding is made inside the exposed holes. Thermo compressive Au-Au bonding and similar metal-metal bonding as Al-Al, Cu-Cu, can be made at temperatures acceptable for MEMS. Reproducible Au-Au bonding can be performed at low temperature by surface activation and cleaning using a plasma treatment.

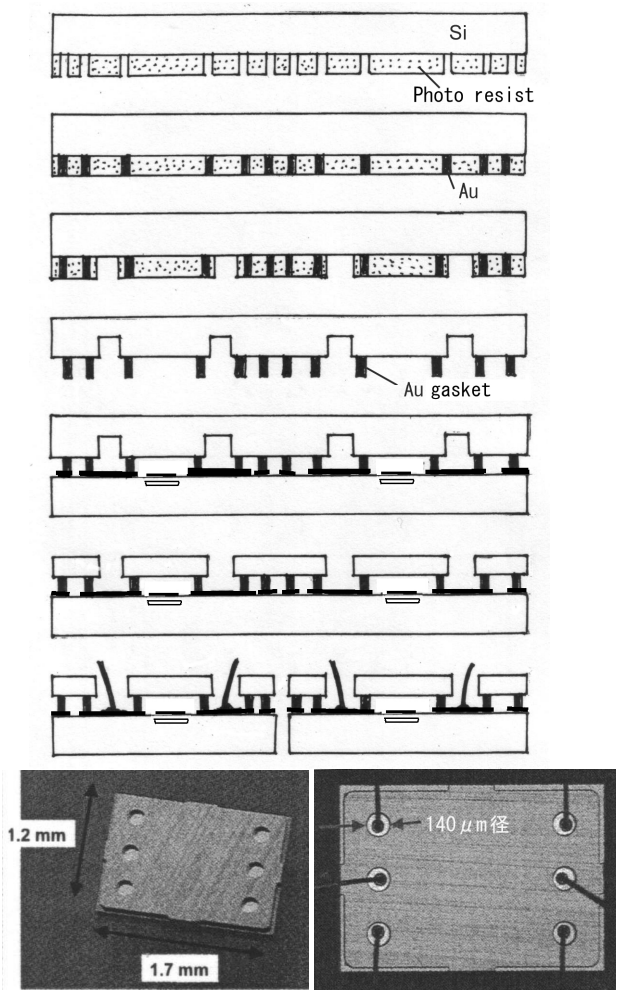


Fig.8: Wafer level packaging using wire bonding in lid holes after metal diffusion bonding [11].

ELECTRICAL INTERCONNECTION WITH EMBEDDED LATERAL FEEDTHROUGH AND INTERFACIAL BONDING (Fig.2(e))

An example of lateral feedthrough on a chip is shown in Fig.9 [12]. This has a metal layer embedded in a silicon dioxide layer. The wafer with MEMS chips are sealed with a glass lid wafer by the anodic bonding. After etching the silicon dioxide on the silicon wafer (Fig.9 (a)), the etched groove is filled with Cr-Al (Fig.9 (c)). The surface is coated with SOG (Spin On Glass) to insulate and to make a planar surface (Fig.9 (d)) and silicon is sputter deposited on it (Fig.9 (e)). This is anodically bonded to a Pyrex glass wafer (Fig.9 (f)). This lateral feedthrough however is not so practically applicable compared to the vertical feedthrough, because the lateral feedthrough has to be fabricated on the same wafer with the MEMS. There are also other lateral feedthrough using planarized surface by reflow and so on.

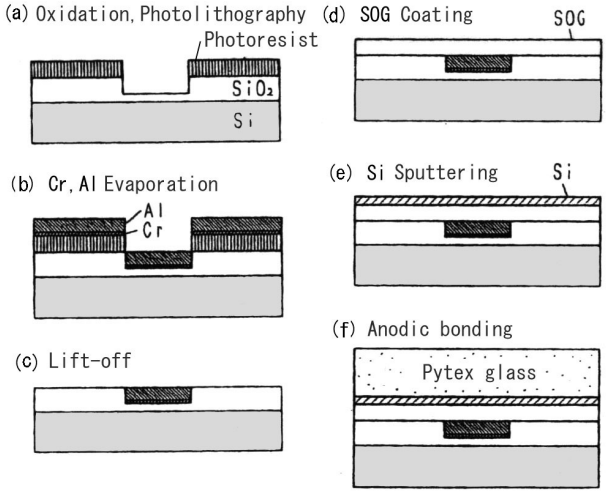


Fig.9 :Lateral feedthrough [12].

WAFER LEVEL PACKAGING USING GLASS-FRIT AND OTHER MELTING INSULATOR MATERIALS (Fig.2(f))

Chips on a wafer can be sealed with lids by melting an intermediate insulator material. Examples are shown in Fig.10 and Fig.11. Sealing is performed even if the surface is not planar and therefore a lateral feedthrough on the chip can be adopted as shown in Fig.11. This uses a glass-frit (low melting temperature glass) as the intermediate insulator material [13]. The glass-flit is coated on the lid silicon wafer by screen printing. After assembling the lid wafer to the MEMS wafer, they are bonded by melting the glass at around 400℃. The silicon is removed except that covers the MEMS structure by dicing the lid wafer and individual chips are separated by dicing the bonded wafer. The chips are ready for wire bonding and plastic molding using conventional IC packaging process.

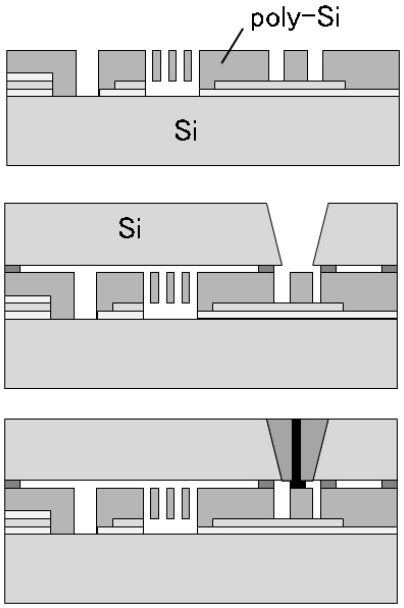


Fig.10: Wafer level packaging of accelerometer using melting insulator material

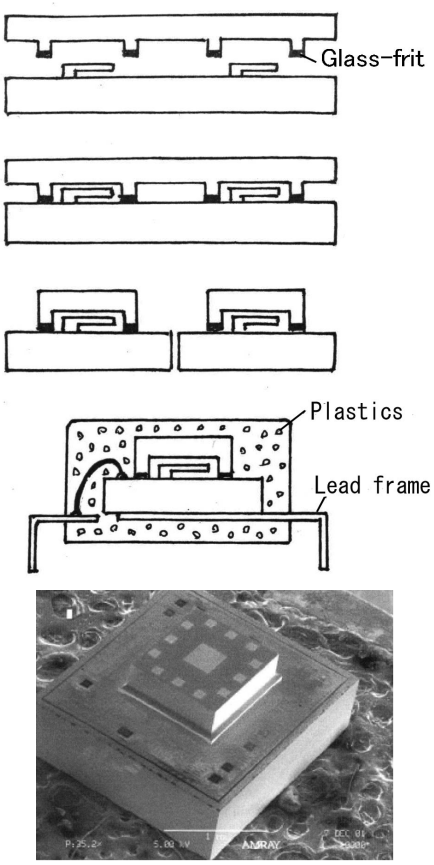


Fig.11: Wafer level packaging using glass-frit capping [13].

WAFER LEVEL PACKAGING USING SOLDER AND OTHER MELTING CONDUCTIVE MATERIALS (Fig.2(g))

Soldering and eutectic bonding can be applied to the wafer level packaging by thermally melting metals. Fig.12 is an example of the wafer level packaging using an Ge to Al eutectic bonding [14]. The MEMS substrate having Ge layer on it is bonded to the Al layer on the CMOS substrate and this technique was applied to the integrated resonating gyroscope. Not only sealing but also electrical interconnection can be made using this bonding.

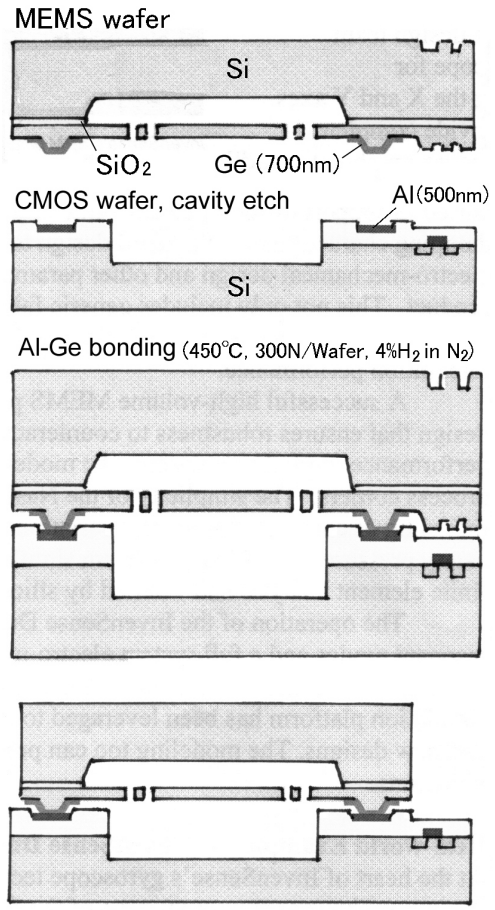


Fig.12: Fabrication process of resonating gyro using Al-Ge eutectic bonding [14].

DEPOSITION SEALING (Fig.2(i)(j))

MEMS structures protected by shells can be made by sacrificial etching. The etching requires a port for the etching solution or gas to access in the cavity. The channels or the holes used as the access port have to be sealed by depositing materials. The MEMS chips covered with the shells can be molded by plastics as conventional IC packaging.

A MEMS resonator made of single crystal silicon is sealed with a chemically vapor deposited poly-Si as shown in Fig.13 [15]. The resonator is fabricated by the deep RIE of the active layer of a SOI wafer. After deposition of silicon dioxide, the surface is polished and a thin poly-Si layer is deposited. The silicon dioxide is etched out through holes made in the thin poly-Si layer. The etching holes are sealed by depositing a thick poly-Si layer. Trenches are made by deep RIE and refilled with deposited silicon dioxide to make isolated electrical interconnections from the resonator. In the process steps of the poly-Si deposition, single crystal silicon can be grown on the exposed silicon of the wafer and is used to make integrated CMOS circuits.

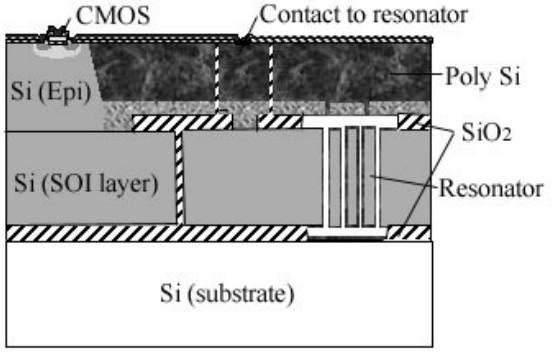


Fig.13: Single crystal silicon MEMS resonator in vacuum cavity by deposition sealing [15].

Fig.14 shows an integrated resonating gyroscope in which poly-SiGe resonator is protected with a thick poly-SiGe shell [16]. This was fabricated by etching out the sacrificial layer through vertical holes in the thick poly-SiGe shell. The holes were plugged by deposition after the sacrificial etching.

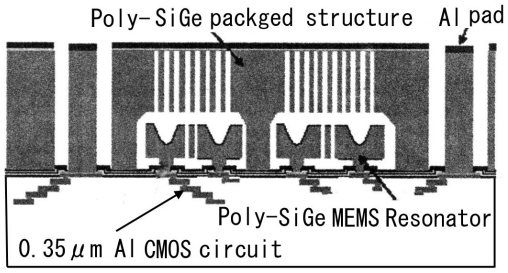


Fig.14: Integrated resonating gyroscope using thick poly-SiGe cover and deposition sealing [16].

The sacrificial layer can be etched out through porous materials, such as porous poly-Si as shown in Fig.15 [17]. The sealing can be made by depositing a metal on the shell of the porous material.

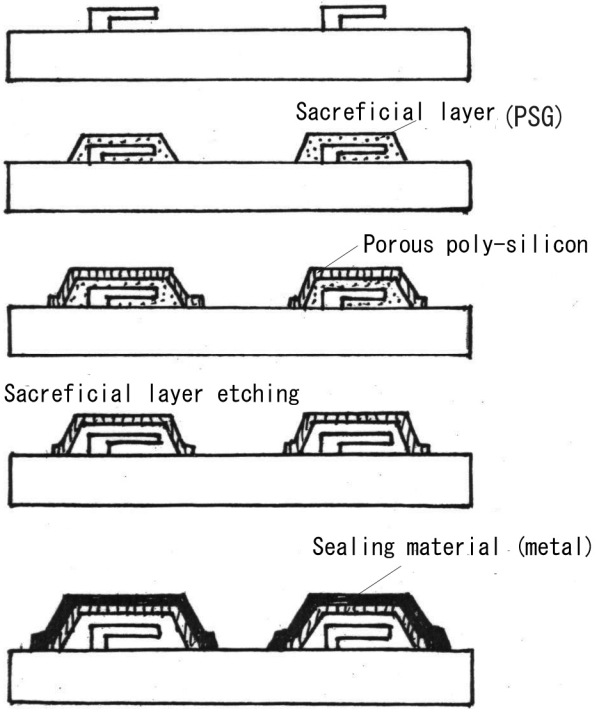


Fig.15: Wafer level packaging using porous poly-Si and deposition sealing [17]

VACUUM PACKAGING

Vacuum packaging is required for some MEMS devices, for example a capacitive diaphragm vacuum sensor, resonators in which it is needed to avoid viscous dumping for high Q factor or a thermal infrared sensor in which thermal dissipation by convection should be minimized.

It was found that gaseous oxygen is generated at the glass-Si interface during the anodic bonding process by the electrochemical decomposition of the glass. To make a vacuum cavity a non-evaporable getter is put in the cavity and the anodic bonding is carried out in vacuum [18]. The getter adsorbs gases by activating it at the temperature for the anodic bonding. Examples of vacuum packaged MEMS are shown in Fig.16. Fig.16 (a) is a capacitive vacuum sensor with a silicon diaphragm which has a vacuum cavity for the reference pressure [19]. Fig.16 (b) is an electrostatically levitated rotational gyroscope which requires vacuum cavity to avoid viscous friction while rotating at 2000 rpm [20]. Non-evaporable getter made on a wafer was developed for a batch fabrication.

Vacuum packaging by the deposition sealing is applied to the MEMS resonator shown in Fig.13. Hydrogen gas resides in the cavity during the poly-Si deposition, however the residual hydrogen gas is diffused out by keeping it in hydrogen free environment at high temperature and hence vacuum cavity is obtained inside the wafer [21].

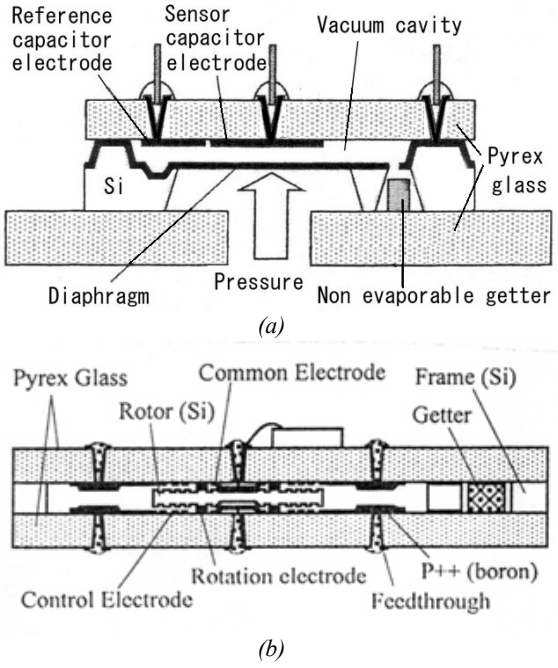


Fig.16: Examples of vacuum packaging using non evaporable getter in cavity,
(a) Silicon diaphragm capacitive vacuum sensor [19],
(b) Electrostatically levitated rotational gyroscope [20].

For an accelerometer the cavity pressure should be controlled for critical damping of the seismic mass. A silicon wafer is anodically bonded to a glass wafer in argon gas environment for the purpose. The argon gas is not absorbed by the getter and the measured cavity pressure ($P_{measured}$) is determined by the argon gas pressure ($P_{bonding}$) during bonding, the absolute temperature for bonding ($T_{bonding}$) and the absolute temperature for measurement ($T_{measured}$) based on the Boyle's law as follows [22].

$$P_{measured} / P_{bonding} = T_{measured} / T_{bonding}$$

The vacuum packaging can be characterized by different methods. In Fig.17 the cavity pressure is measured from the outside pressure when the diaphragm is flat, which means the outside and inside pressures are equal [9]. This structure can be also used to monitor a gas leakage by accumulating the leaked gas. The structure can be installed in MEMS devices having vacuum cavity.

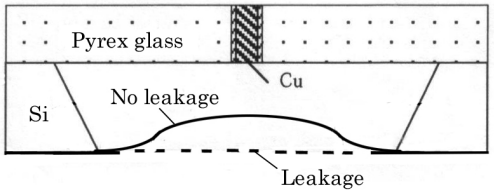


Fig.17: Monitoring of cavity pressure and gas leakage [9].

DISCUSSIONS

Wafer level packaging techniques of MEMS including the wafer level vacuum packaging are described. The packaging methods mentioned above are for hermetic sealing, on the other hand there are non-hermetic packaging methods using polymer for mechanical protecting the MEMS. Bonding plays important roles not only for the wafer level packaging but also for wafer level assembling. Plasma activated bonding leaves hydroxide group on the surface and enables interfacial bonding in atmosphere [23]. Because of the advantage of low bonding temperature at around 300℃, wafers which have different thermal expansion as silicon and GaAs can be bonded.

REFERENCES

[1] M. Esashi, "Encapsulated Micro Mechanical Sensors", *Microsystem Technologies* vol.1, pp.2-9, 1994.

[2] M. Esashi, "Wafer Level Packaging of MEMS", *J. of Micromechanics and Microeng*., vol.18, 073001(13pp), 2008.

[3] T. Kudoh, S. Shoji, M. Esashi, "An Integrated Miniature Capacitive Pressure Sensor", *Sensors and Actuators A*, no.29, pp.185-193, 1991.

[4] M. Shirai, M. Esashi, "Circuit Damage by Anodic Bonding", *Sensor Technical Report*, Institute of Electrical Engineers in Japan, Tokyo, Nov.27, 1992, pp.9-17 (in Japanese).

[5] M. Esashi, "Micromachining for Packaged Sensors", *Digest Tech. Papers Transducers'93*, Yokohama, June 7-10, 1993, pp.260-265.

[6] S. Ko, D. Sim, M. Esashi, "An Electrostatic Servo-accelerometer with mG Resolution", *Trans. IEEJ*, vol.119-E, pp.368-373, 1999.

[7] K. Nakamura, F. Takayanagi, Y. Moro, H. Sanpei, M. Onozawa, M. Esashi, "Development of RF MEMS Switch", *Advantest Technical Report*, vol.22, pp.9-16, 2004 (in Japanese).

[8] T. Abe, X. Li, M. Esashi, "Endpoint Detectable Plating through Femtosecond Laser Drilled Glass Wafers for Electrical Interconnections", *Sensors and Actuators A*, no.108, pp.234-238, 2003.

[9] X. Li, T. Abe, M. Esashi, "An Integrated Encapsulating Technology with High-density Plated-through-holes in Pyrex Glass", *ICEE 2004/APCOT MNT 2004*, Sapporo, July 4-8, 2004, pp.634-637.

[10] M. Mohri, A. Okada, H. Fukushi, S. Tanaka, M. Esashi, "Hermetic Seal using Anodically-bondable LTCC Substrate", *23th Convention of Japan Inst. of Electronic Packaging*, Yokohama, March 11, 2009, pp.51-52 (in Japanese).

[11] R. C. Ruby, A. Barfknecht, C. Han, Y. Desai, F. Geefay, G. Gan, M. Gat, T. Verhoeven, "High-Q FBAR Filters in a Wafer-level Chip-scale Package", *2002 IEEE Internl. Solid-State Circuit Conf.*, San Francisco, Feb. 6, 2002, pp.184-185.

[12] M. Esashi, N. Ura, Y. Matsumoto, "Anodic Bonding for Integrated Capacitive Sensors", *Proceedings Micro Electro Mechanical Systems'92*, Travemunde, Feb.4-7, 1992, pp.43-48.

[13] M. W. Judy, "Evolution of Integrated Inertial MEMS Technology", *Technical Digest Solid-State Sensors Actuator and Microsystems Workshop*, pp.27-32, Hilton Head, June 6-10, 2004.

[14] S. S. Nasiri, A. F. Flannery Jr., "Method of Fabrication of Al/Ge Bonding in a Wafer Packaging Environment and a Product Produced Therefrom", *Internl. patent W0 2006/101769,* 2005.

[15] A. Parridge, M. Lutz, B. Kim, M. Hopcroft, R. N. Candler, T. W. Kenny, K. Petersen, M. Esashi, "MEMS Resonators: Getting the Packaging Right", *The 9th SEMI Microsystem/MEMS Seminor*, Makuhari, pp.55-58, Dec.7, 2005.

[16] M. A. Lagos, A. Arias, J. M. Hinojosa, J. Spengler, C. Leinenbach, T. Fuchs, S. Kronmuller, "Processing of MEMS Gyroscope on Top of CMOS ICs," *2005 IEEE Internl. Solid-State Circuit Conf.*, San Francisco, pp.88-89, Feb. 7, 2005.

[17] R. He, C. J. Kim, "On-wafer Monolithic Encapsulation by Surface Micromachining with Porous Polysilicon Shell," *J. of Micro- electromechanical Systems*, vol.16, pp.462-472, 2007.

[18] H. Henmi, S. Shoji, Y. Shoji, K. Yoshimi, M. Esashi, "Vacuum Packaging for Micro-sensors by Glass-silicon Anodic Bonding," *Sensors and Actuators A*, no.43, pp.243-248, 1994.

[19] H. Miyashita, Y. Kitamura, "Micromachined Capacitive Diaphragm Gauge", *Anelva Technical Report*, vol.11, pp.37-41, 2005 (in Japanese).

[20] K. Fukatsu, T. Murakoshi, M. Esashi, "Electrostatically Levitated Micro Motor for Inertia Measurement System", *Digest Tech. Papers Transducers'99*, Sendai, pp.1558-1561, June 7-10, 1999

[21] K. Ikeda, H. Kuwayama, T. Kobayashi, T. Watanabe, T. Nishikawa, T. Yoshida, "Silicon Pressure Sensor with Resonant Strain Gages Built into Diaphragm", *7th Sensor Symposium*, Tokyo, pp.55-58, May 30-31, 1988.

[22] K. Minami, T. Moriuchi, M. Esashi,, "Cavity Pressure Control for Critical Dumping of Packaged Micro Mechanical Devices", *Digest of Technical Papers Transducers'95*, Stockholm, pp.240-243, June 25-29, 1995.

[23] S. N. Farrens, J. R. Dekker, J. K. Smith, B. E. Roberds, "Chemical Free Room Temperature Wafer to Wafer Direct Bonding", *J. Electrochem. Soc.*, vol.142, pp.3949 -3955, 1995.

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