Strength and Leak Testing of Plasma Activated Bonded Interfaces

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SUMMARY

Bond strength and hermeticity of plasma activated bonded (PAB) Si-Si interfaces are reported. Bonding of 100 mm Si (100) wafers was performed. An average bond strength of 8-10 MPa was achieved without performing any annealing steps. Bonded cavities were found to be hermetic based on the gross and fine-leak tests of MIL-STD 883 with a leak rate of 1-3 E-9 mbar l/s. For comparison, strength and leak tests were also performed with regular fusion bonded wafers annealed at 1100 °C. The influence of changing parameters in the activation process was investigated by analysing the surfaces to be bonded with optical methods.

Keywords: Wafer bonding, bond strength, hermeticity

INTRODUCTION

Plasma activated bonding (PAB) is one possible solution for bonding of wafers when high temperature annealing is not an option, for instance when substrates of dissimilar materials or substrates with metal are to be bonded. Several research groups have presented experiments with oxygen plasmas the last decade [1-8]. The mechanisms of the process are not fully understood, but increasingly more consistency can be observed in more recent experimental results [9-11]. Most authors have focused on optimising bond energy or bond strength in addition to trying to understand the basic mechanisms of the process. We present combinations of bond energy, bond strength and leakage measurements for wafers bonded under several conditions. PAB of structured to blank wafers has been reported by others earlier [4], but we here report on aligned PAB of two structured Si wafers.

EXPERIMENTAL

A stepwise approach was used to establish a strong and hermetic low temperature direct wafer bonding technique for 100 mm silicon (100) wafers. All plasma activation was performed with an O_2 plasma (200 mTorr) in a Reactive Ion Etch (RIE) batch tool, Plasma-Therm PK-12. Bonding was performed either manually in air or automatically in a bonder, SUSS SB6, in a controlled atmosphere.

For bond energy measurements, unstructured and bare wafers were plasma activated for one minute. The power was either 200, 250 or 300 W. The wafers were rinsed in de-ionized water (DIW) and spin-dried before being manually bonded in air. Strips (2 × 5 cm^2) were diced from ten bonded wafer stacks, and the bond energy for each strip was measured with the crack opening method [12]. The set-up used for the bond energy measurements has been presented by Weichel [13].

For bond strength measurements, wafers were structured in KOH with a pull test pattern, see Fig. 1. The wafers, only covered with a native oxide, were plasma activated for two minutes, rinsed in DIW and spin-dried. The power was 150, 200 or 300 W. Either one or both of the wafers were plasma activated. The structured wafers were bonded to unstructured wafers in vacuum in the SUSS SB6. Half of the bonded wafer stacks were stored at room temperature only, while the remaining stacks were given an additional annealing in air at 150 °C for 24 h. Chips diced from the PAB stacks were tested in an automated pull test set-up, MiniMat 2000. Equal chips diced from fusion bonded wafers annealed for two hours at 1100 °C were tested additionally for comparison.

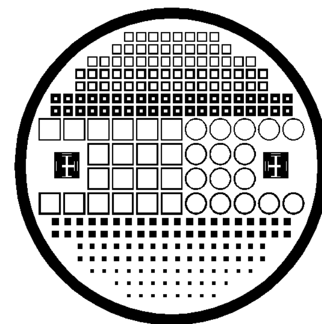

Fig. 1: Si wafers were structured in KOH with a pull test pattern consisting of frames and mesa structures.

In order to perform leakage tests, wafers structured in KOH were plasma activated for two minutes at 200 W, rinsed in DIW and spin-dried. Grooves and deep cavities with thin membranes were etched in the top wafers, and holes were etched in the bottom wafers, see Fig. 2. The narrowest distance between the cavity and the V-groove was typically 0, 20, 30, 40 or 70 µm wide. The stacks were aligned in a bond aligner, SUSS BA6, before being bonded. The cavities were closed in vacuum in the SUSS SB6, and the membranes of the cavities deflected inwards after bonding when a hermetic seal was obtained. The number of membranes deflecting inwards indicated the yield of the process, ranging from 20 - 90 % for six wafer couples. For two of these wafer stacks, the bottom wafers were covered with a thermal silicon oxide of 825 Å as recommended in Ref. [4]. Two equal wafer stacks were fusion bonded in vacuum and annealed for two hours at 1100 ^{o}C for comparison. A yield of 80 - 90 % was achieved for these wafers. For leak testing, deflection of the membranes was measured as a function of time after bonding with an optical profiler, Wyko NT2000. Additionally, two chips diced from each of the two PAB wafers and the two fusion bonded wafers were tested after the conditions of the helium leak test of MIL-STD 883 [14].

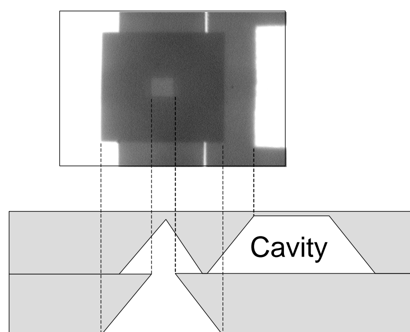

***Fig. 2**: Chip for test of hermeticity. The narrow, bonded interface is 0, 20, 30, 40 or 70 µm wide. Inset: Picture taken with an IR camera on a microscope.*

Based on the large spread in yield numbers for the PAB wafers, it was decided to study the homogeneity of wafer surfaces after exposure to a selection of plasma activation processes. The quality of the native oxide layers before plasma activation, and the flow conditions in the RIE batch tool, as mentioned in Ref. [11], were expected to be relevant factors. Oxide layer thicknesses were measured before and after plasma activation with a Philips SD 2000 ellipsometer. The refractive index of all oxide layers was fixed at the value for a thermally grown oxide. The possibility of having a change in oxide density or other qualities influencing the optical properties of the oxide was not taken into consideration. The oxide thickness should thus be considered as a value representing the process rather than the true value of the thin oxide layer [15].

RESULTS AND DISCUSSION

The bond energies of the unstructured wafers manually bonded in air are presented in Fig. 3. The energy was measured as a function of time after bonding. Bond energies up to 1.7 Jm^{-2} were achieved for wafers activated for 60 seconds at 200 W, which indicated a possible optimum for those process conditions. It was not evident from the measurements if a saturated value for the bond energy was reached, but for the stronger bonds, the thick razor blade could not be inserted without fracturing the wafers. We used razor blades of thickness 130 µm. Annealing at an increased temperature could probably have reduced the long time needed to increase the strength of the bond. Based on other authors' experiences, annealing would however result in numerous voids at the interfaces, see e.g. Ref. [11]. We did not observe any growth of voids at the interface during storage at room temperature with an IR inspection camera.

The results of the pull testing of structured wafers bonded in vacuum are presented in Table 1 and in Fig. 4. The average strengths are presented together with relevant process parameters. Several observations were made. An average maximum bond strength of 9 MPa was achieved for wafers activated for 120 seconds at 200 W, which seemed to be the best of the tested process conditions. As mentioned in Ref. [10], a process optimum may exist where the oxide layer is satisfactory cleaned and damaged simultaneously. The oxide has been suggested to be porous after the plasma activation [9], and we propose that the layer additionally has become softer and easier to deform. After annealing at 150 ^{o}C, the bond was expected to be stronger. A significant increase in strength was however not observed for our test samples.

A noticeably reduced strength was achieved when only one of the wafers was plasma activated. A possible explanation for the phenomenon could be that the number of silanol groups (Si-OH) [4] had to be increased at both wafers in order to take fully advantage of the plasma activation.

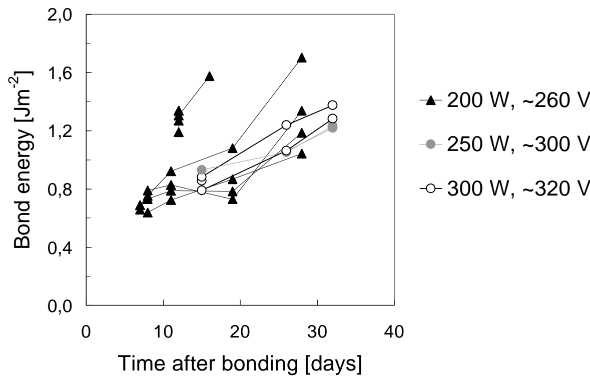

Fig. 3: *Bond energy of strips diced from 10 unstructured wafers bonded in air after plasma activation (60 s and a varying power).*

In addition to the pull test structures (mainly the largest mesa structures were tested), some of the chips prepared for the test of hermeticity were torn apart. A small force was subtracted from the tensile test results to compensate for the vacuum within the cavities before pulling. The strength of the leak test structures was equal to the strength of the pull test structures plasma activated with equal parameters. The result showed that two structured wafers could be bonded with the same quality as one structured wafer and one unstructured wafer.

We tested the hermeticity of the strongest bonding process (120 seconds at 200 W) in two ways. The deflection of the membranes of the test structures was measured as a function of time after bonding to detect leakage of gas into the cavities or desorption of gas from the cavity walls. The detection limit for these leak tests was found to be 20 mbar from calibration curves of reference structures. Even 100 days after bonding, no pressure changes in the bonded cavities were observed. Additionally, chips were tested after the conditions of MIL-STD 883. The results of this helium leak test are presented in Table 2.

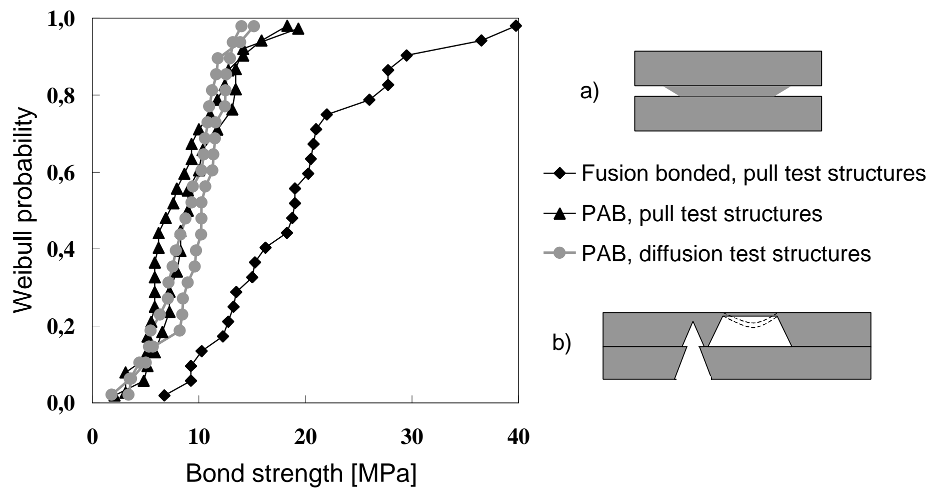

Fig. 4*: Weibull plots [13] of pull test results of four PAB wafers (120 s, 200 W) and one fusion bonded wafer. Schematic drawings of pull test (a) and leak test structures (b) are shown.*

Table 1: *Average bond strength of PAB (120 s and varying power) and fusion bonded wafers. All values are based on 15-25 pull test measurements from one or two wafer stacks bonded at equal conditions.*

RF Power (W)	Self-Bias (V)	Activated wafers	$\langle\sigma\rangle$ RT (MPa)	$\langle\sigma\rangle$ annealed at 150 °C (MPa)
150	229-229	top and bottom	6.7 ± 1.1	6.0 ± 2.6
200	262-262	top	2.9 ± 0.8	4.6 ± 1.4
200	256-274	top and bottom	9.0 ± 2.0	8.5 ± 3.9
300	330-360	top and bottom	5.4 ± 3.6	7.1 ± 4.1
Fusion bonded wafers annealed at 1100 °C				19.3 ± 8.2

Table 2: Results of gross and fine leak tests of chips from PAB and fusion bonded wafers after MIL-STD 883.

Bonding process	Gross leak	Fine leak (mbar l/s) 10^{-9}
PAB	OK	1.0-3.0
Fusion (1100 ^{o}C)	OK	2.4-5.0

Post processing steps were performed on chips diced from the PAB wafers with leak test structures to inspect the usefulness of the bonding process. The membranes still deflected inwards after 24 h in DIW, 24 h in 2.5 % HF, 24 h in acetone, RCA cleaning and 60 s in a resist developer. The pressure inside the cavities increased 20 mbar after annealing for 24 hours at 200, 400 or 600 ^{o}C, independent of temperature. This indicated desorption of gas from the walls rather than in-diffusion. No additional voids were visible at the bonded interface of the annealed chips.

The plasma activated oxide thickness was found to increase with process time and power as shown in Fig. 5 a) and b). Standard deviation in oxide thickness after plasma activation was 0.08 nm for 5 wafers "from the box" and 0.01 nm for 5 pre-treated wafers. The most homogeneous oxide could probably result in higher yield numbers than those achieved in this work.

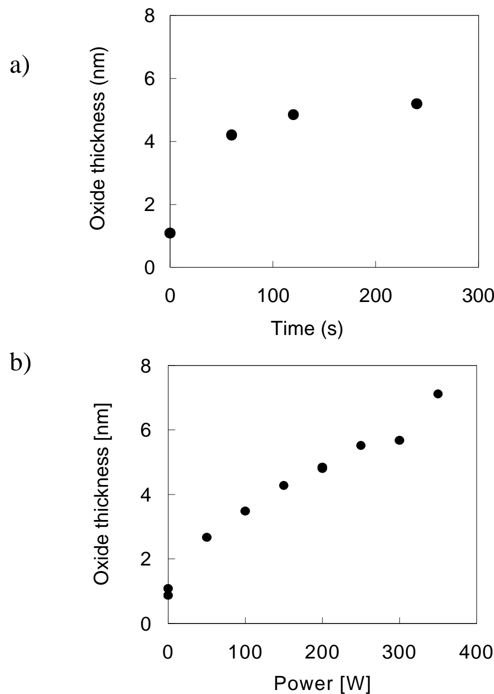

***Fig. 5**: Effect of process time (200 W) (a) and power (120 s) (b) on oxide thickness after plasma activation.*

Pre-treated wafers were RCA cleaned with a 5 % HF dip between the ammonia and the hydrochloric acid baths.

CONCLUSIONS

A room temperature direct wafer bonding process for two structured and aligned silicon wafers was established. The strength of the bond was 8-10 MPa for the best process conditions. The highest bond strength was achieved when both wafers were plasma activated. The seal was found to be hermetic according to the requirements of MIL-STD 883. A homogeneous oxide after plasma activation was found to be achievable even in a batch RIE tool when a controlled native oxide was present on the wafers before activation

ACKNOWLEDGMENTS

The work was funded by The Norwegian Research Council. D. T. Wang is acknowledged for useful discussions on scientific aspects of this work.

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