

Development of a High Density, Planar, Modular Microfluidic Interconnect System

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SUMMARY

The development of a high density, planar, modular microfluidic interconnect system is described that is based upon the application of conventional gasket sealing principles to miniaturized bulk micromachined geometries in silicon. Microfluidic ports between two flat surfaces are sealed by an intervening micromolded elastomeric gasket that mates to micromachined bosses around each port. The gasket seal construction allows for precise control of the sealing pressure and for insuring its uniform distribution around each port. The interconnect system does not utilize any external fitting hardware and can achieve high density microfluidic interconnects with port-to-port pitches as small as 2 mm.

Keywords: *microfluidics, interconnects, packaging.*

INTRODUCTION

An important, but often neglected, principle of fluidic sealing is that the maximum possible leak test pressure is never more than the minimum pressure at any point around the sealing surfaces. The construction of high leak test pressure seals thus involves the design of a system which produces high sealing pressure uniformly around each port.

The simplest implementation of a high density fluidic interconnect involves the sandwiching of a uniform thickness elastomer gasket between the flat surfaces of two mating parts, as shown in Fig. 1a. The limitation of this system is that the two parts must be uniformly compressed to produce perfect parallelism and the surfaces must be extremely smooth so that local surface irregularities do not create regions of low sealing pressure. In practice, the required pressure on the two parts can be as much as 10× the required leak test pressure to produce proper sealing.

An improved system is shown in Fig. 1b, in which a boss is added around each port to localize and increase

the sealing pressure. This reduces the needed compression force on the two parts, but for the small dimensions of a microfluidic port, the elastomer gasket can easily be squeezed out from under the boss, sometimes occluding the port.

A more advanced sealing system is shown in Fig. 1c, where the micromachined boss around the port contains a gasket capture channel which mates to a ridge that is molded into the elastomer gasket. When the two parts are compressed, the elastomer is tightly captured in the channel region around each port, and the containment of the gasket is such as to keep it from being squeezed out from under the boss.

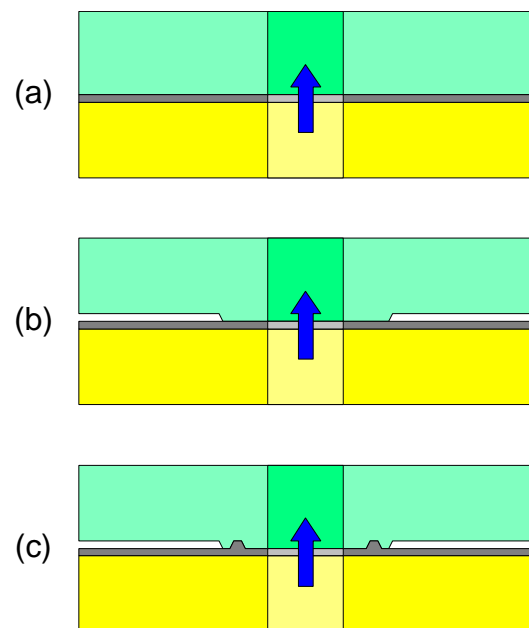


Figure 1: *Development of elastomer gasket technology.*

(a) *flat gasket and mating surfaces.*

(b) *flat gasket with bossed mating surfaces.*

(c) *captured gasket with bossed mating surfaces.*

DESIGN AND FABRICATION

The present system is designed for mating the bottom of a micromachined silicon die to either the top of another silicon die, or to the top of an acrylic microfluidic motherboard. Such a motherboard provides the fluidic analog to a printed circuit board and allows components from different fabrication technologies to be easily integrated into a small overall system size. By basing the interconnect design upon flat sealing surfaces, no external fitting hardware such as nuts or ferrules are required, and high density interconnects can be constructed which are all simultaneously sealed upon alignment and compression of the die onto the mating flat surface.

Micromachined Silicon Die

The silicon die are anisotropically etched using EDP to create the bosses and the gasket capture channel using a single back-side infrared-aligned mask. The surface of the mating part is flat so that no additional micromachining is required for it. The geometry of the etch mask pattern is shown in Fig. 2. Etch compensation serifs are added to each external corner, as shown, to keep the outside features square. The etch compensation distance (EC) is made equal to the etched height of the boss (BH). For the present designs, the boss outer face (BOF), ridge width (RW), and boss inner face (BIF) were constructed using $BOF = RW = BIF$ values of 100, 200, 300, and 400 μm . The port diameter (PD) within the inner boss face can be nearly any dimension, from 10 to 1000 μm for example, and either round or square.

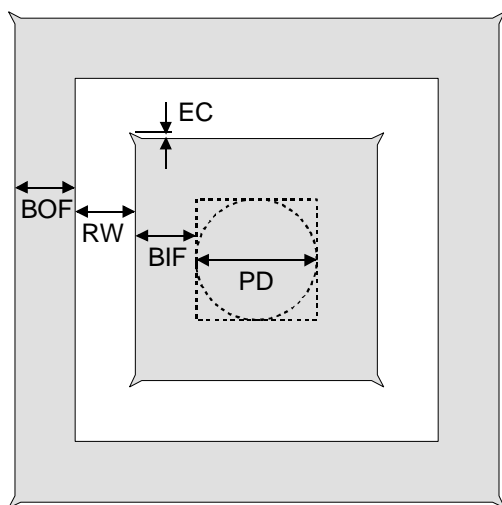
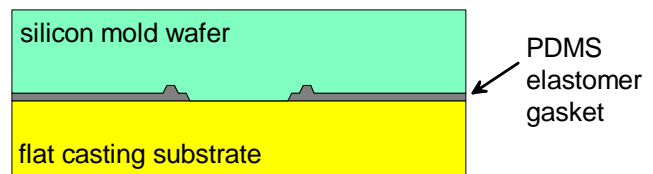


Figure 2. Mask pattern for backside boss etch.

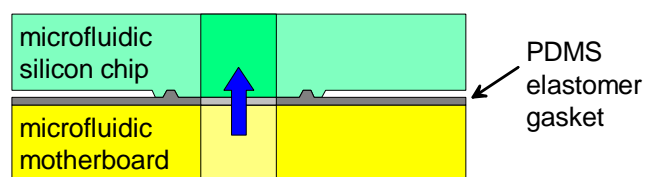
Elastomer Gasket

The elastomer gasket is cast between an anisotropically etched silicon mold wafer and a flat casting substrate, as shown in Fig. 3a, using a soft lithography technique [1]. The silicon micromold wafer is created by two successive photolithography steps, oxide etches, and anisotropic EDP etches to produce the two different etch depths for the gasket ridge and hole. Since the masks for the silicon microfluidic die and gasket micromold are created as a set, the gasket mates to the silicon die with a tolerance of only a few microns.

Prior to casting, the silicon mold is silanized by exposure to $\text{CF}_3(\text{CF}_2)_6(\text{CH}_2)_2\text{SiCl}_3$ vapor for 30 minutes to create a hydrophilic surface. The PDMS prepolymer is then poured out over the mold which is then capped with a flat, but semiflexible, teflon wafer. The PDMS is then cured at 65°C for 4 hours in a vacuum oven. After curing, the teflon wafer can be bent away and the gasket peeled from the mold wafer. Silanization of the mold wafer is necessary to allow the gasket to be released. Thinner PDMS films were also achieved by spin casting. A volume of 1.5 mL of the prepolymer, spun at 5000 rpm for 5 minutes gave a final cured gasket thickness of $\approx 100 \mu\text{m}$.



(a) gasket micromolding



(b) gasket assembly

Figure 3. Schematic of PDMS elastomer gasket micromolding and assembly into interconnect seal.

Upon assembly, the gasket is compressed only around the area of the interconnect port, as shown in Fig. 3b. With proper design of the mask features, nearly zero dead volume interconnections can be created.

Fluidic Vias

This interconnect system allows a wide choice in the construction of the microfluidic ports which are put into each boss. Simple through-wafer vias with vertical sidewalls can be drilled with a high speed C6 carbide bit, laser drilled, or etched using a DRIE process. The interconnect ports can also be integrated into the process flow of other microfluidic devices. Figure 4 shows a microfluidic via that was constructed using EDP anisotropic etching and also incorporates a boron-doped etch stop membrane into which a 10 μm microbead sieve has been etched [2,3]. This early prototype, which did not use etch compensation serifs, has highly rounded exterior corners inside the gasket capture channel. Even though the Si mold wafer has the same corner rounding and the elastomer gasket still fills the capture channel, the nonuniform width of the channel reduces the ultimate leak test pressure. Vias of this type (1 mm square EDP etch pit into a 400 μm thick wafer) can be spaced as close as 2 mm center to center. Smaller, drilled vias can be spaced closer still.

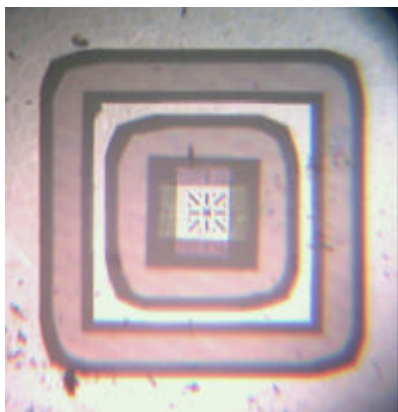


Figure 4. View of bossed silicon die, gasket capture channel, and microbead sieve membrane within port.

Mounting and Assembly

The micromolded gasket is applied to the bottom of the silicon die as shown in Fig. 5. The 54.74° angle of the anisotropic etch creates a capture channel around the ridge in the PDMS gasket that produces a much higher compression force because the gasket is kept from being squeezed out from under the boss. Gasket materials with low compressibility but good plastic flow thus create the highest sealing pressures.

When only a small number of interconnects are employed, the die can rock on the port boss. This

rocking is eliminated by the addition of leveling bosses which maintain parallelism between the die and the substrate, and which are shown in the four corners of Fig. 5.

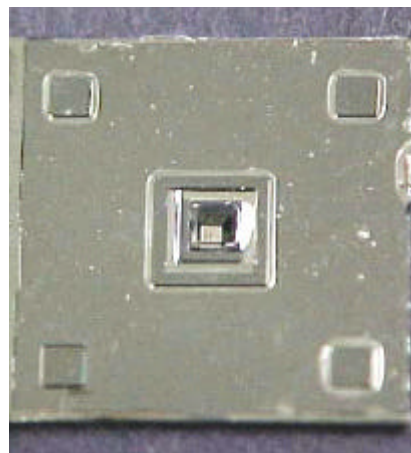


Figure 5. PDMS gasket applied to silicon die. Leveling bosses are seen in the four corners.

The silicon die and PDMS gasket are compressed against their mating part by means of an acrylic compression housing. The internal cavity of the housing is milled to close dimensions of the silicon die, so that the housing also aligns the silicon die to the corresponding part. This scheme allows the system to be easily and repeatably disassembled and reassembled for cleaning or modification purposes.

PERFORMANCE AND OPTIMIZATION

Leak pressure testing was accomplished using the fixture of Fig. 6, which uses a specially ported acrylic compression housing and microfluidic test-block. This fixture also allows two adjacent interconnects to be tested for cross-over leakage.

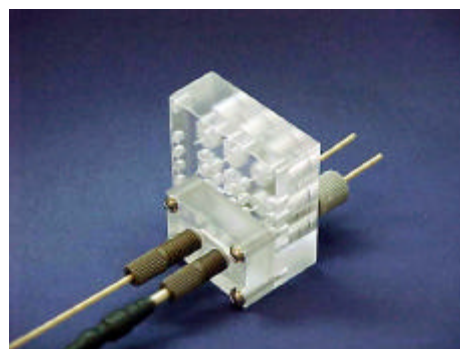


Figure 6. Assembly for pressure testing.

The degree of gasket capture, and hence sealing pressure, is increased by making the film thickness of the PDMS gasket small in comparison to the height of the PDMS ridge. Ideally, a set of closed PDMS sealing ridges are created which are merely held in position by a thin PDMS film. The film itself should provide no actual sealing. Initial prototypes with 50 μm films and 50 μm ridges produced average leak test pressures of 65 psi. Changing the PDMS film thickness to 25 μm with a ridge height of 75 μm produced average leak test pressures of 450 psi; however, the 25 μm thick film proved too fragile for casual handling. Increasing the film thickness back to 50 μm and increasing the ridge height to 75 μm , while keeping the capture groove depth at 50 μm , provided the best overall performance. Average leak test pressures of over 500 psi were then repeatably obtained.

APPLICATIONS

These microfluidic interconnects have been successfully used in the construction of a hand-held immunoassay system which incorporates six piezoelectric pump modules and two polarographic microbead detection cells, each of which is integrated onto an acrylic microfluidic motherboard, shown in Fig. 7 [2,3]. Each silicon die is sealed by the PDMS gasket technology and is compressed against the motherboard by an acrylic compression housing which is also shown in Fig. 7. These modules can be disassembled and reassembled many times using only a small screwdriver, without any loss of leak test pressure. When a seal does begin to deteriorate, simply changing the elastomer gasket restores the original sealing performance.



Figure 7. Microfluidic motherboard with attached modules.

This interconnect system is applicable to ports of arbitrary shape and size. Several useful variations in the mask design can be used to create unique lateral connections and chambers. For example, matching a hole in the PDMS gasket to a slot within a boss, which is encircled by a PDMS sealing ridge, creates a lateral connection between two vertical vias. This structure can be used for fluidic cross-overs in more complex systems where multiple wafers are stacked together using the same interconnect technology on each. These multiple wafers can then be aligned and compressed using a single acrylic housing.

CONCLUSIONS

A high density, planar, modular microfluidic interconnect system is described which is readily integrated with other microfabrication process flows. Leak test pressures of typically 500 psi can be achieved with via center to center spacings as small as 2 mm. The interconnects can also be readily disassembled and reassembled many times without degradation. This modular microfluidic approach provides a very flexible, LEGO[®]-like interconnect system for integrating multiple wafers or different device technologies.

ACKNOWLEDGMENTS

The author wishes to thank E. Aw, M. Mar, M. Takeno, and G. Holman for assistance with the microfabrication and testing.

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