Fabrication and Testing of Single Crystalline 3C-SiC Piezoresistive Pressure Sensors

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SUMMARY

This paper presents the development of a single crystalline 3C-SiC piezoresistive pressure sensor using wafer bonding and bulk micromachining techniques. The wafer used to fabricate this pressure sensor consisted of a 3C-SiC/SiO_2/Si structure that was obtained by wafer bonding and etchback. The pressure sensors were tested at temperatures up to 385°C and exhibited a sensitivity of 101.5 μV/V*psi at room temperature and 53.4 μV/V*psi at 385°C. The estimated gauge factor of the 3C-SiC piezoresistors is about –18.

Keywords: 3C-SiC, pressure sensor, wafer bonding, high-temperature testing

INTRODUCTION

Due to its outstanding electrical and mechanical properties, silicon carbide (SiC) is considered a leading semiconducting material for micromachined high temperature sensors and actuators [1]. 3C-SiC is a particularly attractive SiC polytype since it can be epitaxially grown on Si substrates, thus allowing for the use of Si bulk micromachining to fabricate pressure sensor membranes.

Unfortunately, the heterojunction formed at the SiC/Si interface suffers from unacceptably high leakage currents at elevated temperatures, thus rendering the material unsatisfactory for high temperature applications. One approach to reduce heterojunction leakage is to grow 3C-SiC films on thin SOI wafers which can be bulk micromachined into pressure sensor structures [2]. Although the SiC piezoresistors are isolated from the bulk Si substrate via the buried oxide layer, the thin Si surface layer of the SOI substrate is often not completely converted to 3C-SiC thus creating a path for heterjunction leakage, and potentially a hybrid SiC/Si piezoresistor. An ideal substrate for 3C-SiC piezoresistors would utilize a 3C-SiC/SiO_2/Si substrate absent of any 3C-SiC/Si interfaces. With this substrate, a pressure sensor consisting of 3C-SiC thin film piezoresistors, a bulk micromachined single crystalline Si membrane, and a silicon dioxide insulating layer sandwiched between the two could readily be fabricated.

This paper presents the development and high temperature testing of a single crystalline 3C-SiC piezoresistive pressure sensor. The sensor was fabricated from a novel 3C-SiC/SiO_2/Si substrate that was created using wafer bonding and silicon bulk micromachining.

FABRICATION PROCESS

The 3C-SiC piezoresistive pressure sensor is shown schematically in Fig. 1 and an overview of the substrate fabrication process is shown in Fig. 2.

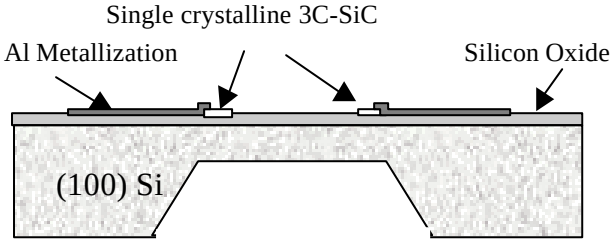

Fig. 1. Cross sectional schematic of the pressure sensor.

The substrate fabrication process begins with heteroepitaxial growth of a 0.5 μm-thick single-crystalline 3C-SiC film by atmospheric pressure CVD (APCVD) on a 100 mm-dia. Si handle wafer (~550 μm-thick), using SiH_4 and C_3H_8 as the

source gases and hydrogen as the carrier gas. A two-step process described elsewhere [4] was used to grow the 3C-SiC films. The as-grown 3C-SiC films are unintentional n-type doped to a level suitable for piezoresistors, therefore intentional doping was not performed. Following 3C-SiC growth, a polysilicon film was deposited on the 3C-SiC surface and then thermally oxidized to form a 1 µm-thick SiO_2 film on the top of 3C-SiC surface. In addition, a 0.5 µm-thick thermal SiO_2 film was grown on a Si carrier wafer. The SiO_2 surfaces on both the handle and carrier wafers were then polished by CMP to a mirror finish. In order to overcome the characteristic warpage of Si wafers caused by the thermal mismatch between 3C-SiC and Si, the Si handle wafer was thinned to 250 µm using backside lapping and polishing followed by KOH etching to obtain a compliant substrate for wafer bonding. After chemically cleaning the SiO_2 surfaces, the handle wafer was bonded to the device wafer, which was held during the process by a vacuum chuck.

The piezoresistive effect in SiC is highly anisotropic, and exhibits a dependence on the dopant type, dopant concentration, and crystal orientation. The dependence on crystal orientation requires that the wafers be bonded with proper alignment to realize piezoresistors with maximum stress sensitivity. Like n-type Si, n-type SiC has its largest piezoresistive coefficient along the <100> direction [4]. In order to obtain <100> oriented 3C-SiC piezoresistors that are positioned perpendicular or parallel to the wet-etched <110> oriented Si membrane edges, it was necessary to bond the handle and device wafers with their primary flats oriented at a 45° angle with respect to each other, as shown in Fig. 3. The bonded pair was annealed at 1100°C for 1hr to form a strong SiO_2-to-SiO_2 fusion bond. The handle wafer was then thinned by mechanical lapping, then etched away in KOH leaving the exposed 3C-SiC film on the Si device wafer, but electrically isolated from the membrane by a 1.5 µm-thick SiO_2 layer. The 3C-SiC/SiO_2/Si substrate was then used for the fabrication of the pressure sensor. The bonding and etchback yield was between 75 and 85 %, as shown optically in Fig. 4.

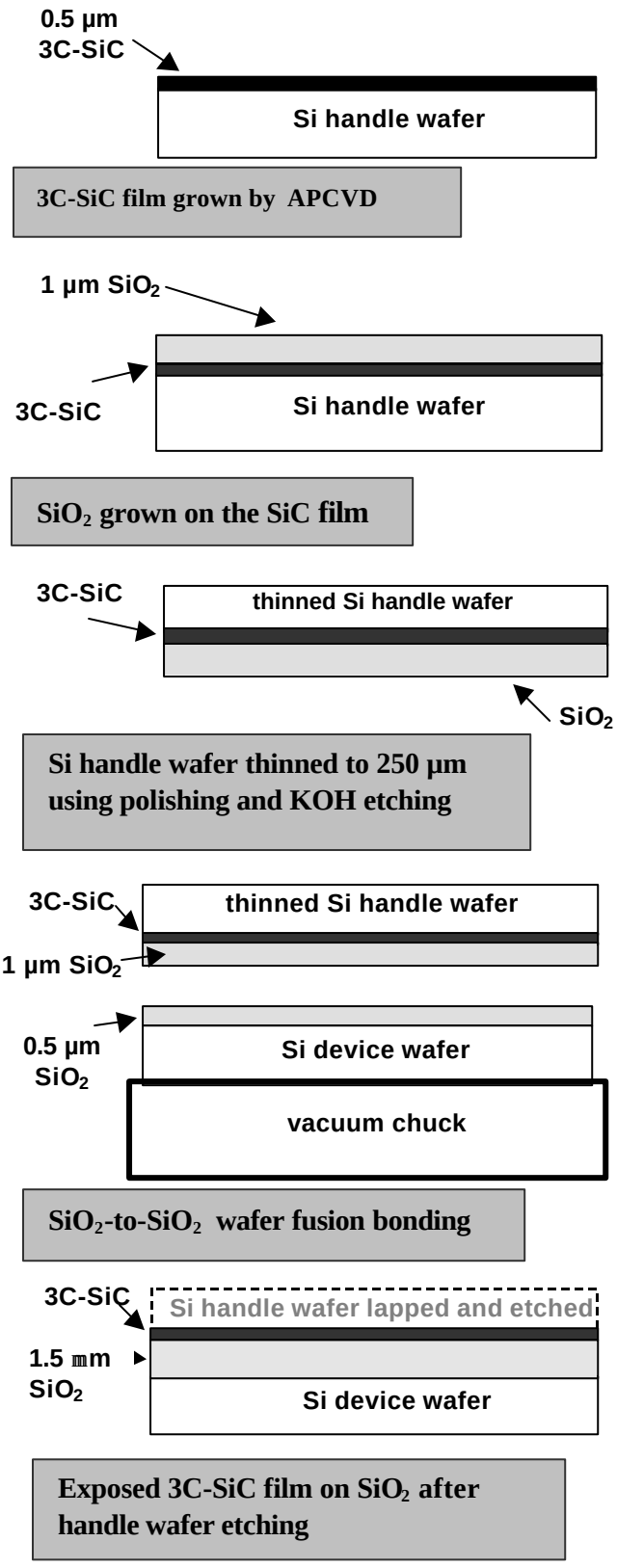

Fig. 2. Cross-sectional schematic of the wafer bonding process.

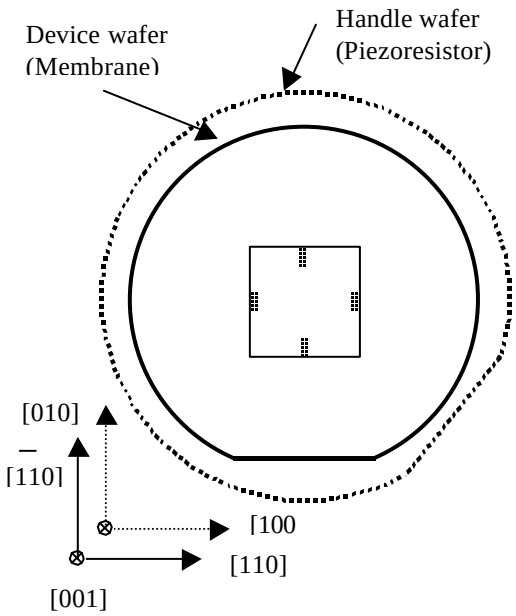

Fig. 3. Schematic showing the orientation of the bonded wafers.

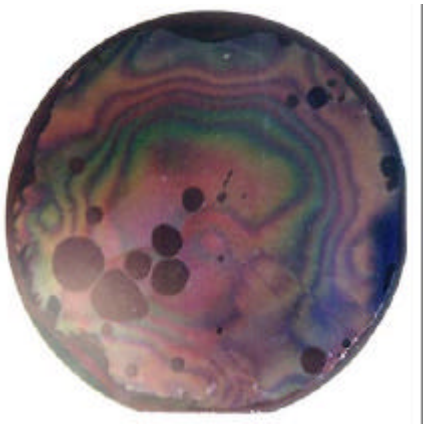

Fig. 4. Photograph of a 3C-SiC/SiO_2/Si substrate.

A 5-mask process was used for the fabrication of the pressure sensors. After wafer bonding and etchback, the 3C-SiC film was patterned into piezoresistors using reactive ion etching (RIE). A 0.5-μm thick Al film used as the etch mask was deposited and patterned by a standard photolithographic step and a wet chemical etch. A mixture of CHF_3/O_2/He gases was used in the SiC RIE step. The etching process was complete when the buried oxide layer was exposed. After realizing the piezoresistors, a 2000Å-thick LTO film was deposited on the substrate for passivation. Contact windows were then opened in the LTO to expose the piezoresistors. A 0.5 μm-thick Al layer was then sputtered, patterned and etched to form the interconnects.

After patterning the piezoresistors, an oxide on the backside of the Si substrate (not shown in Fig. 2) was patterned to open windows for anisotropic KOH etching. A timed etch process was used to form Si membranes of the correct size and thickness. For the majority of the pressure sensors fabricated in this study, a 15 μm-thick silicon layer was used as a membrane. The pressure sensor design utilized four piezoresistors placed near the membrane edge, two positioned parallel to the edges and two perpendicular to the edges. The piezoresistors were connected in a Wheatstone-bridge configuration. An optical micrograph is shown in Fig. 5.

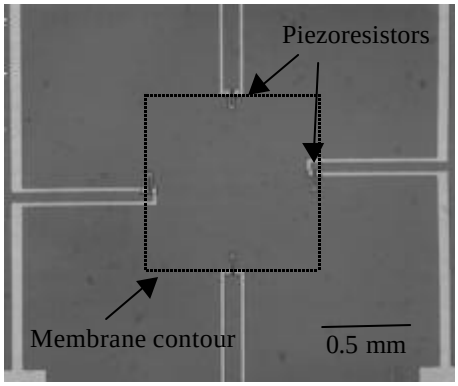

Fig. 5. Optical micrograph of a 3C-SiC sensor.

PRESSURE SENSOR TESTING

The performance of the sensors was characterized at room and elevated temperatures. High temperature testing was performed in a specially constructed heating chamber. The sensor chips were mounted with high-temperature cement onto a stainless steel chuck that could be pressurized and de-pressurized through a 1 mm-diameter hole located at its center. The chuck was positioned on a boron nitride heater and was connected to a compressed air supply via a pressure manifold. The flow of air through the manifold was controlled by a needle valve, and air pressure applied to the chuck was measured by a sensor positioned on the manifold. A DC voltage of 10V was used as the input voltage to the test specimen.

To prevent oxidation of the Al contacts at high temperature, argon was used as the ambient. High-temperature manipulators with tungsten carbide probes were used to connect the sensor to the constant input voltage source and an output voltage meter.

A graph of output voltage versus applied pressure from a sensor with a 750x750 μm^2 diaphragm is shown in Fig. 6. The maximum output is 68 mV and the sensitivity is 101.5 μV/V*psi at room temperature. The end-point linearity is 4.1% of FSO. The gauge factor of the piezoresistors is about –18. The sensitivity of the sensor decreases with increasing temperature, changing from 101.5 μV/V*psi at room temperature to 53.4 μV/V*psi at 385°C. A resistance decrease with increasing temperature was also found for the 3C-SiC piezoresistors, as shown in Fig. 7. The TCR is about 53%/°C at room temperature and decreases to -0.06%/°C at 450°C.

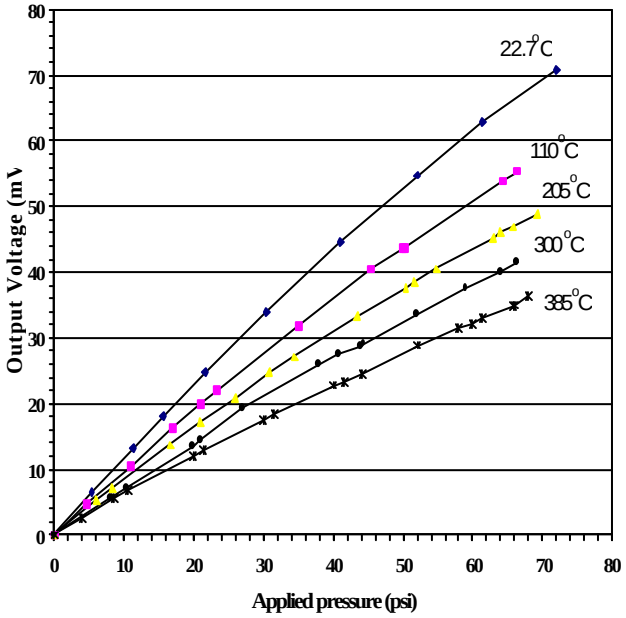

Fig. 6. Voltage output versus pressure between room temperature and 385 C.

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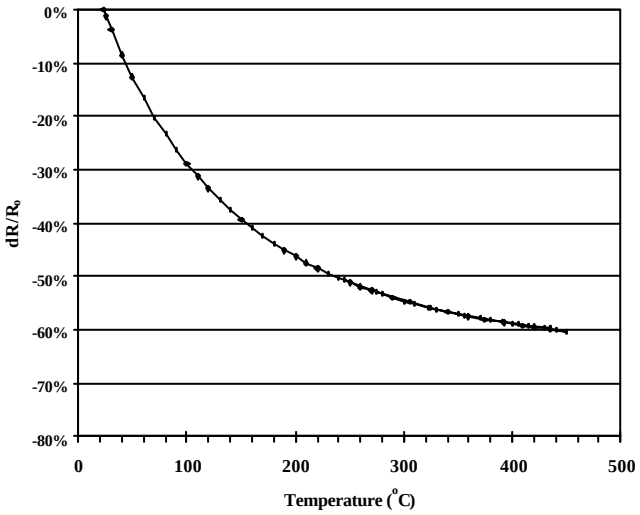

Fig. 7. Percentage change of resistance versus temperature for 3C-SiC piezoresistors.

CONCLUSION

3C-SiC pressure sensors using electrically isolated piezoresistors were fabricated using wafer bonding and bulk micromachining techniques. The wafer bonding process was used to produce 3C-SiC piezoresistors that were electrically isolated and did not have a 3C-SiC/Si interface. The pressure sensors were successfully tested at temperatures up to 385°C.

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