

EXPLOITING PARALLELISM IN RESONATORS FOR LARGE VOLTAGE GAIN IN LOW POWER WAKE UP RADIO FRONT ENDS

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ABSTRACT

This paper reports a lithium niobate (LiNbO₃) resonator array that, when used as a passive voltage amplifier, can produce a passive resonant voltage gain among the highest reported thus far for low-power wake-up radio front-ends. The high voltage gain is obtained by exploiting parallelism in the form of 56 arrayed identical shear horizontal mode resonators. The array of LiNbO₃ devices is designed to simultaneously enable a large static capacitance of 1.05 pF, a spurious mode free response, and a large figure of merit (FoM= $k_r^2 \cdot Q$) of 120, all of which are subsequently demonstrated for the first time for a large resonator array. As a result, voltage gains over 20 or 26 dB have been achieved for highly reactive loadings of typical CMOS wakeup radio front-end input. In addition to the high voltage gain, the array also features a high Q of 915, which produces to 3 dB FBW of 0.1% for filtering noise and interference in the RF ambience.

INTRODUCTION

Internet of Things (IoTs) has inspired recent studies on ultra-low-power wake-up radios for applications where wireless functions are event-driven and infrequently required [1]. The operation of a wake-up radio typically necessitates a high-sensitivity (<-60 dBm) receiver that remains alert to a wakeup signal while consuming very low power (<10 nW) [2]. Two main hurdles remain for achieving such high performance. First, it is challenging to trigger upon a faint RF signal far lower than the threshold voltage of the state-of-the-art CMOS or alternative microelectromechanical systems (MEMS) devices [3]. Second, it is essential to incorporate high frequency-selectivity [4] or great signal correlation [5], [6] in the signal processing stages to minimize the false alarms induced by the interference or background noise in the RF spectrum. One promising solution, as seen in Fig. 1, is to utilize an impedance transformer to up-transform the impedance, and passively amplify voltage swing across the follow-on CMOS rectifier. In other words, the transformer enables the rectifier to receive RF power on a high impedance node for more efficient conversion to baseband without losing power due to impedance mismatch between the antenna and rectifier. Understandably, the input impedance of the rectifier, which is design-dependent and typically consists of a large resistance and reactance in shunt, affects the efficacy of such an approach. A large shunt resistance and a high transformation ratio are typically sought after for the rectifier input and the preceding transformer, respectively.

One effective method to achieve a large transformation ratio under conjugate match is to use a tapped capacitor matching network based on lumped elements [7], [8]. However, it requires a bulky shunt inductor that needs to be shielded or packaged from electromagnetic interference. Moreover, the frequency selectivity of the matching

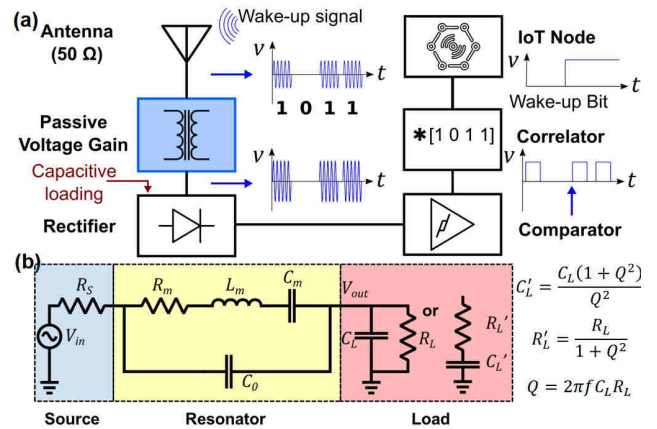


Figure 1: (a) Notional scheme of a low-power wake-up radio receiver system with an impedance transformer. (b) Equivalent circuit model for the resonator array loaded with the input impedance of the CMOS rectifier, which is represented by C_L and R_L in shunt or C_L' and R_L' in series.

network is limited due to moderate Q of the lumped inductor, and consequently is insufficient to reject nearby blockers. Alternatively, high Q resonant MEMS transformers utilizing a variety of modes have been demonstrated recently in different piezoelectric platforms, including the extensional mode in PZT [9], S0 [4] and cross-sectional Lamé mode in AlN [10]. However, the ultimate voltage gains of these two-port implementations are fundamentally limited by their moderate FoM, which is defined as the product of the electromechanical coupling (k_r^2) and quality factor (Q), and the self-loading effects. To further improve the voltage gain, LiNbO₃ S0 [11] and SH0 [12] transformers have been recently investigated in hopes of exploiting the demonstrated high FoMs of these modes in LiNbO₃ [13], [14]. Nevertheless, these devices are still inadequate in transforming impedance close to the input impedance of a CMOS rectifier due to either their small static capacitance (C_0) or spurious modes near the resonance.

In this work, we report an approach of using a one-port MEMS resonator to perform impedance transformation and voltage amplification [Fig. 1(b)]. Although a conjugate match to a typical CMOS rectifier is not attainable using such a method, the large C_0 and high FoM demonstrated in this work can still enable a substantial voltage gain. More importantly, different from tapped capacitors and our prior MEMS and CMOS integration for wake-up radios [7], this approach does not resort to any lumped inductors with moderate Q s. Therefore, narrowband filtering of noise can also be attained, while the drawbacks from integrating a lumped inductor are avoided.

PASSIVE VOLTAGE AMPLIFICATION

As seen in Fig. 1(b), our approach directly integrates a one-port resonator between the source and a low power CMOS rectifier for impedance transformation. C_L (1.07pF)

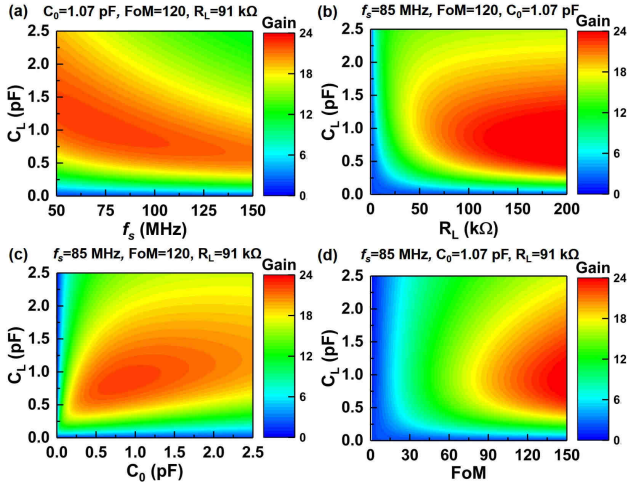


Figure 2: Voltage gain of a one-port resonator terminated with a complex load. The influence of the five parameters, including f_s , R_L , C_0 , and FoM, on the systematic gain are investigated respectively with different C_L .

and R_L (91k) are used to represent the parasitic capacitance from integration and the input impedance of a low power CMOS rectifier similarly designed to the one shown in [7]. To design the one-port resonator for attaining the highest voltage gain over the load impedance, we use a resonator equivalent circuit model shown in Fig. 1 (b). The motional elements, R_m , C_m , and L_m , represent the mechanical resonance, while C_0 symbolizes the static capacitance. Z_{res} is the impedance of resonator. These components can be determined with four independent parameters, series resonant frequency f_s , Q , k_t^2 , and C_0 by [12]:

$$R_m = \frac{\pi^2}{8} \cdot \frac{1}{2\pi f_s C_0} \cdot \frac{1}{k_t^2 Q} \quad (1)$$

$$L_m = \frac{\pi^2}{8} \cdot \frac{1}{(2\pi f_s)^2 C_0} \cdot \frac{1}{k_t^2} \quad (2)$$

$$C_m = \frac{8}{\pi^2} \cdot C_0 k_t^2 \quad (3)$$

$$Z_{res} = (R_m + j2\pi f L_m + 1/(j2\pi f C_m)) // (1/j2\pi f C_0) \quad (4)$$

where f is the operating frequency. A transducer voltage gain can be defined as the ratio of the voltage at the output of the resonator to the voltage provide by source over a matched load ($V_{in}/2$):

$$G_v = 2V_{out}/V_{in} = \frac{2Z_L}{R_s + Z_L + Z_{res}(f_s, FoM, C_0)} \quad (5)$$

$$Z_L = R_L // (1/j2\pi f C_L) \quad (6)$$

where R_s is the source impedance, Z_L is the load impedance. The highest transducer voltage gain occurs at a frequency at which all reactive elements, C_m , C_L , C_0 and L_m , in Fig. 1(b) tune out. This frequency, referred as gain resonance, is between the series and anti-resonances of the resonator, and has a cumbersome closed form expression. Thus, we adopt a numerical approach to calculate G_v as a function of operating frequency between f_s and f_p , and subsequently find the max G_v and gain resonance. The dependence of max voltage gain on key parameters can be then evaluated using the same numerical method.

From Eq. 1-6, we recognize that the key factors affecting transducer voltage gain are C_0 , FoM, f_s , the load imped-

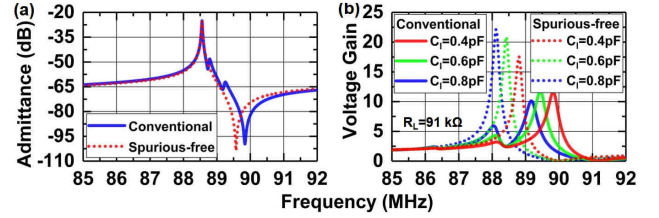


Figure 3: Predicted voltage gain of the resonator array. A 1pF spurious-mode free resonator array with a FoM of 120 is used for identifying the importance of spurious mode free response.

ance C_L , and R_L . Targeting unattended ground sensor application, the center frequency is selected around 85 MHz [15] for its optimal near-ground propagation of EM waves. Thus, the parameters will be studied numerically with the f_s varied near 85 MHz and load impedance varied near the aforementioned rectifier impedance.

As seen in Fig. 2(a), the impact of f_s on the voltage gain is plotted with different C_L showing that lower frequency systems can provide a larger gain for a wider range of C_L . It is also not surprising to see in Fig. 2(b) that a larger R_L leads to larger voltage gain. Fig. 3 shows the effects of C_0 is investigated with different C_L . It is essential to make C_0 comparable with C_L for best performance. Most importantly, a high FoM is shown in Fig. 2(d) to be crucial in achieving a high voltage gain.

In addition to the design considerations that have been studied in Fig. 2, the spurious modes between the series and parallel resonances have been shown to degrade the gain. Performance of a typical LiNbO₃ resonator without spurious mode suppression is displayed along with a spurious-free resonator [Fig. 3 (a)]. As seen in Fig. 3(b), the comparison of their voltage gain performance shows that spurious mode suppression is also required for consistently achieving high gains for a wide range of complex loads.

In this work, f_s and R_L are fixed for the optimal operation of the EM propagation and CMOS rectifier. Therefore, our design effort has been focused on achieving an optimal C_0 , a high FoM, and a spurious-mode free response. More specifically, the static capacitance C_0 should be set roughly equal to the load capacitance C_L , while the FoM should be as high as possible. Spurious modes between the series and parallel resonances should be eradicated to avoid gain reduction.

RESONATOR DESIGN

To achieve the abovementioned performance goals for a one-port resonator, we resort to a large array of 56 LiNbO₃ identical resonators with the layout shown and key parameters listed in Fig. 4 (a). Each resonator is composed of 700 nm LiNbO₃ thin film and a pair of interdigitated electrodes on the top. SH0 mode at -10° to $-Y$ axis on X-cut LiNbO₃ is selected for its demonstrated high k_t^2 and Q [16]. The resonant frequency is designed to be around 85 MHz by setting the lateral dimensions of the resonator to be 19 μm . The array configuration can achieve spurious mode mitigation using smaller resonators with sparse overtones [17], while increasing the total static capacitance to over 800 fF, and a foot print of a 0.5 by 1.1 mm.

In order for the large array of resonators to perform as one large resonator, two steps have been taken to ensure

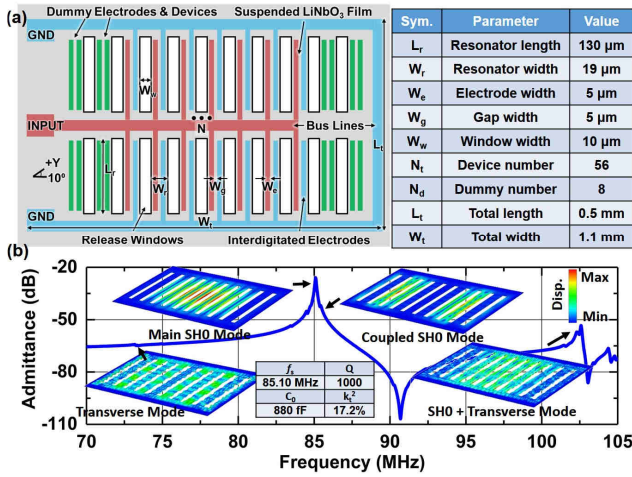


Figure 4: (a) Schematic of the designed high static capacitance, spurious-mode free LN resonator array with key dimensions shown in the table. (b) Simulated admittance response of the resonator array with the extracted key performance parameters listed in the inset table. The displacement mode shape of the main SH0 mode is presented along with the spurious modes.

that the arrayed resonators are truly identical in performance. First, gaps between adjacent resonators and release regions are optimized to minimize the coupled modes across multiple resonators. Second, dummy devices and resonators are placed on both ends of the array for reducing resonance deviation in devices near the ends of the array. The simulation using Coventor [Fig. 4 (b)] also confirms the high FoM and the large static capacitance with various modes being sufficiently suppressed. The mode shapes of the spurious modes are also shown in Fig. 4 (b), confirming that the optimized layout is effective in reducing k_t^2 of the coupled resonance modes.

FABRICATION AND MEASUREMENT

The designed resonator array was fabricated with a process reported in our prior work [12]. The optical and the scanning electron microscope (SEM) images of the fabricated devices are shown in Fig. 5. Great uniformity is seen across the resonators in the array [Fig. 5 (a-b)].

The device was measured with a Keysight N5249A network analyzer. The measured admittance [Fig. 6 (a-c)] shows very slight frequency variation for resonances across the array. The extracted key parameters are shown in the table. The device features a high total capacitance of 1.05 pF that includes the 246 fF parasitic capacitance from the bus line feedthrough. The measured k_t^2 , without de-embedding the effect of the parasitic capacitance, is 13.12%. The effective Q of the array is extracted to be 915. The high k_t^2 and Q lead to a measured FoM of 120, thus permitting a great voltage gain for a wide range of loading. As predicted by simulations, the measured admittance response also shows a wide band spurious-mode free range between series and parallel resonances. The minor spurious modes are caused by thickness-direction overtone coupling between the input and the ground bus lines, as evidenced by the spurious modes in the measured feedthrough of a test structure with only the input and output bus lines [Fig. 6(a) and (b)].

The extracted voltage gains are demonstrated in Fig. 7.

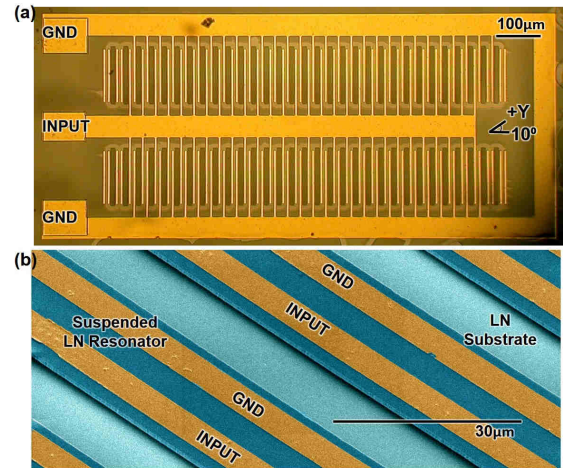


Figure 5: (a) Optical microscope image of the fabricated array with the marked input and ground ports. (b) SEM of the array showing the suspended LN film and well-defined sidewalls.

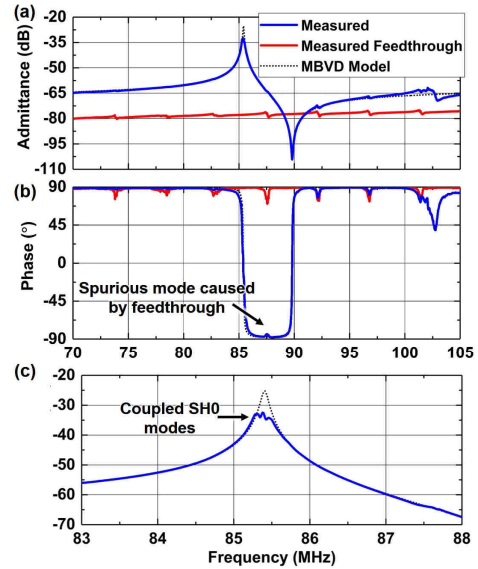


Figure 6: Measured admittance of the fabricated resonator array in (a) amplitude and (b) phase, with the resonance zoomed-in (c).

The results in Fig. 7 are attained by representing the resonator with measured data and then loading the resonator with the specified complex loads in a circuit simulation. A high voltage gain (> 20) has been achieved for a wide-range of complex loads (considering a shunt input resistance of 91 k Ω [2]), thus suggesting that our approach is very robust against any additional parasitic capacitances in the integration with CMOS. The gains obtained from measured data also match well with the gains calculated from the extracted model. The discrepancy in extracted gains for $C_L = 1.2$ pF is caused by the spurious modes in the feedthrough. It is noteworthy that our approach, although shown for complex loads in this work, is also applicable to other types of rectifying devices with predominately reactance as the input impedance [3], [18].

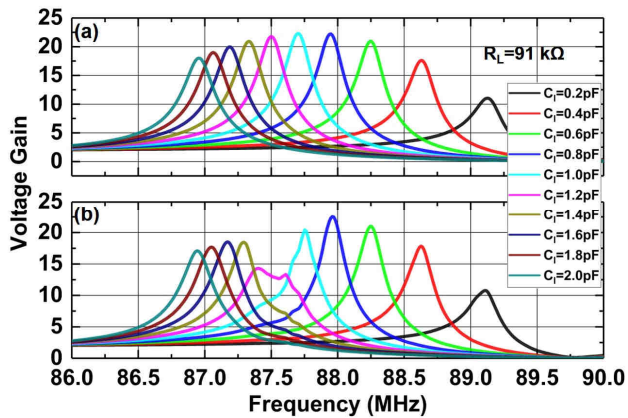


Figure 7: Voltage gains of the resonator array extracted using (a) the MBVD model and (b) the measured data with different load capacitances.

CONCLUSION

In this paper, a LiNbO_3 resonator array is designed and implemented based on the theoretical analysis of the dependence of maximum voltage gain on key resonator design parameters. The fabricated array with 56 parallel devices meets three design goals of achieving an adequately large static capacitance, a high FoM, and a spurious-free response. The measurement shows a large static capacitance of 1.05 pF, a measured FoM of 120, and a response with only significantly suppressed spurious modes. These performance specifications collectively result in a high voltage gain over 20 at the output of the array for complex loads over a wide range from 0.54 to 1.01 pF (with a shunt resistance of 91 kΩ).

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