WAFER-LEVEL SHELLAC-BASED INTERCONNECTION PROCESS FOR ULTRATHIN SILICON CHIPS OF ARBITRARY SHAPE

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ABSTRACT

This work addresses the interfacing of ultrathin microchips based on silicon (Si) with highly flexible, polymer-based cables of several centimeters in length. More specifically, we target chronically implantable neural probes with cross-sections as small as 120×50 µm^2 designed for intracortical applications. The study describes the development of a novel fabrication process based on the temporary fixation of multiple Si chips in a sacrificial polymer matrix. In contrast to existing approaches, our post-CMOS compatible process provides in particular economic advantages since chips are temporarily transferred from standard Si substrates into shellac for the purpose of chip interfacing, thereby saving valuable area on the Si substrate. Furthermore, the shellac matrix inherently adaptes to any chip shape during device embedding. This avoids preparing expensive Si handle wafers with design-dependent recesses realized using micromachining. We combined multiple 50-µm-thick Si chips with 10-µm-thin Parylene-C interconnects and successfully released the assemblies from the sacrificial shellac substrates. We verified the electrical connection between cable and chip at contact dimensions as small as 10×10 µm^2 and tested the chip/cable bond in a 90°-peel test with excellent results.

INTRODUCTION

Chronically implantable brain machine interfaces may lend themselves for future applications in therapies of neural disorders, rehabilitation and neuroprosthetics. The long-term stability of these technical interfaces in neural tissue is however limited due to tissue reaction. It is widely accepted that the foreign body response is strongly linked to the dimensions and mechanical properties of these neural implants. In particular small, flexible implants floating in neuronal tissue demonstrated superior biocompatibility [1].

Previously, we demonstrated a novel concept for flexible, high-density neural probes applying a chip-level assembly process [2] followed by mechanical probe stiffening using a biodegradable polymer [3]. Compared to established probe designs for chronic in vivo applications [4], this concept enabled a reduction of probe stiffness by a factor of around 1400 achieved by substituting large proportions of the Si shafts with a flexible, polymer interconnecting section. The resulting hybrid Si-polymer device of increased mechanical flexibility, as illustrated in Fig. 1(a), comprises high-density electrode arrays. As the process is inherently CMOS-compatible, integrated circuitry can in addition be integrated into the probe shafts enabling the concept of electronic depth control (EDC) [5]. In particular flexible neural probes that cannot easily be repositioned within the brain tissue after implantation may benefit from an electronic control of the recording site position with regard to their long-term recording stability. The applied chip-level assembly process and obvious challenges in neural probe handling impede however a further size reduction significantly below the actually achieved chip cross-section of 120×50 µm^2 at a given contact density of 272 contacts/mm^2.

Wafer-level interfacing of Si-based probes with flexible polymeric cables is a widely accepted technological approach [6-8]. It enables neural probes to be monolithically integrated in a highly efficient way with mm-long cables. The most recent approaches [7,8] focus on a further miniaturization of the stiff Si component targeting the biological impact of these devices. Despite the inherent conceptual advantage with respect to the alignment accuracy, directly fabricating polymer interconnects on valuable Si substrates is economically unacceptable as large proportions of the valuable substrate area is used just as a mechanical support of the cables. This is even more relevant for probes realized using CMOS technologies to increase the overall channel count [5].

This paper reports on a novel approach that combines the economical advantage of a separate probe fabrication with the accuracy of wafer-level cable interfacing. This is achieved using shellac-based sacrificial substrates temporarily aligning and fixating the delicate Si probes of minimal size during cable fabrication.

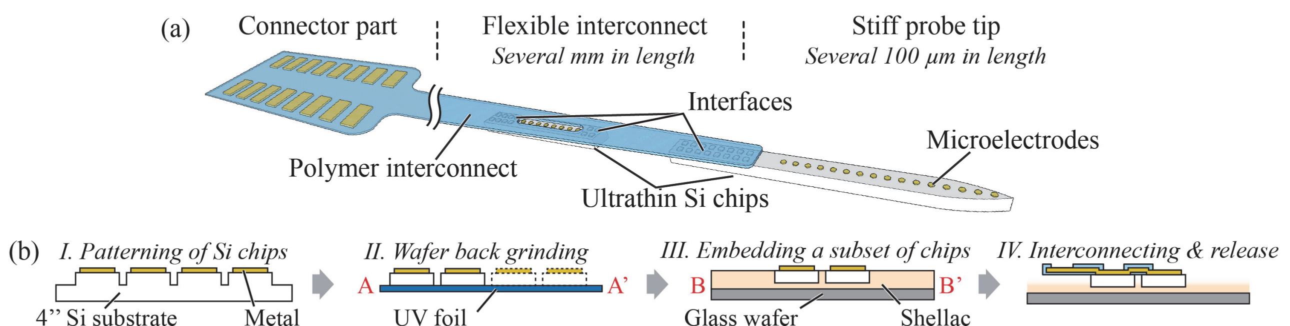

Figure 1: Schematic of (a) multi-chip neural probe of reduced foot print and (b) process flow of the demonstrated shellac-based interconnection process; cross-sectional views relate to the lines A-A' and B-B' indicated in Fig. 3.

INTERCONNECTION APPROACH

The novel wafer-level interconnection approach for ultrathin Si chips based on the sacrificial shellac matrix is outlined in Fig. 1(b). First, Si chips are realized on standard 4-inch Si wafers. This includes a bottom insulation, metallization, passivation, and definition of the chip contour by deep reactive ion etching (DRIE) {Fig. 1(b,I)}. These structures are translated into ultrathin chips using a subsequent wafer grinding from the wafer rear side {Fig. 1(b,II)}. This process was introduced by Herwik et al. as the etching before grinding (EBG) process [9]. A subset of the resulting ultrathin chips is transferred from a supporting UV tape into the novel sacrificial substrate {Fig. 1(b,III)}. In the following process sequence, interconnects based on Parylene-C (Px-C) are directly deposited and patterned on the Si chips that are temporarily secured in the shellac matrix {Fig. 1(b,IV)}. Finally, the shellac substrate is dissolved to release the Si-polymer assemblies without the necessity to apply external forces.

In view of a potentially improved chip alignment and a facilitated chip release, we chose a sacrificial substrate concept over a more common approach involving rigid, Si-based handle wafers [10]. Such handle wafers feature cavities that are intended to secure and align microchips during the subsequent wafer-level processing steps. The lateral accuracy of chip positioning is however strongly dependent on the clearance between chip and wafer cavity sidewalls. Obviously, a tighter fit between chip and cavity results in a better alignment. In our case, it would also leave a smaller lateral gap between chip and wafer that has to be bridged by the polymer interconnect. The chip release after coating with Px-C is delicate, however, and has proven to require large mechanical forces potentially destroying the chip-cable interface. Furthermore, the vertical chip alignment in the wafer cavities relies on tight tolerances for the etched cavity depth and ground chip thickness. Variations of both parameters result in an unavoidable vertical step between wafer and chip surfaces influencing among others the accuracy of photolithography. The step might further result in discontinuities in the electrical interconnection.

These critical processing issues of the handle wafer-based approach are addressed by our new fabrication concept. It aligns both, the chips and the sacrificial substrate, with respect to their front sides. Further, the shellac material avoids gaps around the chips occuring in the handle wafer concept. In addition, the dissolution of the shellac matrix at the end of the fabrication process minimizes forces acting of the Si-polymer assemblies during release.

MATERIALS AND PROCESSING

Shellac has recently been established as a substrate material for environmentally friendly microfluidics [11]. The thermoplastic is known to be quickly dissolved in boiling alcohols, e.g. ethanol (EtOH), which enables a fast and controlled release of components embedded in it. Solvents and developers used in photolithography can however cause its swelling or even dissolution. The proposed use of a Px-C coating applied in our process sequence {Fig. 1(b,IV)} already provides an elegant solution to this problem. The Px-C film constituting the bottom insulation layer of the electrical interconnect conformally covers the entire shellac substrate. With an appropriate process design this protective layer can be kept intact until the end of the last lithography step. Solvent compatibility was therefore not found to be a hindrance for microfabrication.

A second challenge is that the glass transition temperature of the pristine shellac was measured to be only around 43°C. Thermal annealing of the material offers the possibility to raise the glass transition temperature. Nonetheless, the processing temperatures in this work were kept as low as possible. For instance, baking steps applied for photoresists are generally performed for a prolonged duration at 60°C in vacuo. Dry etching and deposition processes are operated in a stepped mode to alleviate the secondary effect of substrate heating.

The test chips used in this study are fabricated as for the EBG process [9]. In summary, a patterned titanium (Ti)/gold (Au)/Ti metallization is sputter deposited on a stress-compensated insulating layer stack of SiO_x/Si_xN_y deposited by plasma enhanced chemical vapor deposition. In contrast to standard Si-based probes, the top passivation is omitted in this case. Finally, 50-µm-thick test chips are patterned and released using a combination of DRIE and wafer grinding.

The Px-C interconnecting process is shown in detail in Fig. 2. The transfer of the Si chips into the sacrificial shellac substrate after EBG processing starts with positioning an array of Si chips on a PDMS foil {Fig. 2(a)}. A laser-cut Kapton mask (Kapton HN, DuPont de Nemours, Luxembourg) defines the relative positions within the chip array. The mask is placed centrally on the PDMS foil where it readily adheres. It allows manual positioning of the chips up-side down without damaging the chip metallization. Next, PDMS foil and chips are coated with a 0.2 wt-% solution of shellac (Schellack Astra, Dictum GmbH, Metten, Germany) in EtOH {Fig. 2(b)}. The subsequent baking step at 80°C simultaneously extracts the solvent and anneals the shellac. This laminate is then thermally bonded to a 4-inch glass substrate at 80°C {Fig. 2(c)}.

After peeling off the PDMS foil, the chip surface is cleaned and activated in an O_2 plasma. This is followed by

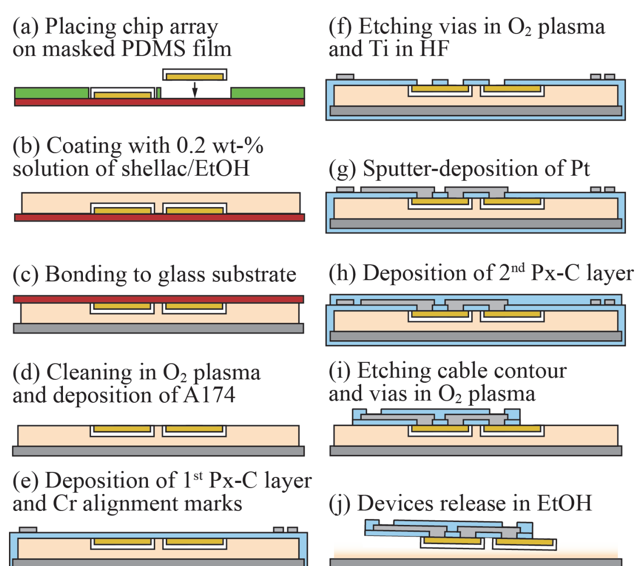

Figure 2: Schematic of the wafer-level interconnection process for Si chips embedded in a sacrificial shellac substrate.

the deposition of the adhesion promotor A174 (Sigma, Germany) {Fig. 2(d)} and a first 5-µm-thick Px-C layer using a vapor phase process (PDS 2010 Labcoter 2, Specialty Coating Systems, Indianapolis, IN, USA). The Px-C layer constitutes the passivation of the wiring in the interconnecting sections and also on the chips.

As the chips are only aligned with respect to each other, a set of chromium (Cr) alignment marks is deposited relative to the chip array for the subsequent photolithography steps. We applied an adapted lift-off process that fulfills the temperature constraints of the applied shellac material. The dual-layer resist process involves the spin-coating of LOR3A (MicroChem Corp., Westborough, MA, USA) and a 1.8-µm-thick layer of AZ1518 (Microchemicals GmbH, Ulm, Germany) with an intermediate bake at 60°C for 2 h in vacuo. The layer stack is then prebaked over night. After UV exposure and manual development in AZ726 MIF (Microchemicals GmbH), 40 nm of Cr are deposited by evaporation {Fig. 2(e)}.

Next, the chip metallization is exposed by reactive ion etching (RIE) of the Px-C layer in an O_2 plasma using the photoresist AZ9260 (Microchemicals GmbH) as an etching mask {Fig. 2(f)}. The resist is prebaked for several hours and allowed to rehydrate over night. The etching of the vias is performed in several steps to maintain the wafer temperature at a moderate level. The topmost exposed Ti layer of the Si chips is finally removed by dipping the wafers into 1% hydrofluoric acid {Fig. 2(f)}.

A 200-nm-thick platinum (Pt) layer is then sputter-deposited in multiple layers in order to minimize substrate heating {Fig. 2(g)}. AZ4533 (Microchemicals GmbH) with a thickness of 5 µm serves as an etch mask. The metallization is patterned by argon ion milling at an angle of 70°. The surface is finally cleaned in an O_2 plasma.

After depositing the second Px-C layer {Fig. 2(h)}, the cable contour is defined by RIE {Fig. 2(i)}. Following the resist strip, the chips are released by exposing the shellac-based substrates to EtOH heated to boiling temperature {Fig. 2(j)}. The chips are released after 1 to 2 h and finally cleaned using fresh EtOH and DI water.

EXPERIMENTAL RESULTS

Figure 3(a) shows four sets of Si test chips held in place by a UV tape attached to the rear side of the chips. A corresponding subset of chips embedded in shellac is shown in Fig. 3(b). Each chip set includes two larger chips for mechanical testing of the bond between the chip and the Px-C interconnect. The smaller chips are intended for electrical testing of line integrity before and after releasing the Si-polymer assemblies from the shellac substrate. The respective wiring in the chip metallization is shown in Fig. 3(c). It applies a two-wire resistance measurement between pads on the cables, as schematically shown in Fig. 3(c), and pads on the chips. As indicated in Fig. 3(c), the test can be performed with single chips as well as with multi-chip assemblies.

Figure 4 exemplarily shows fabrication results of the Px-C interconnection process. Multi-chip assemblies as proposed were successfully implemented. No chips were found to delaminate during the releasing procedure. Also, no partial delamination of the Px-C coating was observed indicating in general a qualitatively strong bond.

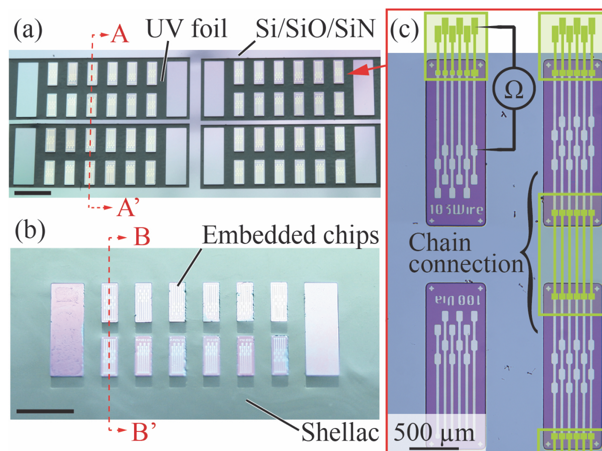

Figure 3: Micrographs showing (a) ultrathin chips realized by EBG and (d) a subset of the chips embedded in shellac (scale bars are 2 mm). (c) Test chips with unpassivated metal pads for probing and interconnecting as schematically indicated.

The integrity of the electrical interconnection between cable and chip was verified for line widths of 20 µm and vias as small as 10×10 µm² in size. The channels on the test chips were probed before and after the release step. No channels were lost during this procedure. However, an increase in resistance between 3 and 8.5% from initial values between 63 to 66 Ω for a roughly 2-mm-long interconnect section was observed.

BOND TESTING

Quantification of the adhesion between the bottom Px-C layer and the PECVD SiO_x/Si_xN_y chip passivation was performed using a 90°-peel test. For handling purposes, dedicated test chips were adhesively bonded to a glass slide {Fig. 5(a)}. Peel test were performed at 500 µm/s using a multipurpose bond tester (Dage Series 4000, Dage Deutschland GmbH, Dettingen unter Teck, Germany). The adhesion strength P_{90} is calculated as $P_{90} = F/w$ where F and w denote the average recorded force during peel off and the width of the interface, respectively. Literature values for P_{90} are on the order of 100 mN/mm for Px-C on A-

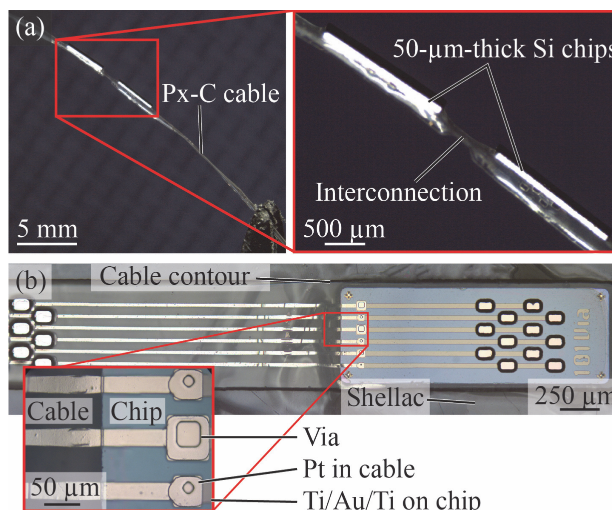

Figure 4: Micrographs of (a) Px-C/Si devices after release in EtOH. The ultrathin Si chips were successfully connected via a Px-C cable with metal lines.

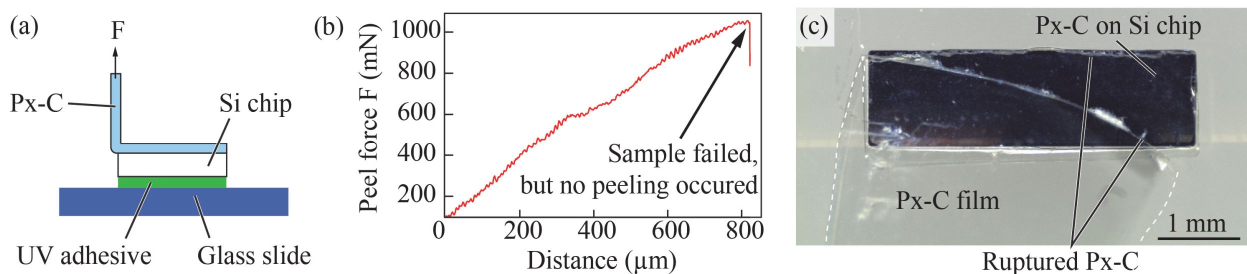

Figure 5: (a) Schematic of 90° peel test, (b) exemplary result of a peel test on 4-mm-wide samples, and (c) optical micrograph of a sample after peel testing showing ruptured Px-C. The Px-C layer could not be peeled off the chips.

174-treated PECVD Si_xN_y [12]. For the 4-mm-wide samples, forces of around 400 mN were thus expected.

In our experiment, forces of up to 1 N were recorded for chips treated with O_2 plasma and A-174 {Fig. 5(b)}. In most cases, the test specimen failed without significant peeling. The samples rather showed rupturing of the cable itself, as indicated with the sample in Fig. 5(c), where the Px-C cable ruptured at the border of the test chip at 700 mN. The extracted tensile strength of Px-C interconnects of around 35 to 50 MPa are in good agreement with previously reported values [12]. The experimental results clearly demonstrate the excellent mechanical performance of our Si-polymer assemblies.

CONCLUSIONS

In this work, we presented a novel wafer-level interconnection process for ultrathin Si chips with highly flexible, Px-C-based cables. The constituting materials of the Si/polymer assemblies are established in neural technology and allow for the implementation of high-density, multi-chip electrode arrays for neural recording. The novel shellac-based process demonstrates a promising route for CMOS-compatible post-processing of Si chips in terms of economic usage of wafer area and improved chip alignment and fixation. Single and multi-chip devices have been successfully implemented in this work. Electrical functionality has been verified and the mechanical performance of the samples is excellent. Future work has to focus on the extraction of geometry-specific design rules and the implementation of flexible neural probes featuring EDC.

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