A TRANSFER-FREE WAFER-SCALE CVD GRAPHENE FABRICATION PROCESS FOR MEMS/NEMS SENSORS

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ABSTRACT

In this paper we report a novel transfer-free graphene fabrication process, which does not damage the graphene layer. Uniform graphene layers on 4" silicon wafers were deposited by chemical vapor deposition using the CMOS compatible Mo catalyst. Removal of the Mo layer after graphene deposition results in a transfer-free and controlled placement of the graphene on the underlying SiO_2. Moreover, pre-patterning the Mo layer allows customizable graphene geometries to be directly obtained, something that has never been achieved before. This process is extremely suitable for the large-scale fabrication of MEMS/NEMS sensors, especially those benefitting from specific properties of graphene, such as gas sensing.

INTRODUCTION

Graphene is an attractive new material for many sensors because of its unique electrical and thermal properties. It is particularly interesting for gas sensing, due to it large surface area (essentially there is no bulk), extreme sensitivity down to single molecules [1], and low electronic noise [2], Due to its room temperature operation and small size, graphene sensor can potentially be integrated in hand-held and mobile devices, enabling toxic gas sensing at an unprecedented scale.

This exciting new material was first isolated by Geim and Novoselov in 2004 by using scotch-tape exfoliation from a graphite crystal [3]. Although this synthesizing process is surprisingly simple and low cost, enabling a rapid expanding research effort in graphene, it is not industrially scalable. From all methods of synthesizing graphene, including liquid exfoliation and epitaxy from crystalline SiC wafers, chemical vapour deposition (CVD) on a metal catalyst is currently widely regarded as the most promising large-scale synthesizing method. A whole range of metal catalyst has been investigated, but the most common ones are nickel for multi-layer graphene [4], and copper for mono-layers [5].

While the CVD deposition of graphene has progressed significantly, demonstrating growth on large metal foils or metal thin-films on wafers [6], [7], a graphene layer on a metal catalyst is impractical for most applications. In fact, this implies that transfer of the graphene layer towards another substrate is required. During transfer the metal film is removed and the graphene is transferred to a different substrate, after which devices can be fabricated utilizing the transferred graphene layer. In order to maintain the unique properties of the graphene layer it is important that the transfer process is clean, that is no residues of the metal or transfer medium remain after transfer, and no wrinkles are formed as they degrade the graphene electric properties [8], [9]. Ideally the transferred graphene should be placed directly at the desired location to minimize the required post-processing.

The majority of transfer methods use a polymer like poly-methyl methacrylate which is coated over the graphene layer and $FeCl_3$ to etch the Cu or Ni catalyst layer [10]. After the removal of the metal catalyst, the graphene on the polymer is retrieved from the etching solution and either wet or dry stamped to the target substrate. Subsequently the polymer is dissolved in hot acetone or another organic solvent. The problem of this method is that both the etching solution and the polymer leave residues on the graphene layer. Effort has been put in cleaning methods [11], different etching solutions, circumventing the etching by using electrochemical release, or by decreasing the adhesion between the metal and graphene by oxidation [12], [13]. Other researchers investigated the use of polymer layers which can be removed more easily or from which the graphene can be detached by heating [8], [13], [14]. Currently, no scalable transfer method is available which results in a reproducible and clean transfer of the graphene layer to the desired location of a target substrate without degrading the grapheme layer quality.

In this paper we present a novel transfer-free, and semiconductor manufacturing compatible approach to the wafer-scale fabrication of graphene devices. Moreover, the method allows customizable graphene geometries to be obtained directly at the desired location. We employ the CMOS compatible molybdenum catalyst. Previously it has been shown that graphene could be deposited on Mo foils [15], and recently our group demonstrated graphene deposition on Mo thin-films [16]. By using this catalyst in combination with a transfer free fabrication method, graphene based gas sensors were fabricated and characterized.

EXPERIMENTAL

For the fabrication of the devices 4" Si (100) wafers were used as substrate. The process is illustrated in fig. 1. First, a thin-film of Mo is sputtered from a pure (99.95%) Mo target on top of 90 nm SiO_2, which was grown using thermal oxidation. As the melting-point of Mo (2623 °C) is much higher than that of Cu (1085 °C) and Ni (1455 °C), the catalyst film can be made as thin as 25 nm without the metal film segregating at the graphene CVD

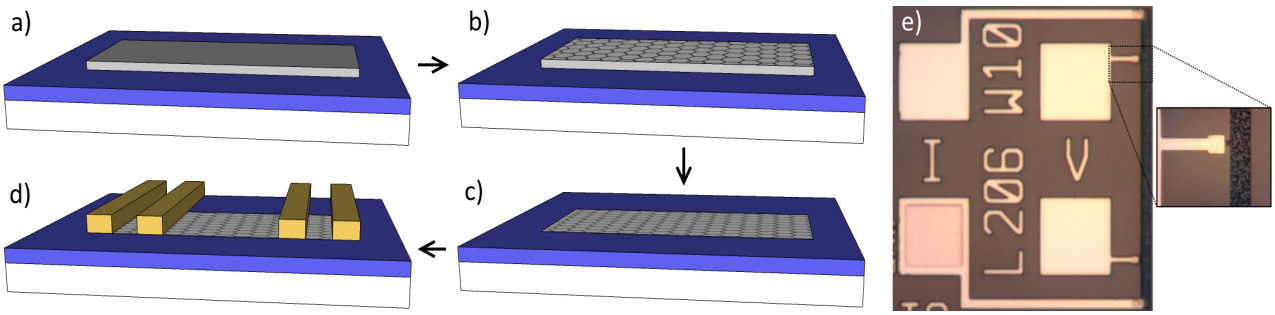

Figure 1: Schematic overview of the fabrication process: a) deposition and patterning of the Mo layer on Si substrate with 90 nm SiO_2; b) CVD deposition of graphene on Mo; c) wet etching of the Mo layer; d) deposition of Cr/Au electrodes using a lift-off process; e) micro-photograph of electrical test structure with a graphene line-width of 10 µm with close-up of Au-graphene contact.

temperature of 1000 °C. Moreover, this allows the film to be pre-patterned down to sub-micron dimensions for the selective growth of graphene. Dry etching with SF_6, in combination with a photo-lithographic resist layer, is used to pattern the Mo (fig 1a).

Graphene is deposited on the Mo catalyst using a commercially available AIXTRON BlackMagic Pro at 1000 °C using $Ar/H_2/CH_4$ as feedstock at a pressure of 25 mbar (fig. 1b). After the CVD deposition of graphene the Mo catalyst is rapidly etched using a phosphoric acid solution, after which the wafers are rinsed and spin-dried. As the distance between the graphene and SiO_2 after the Mo etching is relative small, the graphene directly sticks to the SiO_2 without floating away during the etching and rinsing (fig. 1c). Finally, Cr/Au (10/50 nm) electrical contacts are deposited using a lift-off process.

To monitor the graphene layer quality after deposition, Raman spectroscopy was performed using a Renishaw inVia Raman microscope with 633 nm laser. For the energy-dispersive X-ray spectroscopy (EDX) a JEOL JSM-6010LA with silicon drift detector was used. Electrical measurements were performed on a semi-automatic probe-station with an Agilent 4156C semiconductor parameter analyzer. The gas sensors were tested in a Gas Sensor Characterization System (GSCS, Kenosistec equipment) in which the relative humidity was controlled to 50% at 22 °C and which was fitted with MKS programmable mass flow controllers. The bias was supplied by a TTi QL355T precision power supply.

RESULTS AND DISCUSSION

During the fabrication process Raman spectroscopy was used to monitor the graphene layer, as the Raman spectra is highly sensitive to contamination and defects present in the graphene layer [17]. Fig. 2 displays the acquired spectrum at three stages during the process. The black line represents the graphene directly after CVD deposition on the Mo, while the red and green lines represent the graphene after Mo-etch and Au patterning, respectively. Four peaks can be distinguished: the D and D'-bands around 1330 cm^{-1} and 1620 cm^{-1}, respectively, which are related to defects in the broadest sense of the word, the G-band (1580 cm^{-1}) which originates from the sp^2 C-C bond, and the G' or 2D-band (2670 cm^{-1}) which relates to the number of graphene layers.

As can be observed from fig. 2, the D-band intensity

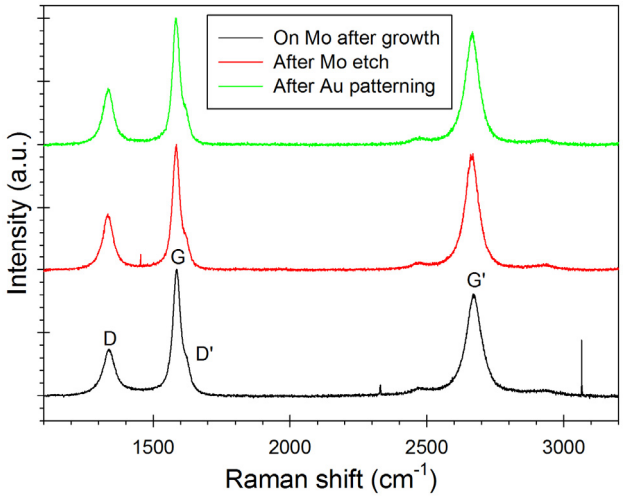

Figure 2: Raman spectra obtained at different stages in the process using a 633 nm laser, indicating no degradation of the graphene layer during processing.

and width remain constant throughout the process, which is a strong indication that no additional defects are being introduced. When the graphene still resides on top of the Mo, the graphene Raman signal is quenched by the metal, which is compensated here by increasing the exposure energy of the laser. The relative high D-band directly after growth comes from the CVD process and can be reduced by recipe tuning [15]. However, a controlled number of defects can actually be advantageous for gas sensing, as they provide reaction sites for the adsorption of molecules [18].

Using the process described in the previous section test devices were fabricated on 4" wafers. Fig. 1e displays a micro-photograph of an electrical four-point probe test structure. The Au contacts and the semi-transparent graphene layer, which has a more dark blue shade than the SiO_2, can clearly be observed. As the Mo is pre-patterned by dry etching, accurate micron-size features could be obtained in the graphene. This can clearly be seen in the inset of the Cr/Au-graphene contact, which features a 2 µm wide graphene line. For our process the minimum sizes which could be obtained were as small as 0.5 µm and was limited by our lithographic process. The contrast variations observed in the graphene appear to originate from slight variations in the number of graphene layers.

The average thickness of the graphene layer was

determined by transferring the layer to an optically transparent substrate and subsequently recording the UV-Vis transmission spectrum. At a wavelength of 550 nm the transmission is 59.5 %, from which the average number of layers is estimated to be 23, using the empirical equation from Zhu et al. [19]. As the growth of graphene on Mo is a bulk diffusion and precipitation process like for Ni, the number of layers can be tuned by changing the CVD parameters. As was shown by Wu et al. [15], the cooling rate has the biggest impact, where faster cooling leads to trapping of the C atoms in the Mo film and thus a thinner layer. Using a sufficiently fast cooling rate they demonstrated that mono-layers can be obtained on the Mo. We found that this is also possible on Mo thin-films, but so far have not been able to obtain a uniform mono-layer of graphene which is likely due to the limited cooling rate of our CVD reactor [16].

From the optical micro-graphs no residues of Mo are visible when the Mo layer was removed after growth, even when structures with sizes of hundreds of µm were etched. To verify that the Mo is indeed removed, EDX was performed in the centre of a 380 µm patch of graphene, of which the spectrum is shown in fig. 3. As can be observed, only the peaks, which are associated with C, O and Si are visible. At the location where normally the Mo peak can be found no feature can be distinguished with sufficient accuracy above the noise level. This indicates that the Mo is removed to such an extent that it is at least below the detection limit of the instrument. The strong graphene features in the Raman spectrum after etching also indicate that the graphene is now on SiO_2, instead of Mo which strongly quenches the graphene Raman spectrum.

Using the devices shown in fig. 1e, with different widths for the graphene line (2, 5, and 10 µm), four point probe electrical measurements were performed on the graphene layer. The obtained I-V characteristics are shown in fig. 4. The linear responses indicate that the contact between the Cr/Au and graphene layer is ohmic. Using the dimensions of the device the sheet resistance of the graphene layer can be estimated, which is on average 900 Ω/□. Using the approximate number of layers, which with a thickness of 0.34 nm per graphene layer results in a total thickness of 7.8 nm, this translates into a resistivity of 0.7 mΩ-cm. This is roughly two orders of magnitude higher than the theoretical minimum resistivity of a graphene mono-layer [20] which can be attributed to the relative high number of defects in the as-grown CVD layer. Using a semi-automatic probe station, 74 devices of each geometry were measured over the entire wafer. For the 10 µm device a yield as high as 97% and 89% was obtained for the 10 µm and for the 2 µm wide devices, respectively.

The devices were wire-bonded and tested in a controlled gas environment with two different gases: 1 ppm of NO_2 and 100 ppm of NH_3. The current response of the devices under a bias of 1 V is plotted in fig. 5. As gas molecules are adsorbed on the graphene layer, they alter the electrical characteristics, that is, dope the material. For the gases tested, NO_2 donates a hole, while NH_3 donates an electron. Our graphene layer has p-type electrical characteristics, as determined by the back-gated measurements shown in fig. 6. As expected, NO_2 gives rise to a lower resistance, while NH_3 increases the resistivity. The obtained response for the NO_2 gas is comparable to results from the literature [1], even if the device geometry has not yet been optimized.

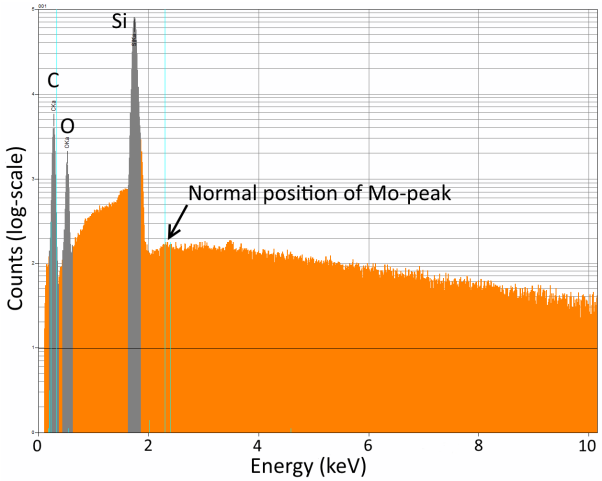

Figure 3: EDX spectrum of a sample after Mo etching. Only the Si, C and O peaks are visible. The count axis is in log-scale.

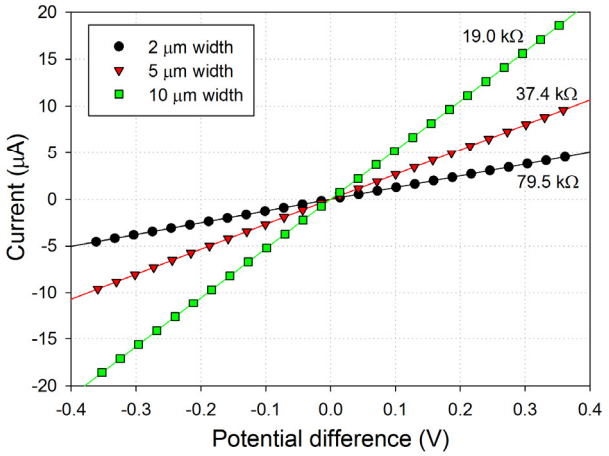

Figure 4: Typical I-V characteristics of graphene resistors with different widths (length 206 µm). The linear response indicates ohmic contact, R_{sheet} = 900 Ω/□

CONCLUSION

A novel transfer-free and semiconductor manufacturing compatible method for the wafer-scale deposition of graphene was presented. Besides providing a clean transfer of the graphene layer, this method also allows the exact patterning and placement of the graphene layer by pre-patterning the Mo catalyst layer. This method eliminates any need to further process the graphene layer. Using Raman spectroscopy it was shown that no additional defects were introduced by the fabrication method, while EDX confirms that the Mo is etched even in the centre of large graphene patches. The electrical measurements demonstrate ohmic contact between the graphene and Cr/Au layer, with a sheet resistance of 900 Ω/□ and a yield as high as 97 %. The response to gases confirmed the p-type nature of our graphene layer, while the conductivity change of 2.77 % for the non-optimized devices is comparable to what is reported in the literature.

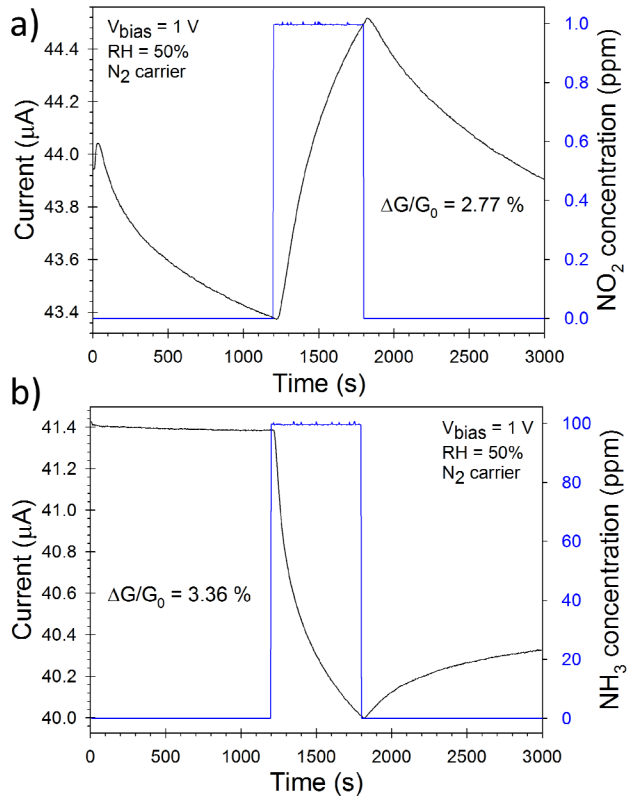

Figure 5: Current response of a wire-bonded device against: a) 1 ppm of NO_2 , b) 100 ppm of NH_3 . The carrier gas is N_2 and the humidity was controlled to 50%, V_{bias} = 1 V.

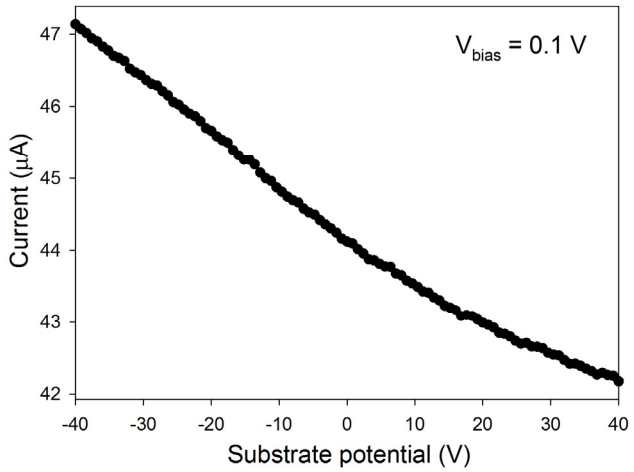

Figure 6: Current response of the graphene layer for a changing back gate potential. The oxide thickness is 90 nm, V bias = 1 V. Good contact to the Si substrate is assured by deposition of Al(1% Si) on the p-type Si substrate after a HF-dip has been performed.

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REFERENCES

[1] F. Schedin, A. K. Geim, S. V. Morozov, E. W. Hill, P. Blake, M. I. Katsnelson, and K. S. Novoselov, *Nat. Mater.*, vol. 7, pp. 652–655, 2007.
[2] A. A. Balandin, *Nat. Nanotechnol.*, vol. 8, pp. 549–555, 2013.
[3] K. Novoselov, A. Geim, S. Morozov, D. A. Jiang, Y. Zhang, S. Dubonos, I. Grigorieva, and A. Firsov, *Science*, vol. 306, no. 5696, pp. 666–669, 2004.
[4] Q. Yu, J. Lian, S. Siriponglert, H. Li, Y. P. Chen, and S.-S. Pei, *Appl. Phys. Lett.*, vol. 93, pp. 113103–1–3, 2008.
[5] X. Li, W. Cai, J. An, S. Kim, J. Nah, D. Yang, R. Piner, A. Velamakanni, I. Jung, E. Tutuc, S. K. Banerjee, L. Colombo, and R. S. Ruoff, *Science*, vol. 324, no. 5932, pp. 1312–1314, 2009.
[6] S. Bae, H. Kim, Y. Lee, X. Xu, J.-S. Park, Y. Zheng, J. Balakrishnan, T. Lei, H. R. Kim, Y. I. Song, Y.-J. Kim, K. S. Kim, B. Özyilmaz, J.-H. Ahn, B. H. Hong, and S. Iijima, *Nat. Nanotechnol.,* vol. 5, pp. 574–578, 2010.
[7] L. Tao, J. Lee, M. Holt, H. Chou, S. J. McDonnell, D. A. Ferrer, M. G. Babenco, R. M. Wallace, S. K. Banerjee, R. S. Ruoff, and D. Akinwande, *J. Phys. Chem. C*, vol. 116, no. 45, pp. 24068–24074, 2012.
[8] Y.-C. Lin, C. Jin, J.-C. Lee, S.-F. Jen, K. Suenaga, and P.-W. Chiu, *ACS Nano*, vol. 5, no. 3, pp. 2362–2368, 2011.
[9] W. Zhu, T. Low, V. Perebeinos, A. A. Bol, Y. Zhu, H. Yan, J. Tersoff, and P. Avouris, *Nano Lett.*, vol. 12, no. 7, pp. 3431–3436, 2012.
[10] Y. Lee, S. Bae, H. Jang, S. Jang, S.-E. Zhu, S. H. Sim, Y. I. Song, B. H. Hong, and J.-H. Ahn, *Nano Lett.*, vol. 10, no. 2, pp. 490–493, 2010.
[11] X. Liang, B. A. Sperling, I. Calizo, G. Cheng, C. A. Hacker, Q. Zhang, Y. Obeng, K. Yan, H. Peng, Q. Li, X. Zhu, H. Yuan, A. R. H. Walker, Z. Liu, L. mao Peng, and C. A. Richter, *ACS Nano*, vol. 5, no. 11, pp. 9144–9153, 2011.
[12] Y. Wang, Y. Zheng, X. Xu, E. Dubuisson, Q. Bao, J. Lu, and K. P. Loh, *ACS Nano*, vol. 5, no. 12, pp. 9927–9933, 2011.
[13] S. Y. Yang, J. G. Oh, D. Y. Jung, H. Choi, C. H. Yu, J. Shin, C.-G. Choi, B. J. Cho, and S.-Y. Choi, *Small*, vol. 11, no. 2, pp. 175–181, 2015.
[14] J. Kang, S. Hwang, J. H. Kim, M. H. Kim, J. Ryu, S. J. Seo, B. H. Hong, M. K. Kim, and J.-B. Choi, *ACS Nano*, vol. 6, no. 6, pp. 5360–5365, 2012.
[15] Y. Wu, G. Yu, H. Wang, B. Wang, Z. Chen, Y. Zhang, B. Wang, X. Shi, X. Xie, Z. Jin, and X. Liu, *Carbon*, vol. 50, pp. 5226–5231, 2012.
[16] Y. Grachova, S. Vollebregt, A. L. Lacaita, and P. M. Sarro, *Procedia Engineering*, vol. 87, pp. 1501–1504, 2014.
[17] A. C. Ferrari, *Solid State Commun.*, vol. 143, pp. 47–57, 2007.
[18] Y.-H. Zhang, Y.-B. Chen, K.-G. Zhou, C.-H. Liu, J. Zeng, H.-L. Zhang, and Y. Peng, *Nanotechnology*, vol. 20, no. 18, pp. 185504–1–8, 2009.
[19] S.-E. Zhu, S. Yuan, and G. Janssen, *Europhy.s Lett.*, vol. 108, pp. 17007–1–4, 2014.
[20] E. H. Hwang and S. D. Sarma, *Phys. Rev. B*, vol. 77, no. 11, pp. 115449–1–6, 2008.

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