ULTRA-SCALED HIGH-FREQUENCY SINGLE-CRYSTAL SI NEMS RESONATORS AND THEIR FRONT-END CO-INTEGRATION WITH CMOS FOR HIGH SENSITIVITY APPLICATIONS

E. Ollier, C. Dupré, G. Arndt, J. Arcamone, C. Vizioz, L. Duraffourg, E. Sage, A. Koumela, S. Hentz, G. Cibrario, P. Meininger, K. Benotmane, C. Marcoux, O. Rozeau, G. Billiot, E. Colinet, F. Andrieu, J. Philippe, F. Aussenac, D. Mercier, H. Blanc, T. Ernst and P. Robert*
CEA-LETI, MINATEC Campus, 38054 Grenoble, France

ABSTRACT

This paper reports on ultra-scaled single-crystal Si NEMS resonators (25-40nm thick) operating in the 10-100MHz frequency range. Their first monolithic integration at the front-end level with CMOS enables to extract the signal from background leading to possible implementation of direct/homodyne measurement, for high sensitivity sensing applications and portable systems.

INTRODUCTION

NEMS (Nano-Electro-Mechanical-Systems) are currently being investigated for promising applications, for example ultimate mass sensing in gas and biological applications. Low mass resolution and fast response obtained with NEMS have been reported [1,2]. NEMS have also shown their potentiality for portable multi-gas analyzers [3]. But down-scaling of NEMS comes with issues related to transduction at the nano-scale and interfacing with the macro-world. Indeed, optimized transduction is required to ensure good SNR (Signal to Noise Ratio) and excellent SBR (Signal to Background Ratio) is necessary to interface the sensing element.

NEMS operated in stand-alone configuration with a separated electronic circuit suffer from practical limitations because of the impact of pads and bonding parasitic capacitances on the background signal and SNR. Down-mixing or frequency modulation techniques can help but the laboratory equipments required are not suitable for integrated portable systems. Direct/homodyne measurement is preferable. This situation argues for integration of first electronic readout circuitry close to the NEMS [4]. First demonstrations of monolithic integration have been proposed with NEMS made in the Back-End oxides of a standard CMOS technology, the NEMS being made of Metal [5] of PolySi material [6]. A SON (Silicon-On-Nothing) technology has also been proposed to enable to fabricate the NEMS in single-crystal silicon [7].

Compared to this state-of-the-art, this paper presents ultra-scaled NEMS (25-40nm thick) made of single-crystal Si , capable to offer gravimetric detection with resolution down to ~ a few zg (10^{-21}g) or yg (10^{-24} g). The issues of transduction and interfacing are solved thanks to piezoresistive detection and co-integration of single-crystal silicon NEMS with a simple CMOS circuit.

DEVICE DESCRIPTION AND DESIGN

In this paper the dimensions of the so-called "crossbeam" NEMS [2] have been shrinked down to 40nm and have been embedded with a CMOS circuit based on FD(Fully-Depleted)-SOI technology from CEA-LETI. The "crossbeam" NEMS structure (Figure 1) is composed of a resonant cantilever beam, two lateral electrodes for actuation purposes and two piezoresistive gauges for the transduction of the mechanical motion that occurs in first in-plane flexural mode. Typically the beam is a few µm long and 40-100nm wide; nanowire gauges are 100nm long and 40-50nm wide; the electrostatic gap is 60-180nm. The CMOS circuit (Figure 1) is constituted of a low-noise high-frequency inverter analog amplifier (>60dB), a biasing stage and a buffer used to load 100pF connection capacitance without major signal attenuation. This CMOS circuit is described in details in [8]. A specific design kit has been developed, based on models of crossbeam NEMS [2] and FDSOI transistors.

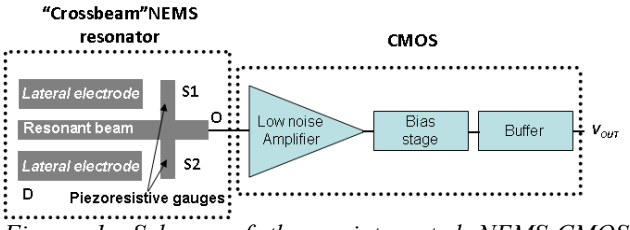

Figure 1: Scheme of the co-integrated NEMS-CMOS circuit including an amplifier, a bias stage and a buffer

CO-INTEGRATION TECHNOLOGY

Figure 2 shows SEM pictures of fabricated ultra-scaled single-crystal silicon NEMS co-integrated with their CMOS-FDSOI circuit monolithically integrated on the same silicon chip.

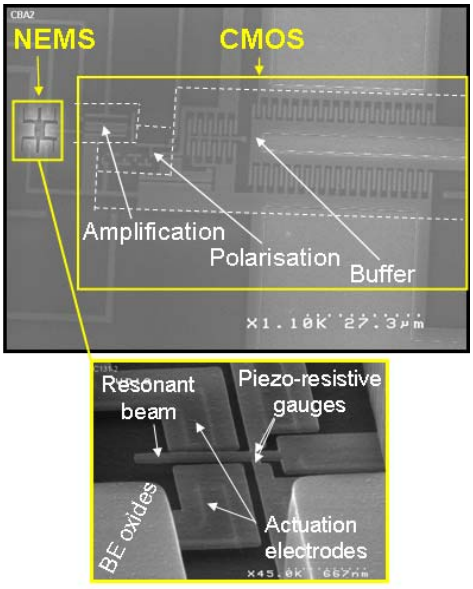

Figure 2: SEM view of ultra-scaled single-crystal NEMS monolithically co-integrated with CMOS-FDSOI.

The co-integration process (Figure 3) is done at the Front-End level of a CMOS-FDSOI technology with 16 mask levels. It enables to fabricate on the same chip NEMS devices made of single-crystal silicon and CMOS transistors based on FDSOI technology, both embedded in a thin 40nm SiTop layer of 200mm SOI wafers. This configuration enables to benefit of the excellent mechanical properties of single-crystal silicon (low residual stress, reliability) together with the capability to co-integrate simple CMOS circuits. The FDSOI process has been adapted to the NEMS requirements (gate length relaxed to 300nm) to ensure good gate control over the channel. Specific building blocks have been developed: patterning of ultra-scaled nano-structures, passivation and protection of the silicon nanowire surface by an oxide layer, final release of Si nanowires with CF4 isotropic etching of a Poly-Si encapsulation of the nanowires. The latter avoids any need of protecting the back-end oxides during the final release step.

The process is done on thin SOI substrate and starts with Phosphorus doping of the 40nm SiTop layer at 1.10^{19} at/cm^3. Then the NEMS are patterned in the 40nm thick SiTop layer thanks to hybrid DUV-EB lithography and dry plasma etching (Figure 3a) which is capable to define both large structures (tens of microns) and also nanowires 40nm large together with 60nm large gaps. A first release of the NEMS structure is made so that a thermal oxidation of the suspended NEMS can be realized to passivate and protect the nanowire silicon surface (Figure 3b). This first release uses HF-vapor etching of the 145nm thick BOX of the SOI substrate. Then the suspended NEMS are partially oxidized at 1100°C (Figure 3c) with specific conditions to control the 15nm oxide thickness and also the shape of the nanowire (Figure 4). The oxidized silicon NEMS structure is encapsulated by a conformal Poly-Si layer that is planarized so that its residual thickness is about 200nm over the SiTop (Figure 3d). This layer is a sacrificial layer that will be removed at the end of the process. Before CMOS process, a 200nm thick High Thermal Oxide (HTO) layer is deposited to protect the encapsulated NEMS and it is opened above both the NEMS contacts and the MOS areas (Figure 3d). Then the CMOS-FDSOI is processed at the Front-End level (Figure 3e), including gate stack deposition (3nm HfO_2 gate oxide, 60 nm TiN-PolySi gate) and etching, spacers formation, Source/Drain implantation, NiSi silicidation. The Back-End process is performed to contact and interconnect the NEMS structures and the CMOS transistors. Tungsten material is used for the electrical contacts. AlSi material is used for the unique metal level to form both interconnections and pads. In order to release the NEMS structures, the back-end oxides are anisotropically etched above the NEMS area down to the Poly-Si encapsulation layer. Then the NEMS are released thanks to a selective isotropic CF_4 chemical etching of the Poly-Si (selectivity relative to encapsulation thermal oxide: ~70) (Figure 3f). This release technique allows to avoid the need of protective layer for the back-end oxides thanks to its high selectivity relative to oxide materials.

Finally, Figure 5 illustrates this NEMS-CMOS co-integration technology thanks to cross-section SEM photographs of the NEMS beam and the MOS transistor.

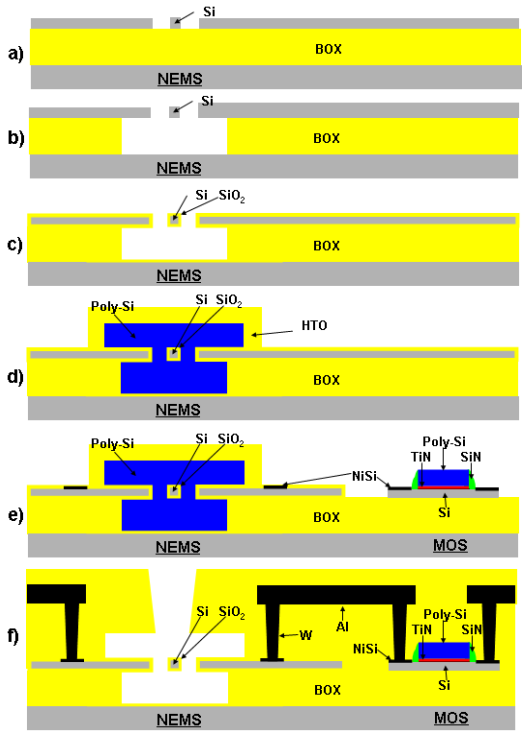

Figure 3: Schematic of the process flow of the co-integrated NEMS-CMOS_FDSOI technology

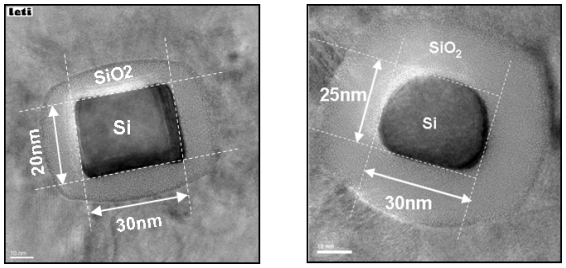

Figure 4: TEM photograph of the cross-section of the single-crystal silicon nanowire used as piezoresistive gauge and covered with a 10-15nm thermal oxide

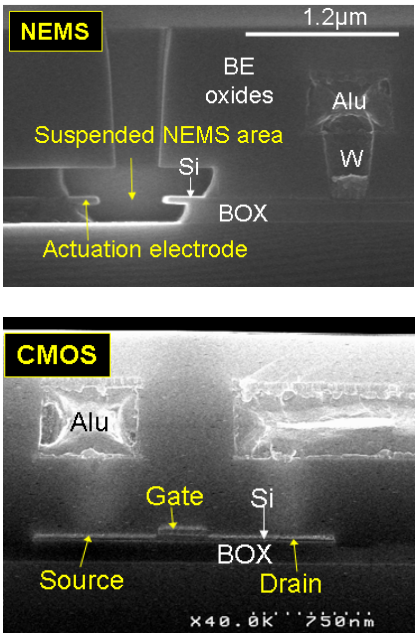

Figure 5: SEM photographs of the cross-section of the NEMS area and the MOS transistor.

ELECTRICAL RESULTS

Characterization of ultra-scaled NEMS in stand-alone configuration

To enable the measurement of the cross-beams devices in stand-alone configuration (without the CMOS circuit) independently from the CMOS circuit, a down-mixing technique was used. Indeed, this technique is mandatory to overcome the low signal-to-background ratio encountered with such down-scaled devices, otherwise the signal does not emerge from the background signal. The heterodyne piezoresistive downmixing technique described on Figure 6 converts the signal caused by the resonant mechanical motion (in the 100MHz range) at a lower frequency (10-100kHz), below the cut-off frequency of the output low-pass RC filter formed by the external connections in series with the NEMS output resistance. This results in very good signal-to-background ratio since the feed-through signals at the driving and bias frequencies are not down converted and are filtered.

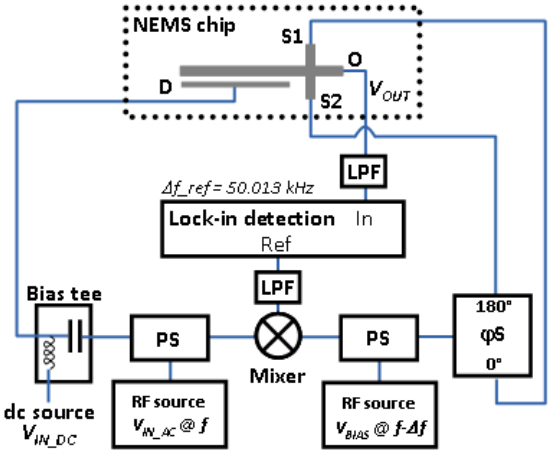

Figure 6: Scheme of heterodyne piezoresistive downmixing technique. PS: power splitter, LPF: low pass filter, ϕS: phase shifter.

Figure 7 shows the typical frequency response of an ultra-scaled 105 MHz "crossbeam" device measured in open-loop configuration. This device, fabricated in a single-crystal p-type (P doping - 1.10^{19} atm/cm3) silicon layer 40nm thick, is constituted of a cantilever beam 100nm wide and 1.2µm long, with two piezoresistive gauges 50nm large and 100nm long. The electrostatic gap is 110nm wide. The polarization conditions are Vbias=1V, Vin-ac=1V and Vin-dc=15V for measurement in air and Vin-dc=18V for measurement in vacuum. The high voltages applied are due to the large electrostatic gap (110nm) and also by the fact that these high voltages improve the signal-to-noise ratio. The quality factors are respectively 90 and 930 in air and vacuum. These experimental results demonstrated the good behavior of the fabricated ultra-scaled devices, but in the same time it emphasizes the difficulty to extract in a simple way a good electrical signal from these ultra-scaled devices used in stand-alone configuration.

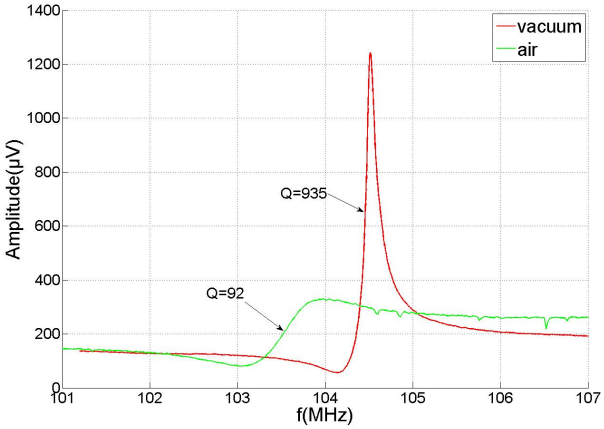

Figure 7: Frequency response of an ultra-scaled cross-beam in stand-alone configuration, measured with down-mixing technique. Si thickness: 40nm, beam: 100nm wide - 1.2µm long, piezoresistive gauges: 50nm large - 100nm long, electrostatic gap: 110nm. Vbias=1V, Vin-ac=1V, Vin-dc=15V in air and 18V in vacuum.

Characterization of ultra-scaled NEMS co-integrated with CMOS-FDSOI

Standard measurements (Figure 8) of Id(Vg) and Id(Vd) performed on embedded NMOS and PMOS (gate length:400nm, gate width: 10µm) validate this FDSOI-based technology embedding NEMS in its Front-End. Typical experimental characteristics of the CMOS transistors are in good agreement with the expected characteristics. Threshold voltages V_t are respectively 0.39 and -0.46V for NMOS and PMOS. Transconductance g_m are respectively 0.358mS and 0.198mS for NMOS and PMOS. This results demonstrate that the co-integration of NEMS in the CMOS-FDSOI process has no significant impact on the CMOS electrical performances.

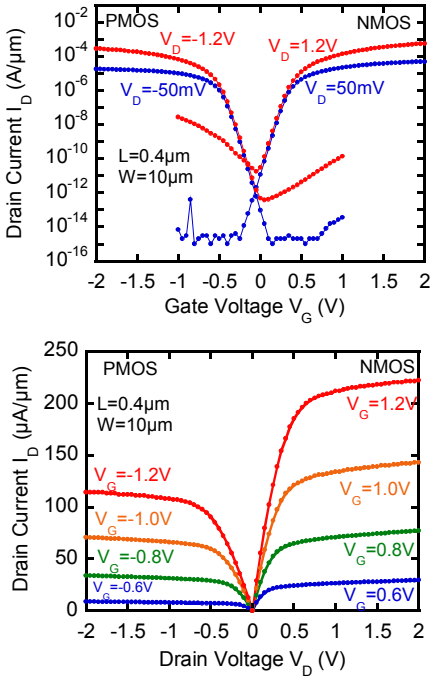

Figure 8: Id(Vg) and Id(Vd) curves of transistor embedded in the NEMS-CMOS co-integration (Si thickness: 40nm, gate length: 400nm, gate width: 10µm)

Figure 9 shows the dynamic response in vacuum of an ultra-scaled 100 MHz NEMS resonator co-integrated with its adjacent CMOS circuit and successfully measured in a direct/homodyne configuration with differential actuation. The device is a single-crystal p-type 40nm thick silicon "crossbeam" with the following dimensions: 100nm wide - 1.2µm long, with two 50nm wide and 100nm long piezoresistive gauges. The electrostatic gap is 60nm wide. The polarization conditions are Vbias=1V, Vin-ac=10mV. The output signal is readout after the buffer with a network analyzer. The s21 magnitude (-45dB at resonance) clearly emerges from the background signal, the phase-shift being between 20° and 100°. These features already allow interfacing this co-integrated device with additional electronics to build a sensor, for example with a PLL (phase-locked loop). In addition, a relatively simple optimization could be implemented in future to improve the gain and the phase behavior in order to build self-oscillating devices. Additional results about the co-integrated CMOS circuit are reported in [8].

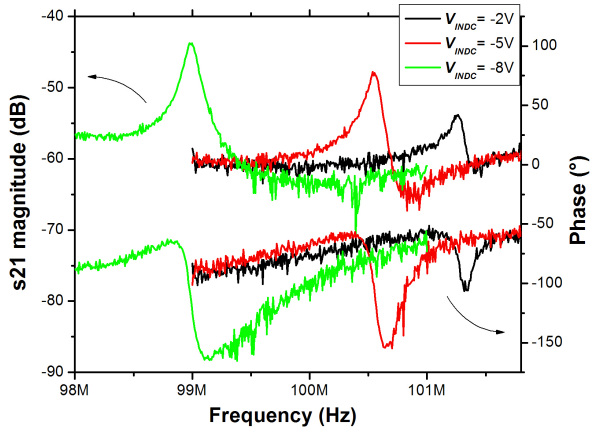

Figure 9: Electrical demonstration (frequency response in terms of resonance curves: gain and phase shift) in vacuum of the direct/homodyne dynamic measurement of an ultra-scaled 100 MHz NEMS device thanks to the co-integration of the CMOS-FDSOI circuit on the same chip.

CONCLUSION

This paper demonstrates the feasibility of top-down ultra-scaled single-crystal Si NEMS resonators (25-40nm thick) operating in the 10-100MHz frequency range and the benefit to co-integrate a simple CMOS readout circuit close to these NEMS in order to extract the signal from background with a simple direct/homodyne read-out. The co-integration process made at the Front-End level of a CMOS technology is totally compatible with the requirements of NEMS processes (release at the end of the process to preserve the suspended structure during MOS and Back-End fabrication) and with the Back-End CMOS oxide layers that do not suffer from the vapor HF etching usually used for MEMS release. In addition, it offers protection-passivation of the NEMS by an oxide layer. Electrical measurement performed on stand-alone NEMS and co-integrated NEMS-CMOS have validated the technology and open the way to implement these co-integrated devices in PLL architecture to build a gas sensor for example. After a few improvements, self-oscillating architectures could also be considered. This approach is also consistent with 3D integration strategies. Furthermore, this work paves the way for NEMS-CMOS arrays.

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CONTACT

*E. Ollier, Tel:+33 4 38 78 57 35, eric.ollier@cea.fr