# POLY-SIGE-BASED CMUT ARRAY WITH HIGH ACOUSTICAL PRESSURE

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## ABSTRACT

Capacitive micromachined ultrasound transducers (CMUT) have the potential to enable 3-D ultrasound imaging. This paper reports a novel manufacturable build-up of a CMUT device which is CMOS compatible. The approach allows high density integration and independent optimization of the CMUT device and the integrated electronics. The CMUT device makes use of polycrystalline silicon-germanium (poly-SiGe) as the structural material, in combination with silicon carbide (SiC) as the dielectric layer to allow high electrical field in the transduction gap. Breakdown voltage of above 500V is demonstrated. Transmit pressure normalized to the surface of the transducer is as high as 580kPa for DC and AC voltages of 340 and 75V, respectively. Initial characterization of pulse-echo measurement is also reported.

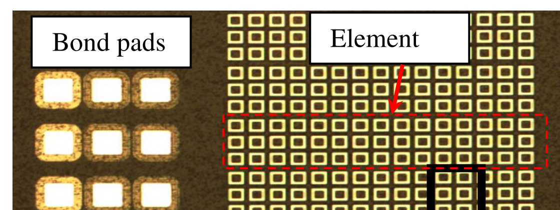
## INTRODUCTION

Three-dimensional ultrasound imaging potentially offers unique attractive features for clinical diagnostic. These new opportunities require, however, monolithic integration of large-scale 2D array CMUT with the underlying electronic circuit (CMOS wafer), to eliminate the impossibly high number of interconnects that would otherwise be required. This integration also offers the benefit of having the driving and readout electronics (pre-amplification/signal processing) very close to the CMUT itself, leading to a better signal-to-noise ratio. This in turn translates to improved device performance, i.e., on sensitivity and bandwidth. Additionally, smaller die size and package are also expected.

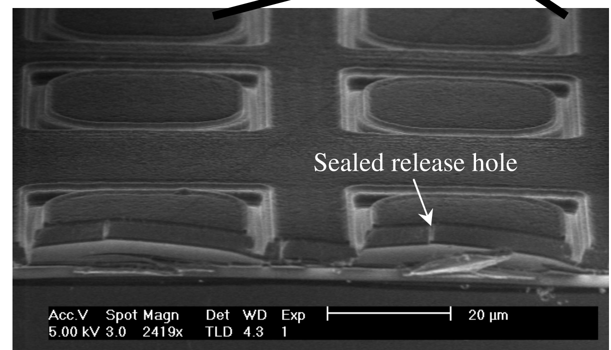
Several approaches have been reported for the integration of CMUT with CMOS [1-5]. As a first approach, the CMUT device is built in the CMOS process itself, taking advantage of a mature process but having the limitation of a fixed layer heights and materials. In a second approach, both parts are made on separate substrates and electrically connected with through-silicon vias (TSV). As this places no temperature or material constraints on the CMUT device, the silicon can therefore be used advantageously as a structural material. The TSV process option can however be expensive due to the number and complexity of processing operations required. Finally, the CMUT device can be processed on top of a CMOS wafer in a "MEMS-last" approach, whereby the post-processing must be performed at relatively low temperatures in order to maintain the IC performance. Until now an aluminum layer was used for the electrode, but this is also known for its creep effect with potential reliability issues in MEMS applications. However, the two last approaches allow full flexibility in controlling the fundamental acoustical device properties.

## TECHNOLOGY CONSIDERATIONS

As the thermal process budget has to be carefully designed to retain the performance and reliability of the CMOS electronics, Poly-SiGe has been selected. Its attractiveness is the relatively low processing temperature which is compatible with CMOS, and its comparable material properties to poly-Si which allows it to be used as a MEMS structural layer [6,7]. Several examples of CMOS-MEMS integration in a "MEMS-last" approach have been reported [8, 9]. Naturally, the employment of Poly-SiGe is extended to the development of a CMUT device displayed in Figure 1.




*a) Microscope picture*

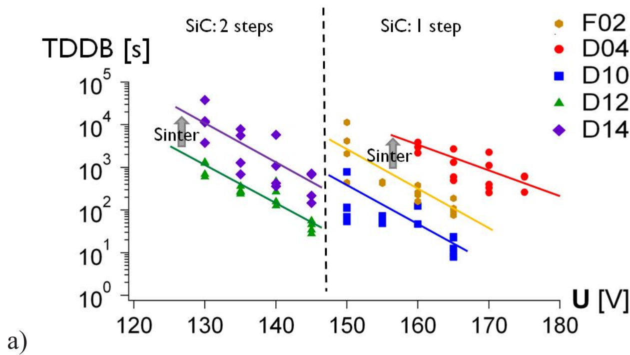



*b) Tilted SEM picture*

*Figure 1: Pictures of CMUT elements with dual thickness membrane.*

A dielectric layer is needed for preventing early voltage breakdown and for operating the device at very high actuation voltages. An amorphous silicon carbide (SiC) layer, deposited by plasma enhanced chemical vapor deposition (PECVD), is used for the first time in CMUT devices for this purpose. The choice of SiC is driven by process manufacturability considerations whereby vapor hydrofluoric acid (HF) is used instead of wet etch solution which could lead to potential stiction issues. The vapor HF step uses oxide as a sacrificial layer but also prevents the utilization of SiN because of residue formation with nitrogen compound. For this high actuation voltage, the SiC layer has been optimized in terms of deposition temperature, single/multi layer deposition and thermal treatment to increase the time dependant electrical breakdown as described in Fig.2.

Finally, attractive process features such as single and dual thickness membranes offer space for design optimization, e.g., membrane displacement closer to a piston-like approach and/or independent optimization of the transmitter/receiver functions. This feature is achieved thanks to the use of an embedded oxide hard mask.




a)

| Sample | SiC | Sinter 30' @ 450 °C |
| --- | --- | --- |
| F02 | 1 step (400 nm @ 350°C) | no |
| D04 | 1 step (400 nm @ 350°C) | yes |
| D12 | 2 steps (2x200nm 350°C ) | no |
| D14 | 2 steps (2x200nm 350°C ) | yes |
| D10 | 1 step (350nm @ 400°C) | yes |

b)

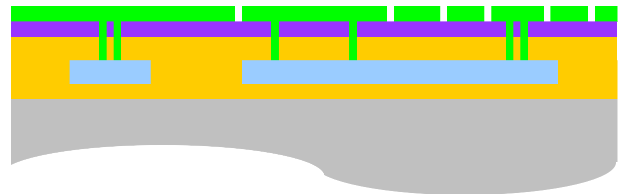
*Figure 2: Optimization of the time dependent dielectric breakdown (TDDB) (a) with process split in SiC deposition in temperature deposition, one or two layer deposition and thermal treatment (b).*

## PROCESS DESCRIPTION

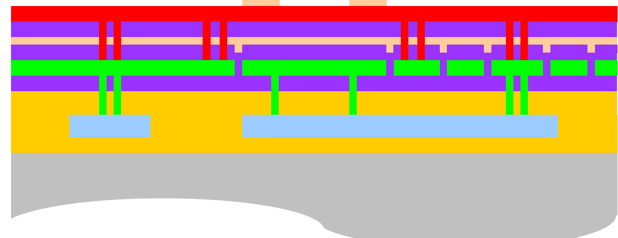
The process flow of the poly-SiGe-based CMUT is described in detail in this section and schematically illustrated with several drawings in Fig.3.

A CMOS wafer is used as the starting substrate, or in the case of the stand-alone version the starting point is a patterned metal layer on a silicon substrate covered with oxide. From this point onward, the process flow is completely identical for both cases. The metallic layer is covered by the deposition of an oxide layer and then planarized by a chemical mechanical polishing (CMP) step to a thickness of 1000nm. A 400nm SiC layer is deposited in order to protect the underlying circuitry electronics from the HF-based release etchant. MEMS vias are opened in both the protective and oxide layers down to the metallic Al layer for electrical connections. A 400nm Poly-SiGe layer is deposited by chemical vapor deposition (CVD) to fill in the MEMS vias and to form the bottom electrode after patterning (Fig.3 (a)).

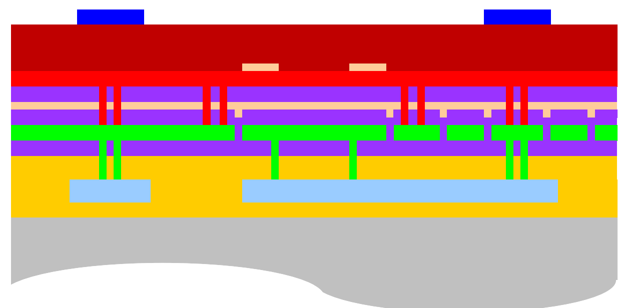
For reasons of symmetry, the actuation gap is defined by a stack consisting of a 200nm oxide layer between two SiC layers of 400nm. In practice, the deposition of the first SiC layer is followed by an oxide deposition which is planarized down to the SiC surface to remove the topography generated by the bottom electrode patterning. A new sacrificial oxide layer which will precisely define the air gap is deposited and followed by the final SiC layer deposition.



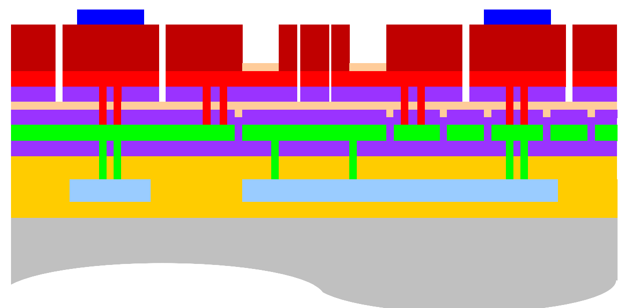
*a) After the definition of the bottom electrode.*



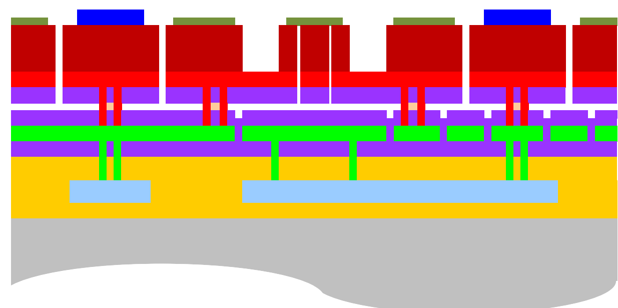
*b) After the definition of the embedded hard mask.*



*c) After the definition of the bond pads.*



*d) After the poly-SiGe etch step.*



*e) Final cross-section.*

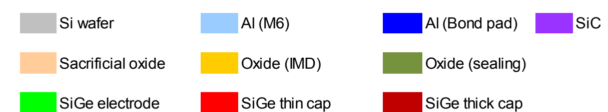



*Figure 3: Conceptual cross-section of the CMUT device made from poly-SiGe and SiC with dual thickness membrane.*

Trenches are provided in the SiC/Oxide/SiC stack for defining the electrical connections and the mechanical anchors. The anchor is not defined by a large area but by an array of lines with fixed widths of 0.8µm, in order to get a planar surface after the subsequent poly-SiGe layer deposition.

The dual thickness membrane is defined by a combination of several deposition steps for improved thickness control, and not by a delayed mask process [10]. To accomplish this, a first layer of poly-SiGe (Poly-SiGe thin cap) is deposited followed by the deposition and patterning of a thin oxide layer. This oxide layer is kept in the area where the structure will be defined only with the thin layer, and acts as a hard mask for the subsequent poly-SiGe etch (Fig.3(b)). The second layer of Poly-SiGe (Poly-Sige thick cap) is deposited to complete the desired membrane thickness. The bond pads for electrical connections are formed before the structural layer patterning on a planar surface (Fig.3(c)).

Release holes, isolation trenches between bond pads and dual thickness membranes (structures with different depths in poly-SiGe) are etched in a single step by a Bosh process thanks to its selectivity towards oxide (Fig.3(d)). A close-up view of the detail of the embedded oxide hard mask after poly-SiGe etch is displayed in Fig.4. During the vapor HF release operation, the oxide inside the cavity is etched to free up the membrane as well as the embedded oxide hard mask.

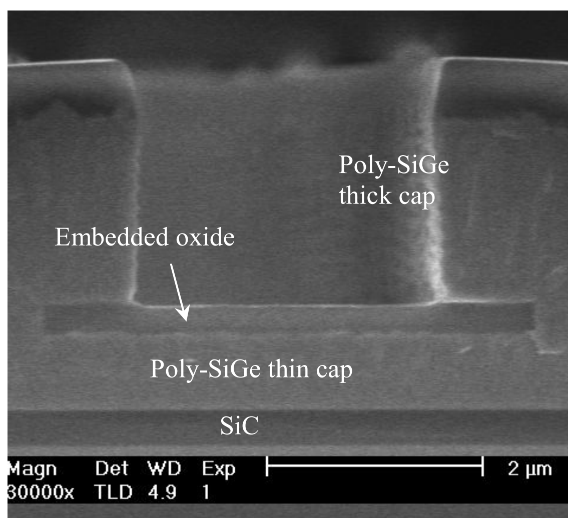
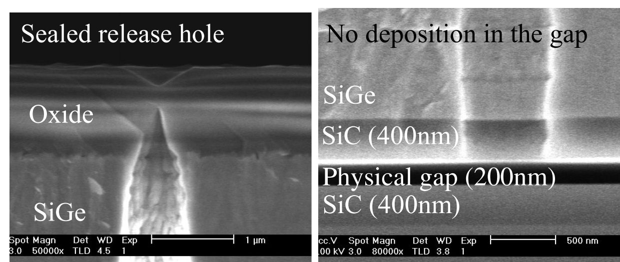



*Figure 4: Poly-SiGe thin cap thickness is controlled by deposition and covered by an embedded oxide before deposition of the poly-SiGe thick cap. The embedded oxide acts as a hard mask during poly-SiGe etch which allows the definition in a single etch step of several depths, thanks to the etch selectivity.*

Release holes are sealed by a PECVD oxide layer without deposition at the bottom of the cavity, hence allowing full membrane displacement. Additional high density plasma (HDP) oxide is deposited above the PECVD oxide layer to avoid any potential crack propagation during membrane actuation. Details of a sealed release hole (bottom and top parts) are displayed in Fig.5. To complete the CMUT device manufacturing, the sealing oxide is patterned and etched above the thin layer of poly-SiGe and also above the bond pads for electrical connections (Fig.3(e)).




*a) Top part of the release hole b) Bottom part of the release hole*
*Figure 5: SEM views of an oxide sealed release hole.*

## CHARACTERIZATION

As a first step, the breakdown voltage of CMUT test structures has been recorded for the actuation gap (composed of an air gap of 200nm and the two layers of 400nm of SiC as described previously). The breakdown starts to occur in the range of 350-450V but some structures survived to voltages of above 500V, as plotted in Fig.6, allowing sufficient margin from the operational voltage. As depicted in Fig.7, the breakdown is located in the bond pad area and it is not an intrinsic characteristic of the CMUT cell. This weakness can be improved by a design modification.

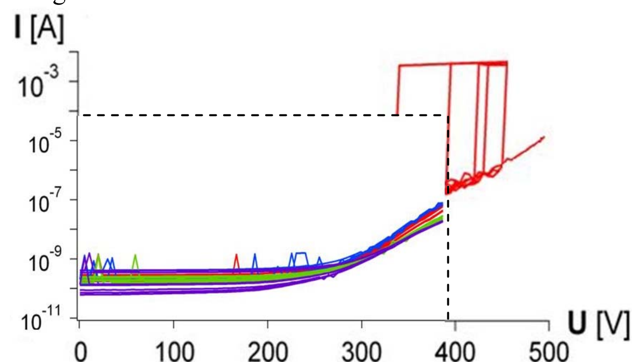



*Figure 6: Graph of the leakage current versus voltage applied on test structures (Two set-ups are needed to cover the voltage range until 500V (superposed graphs)).*

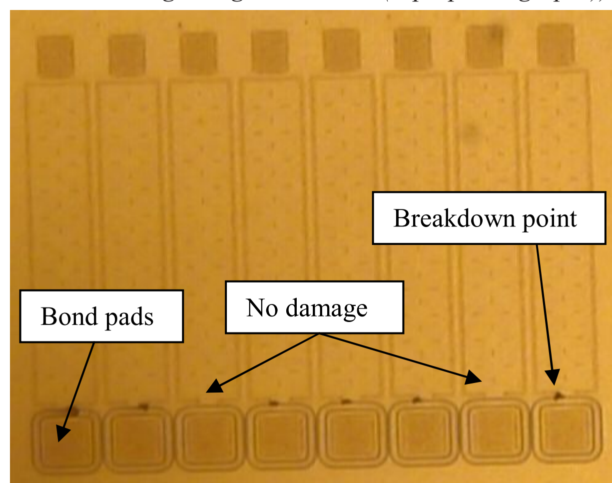



*Figure 7: CMUT test structures after high voltage exposition (500V). Two structures survived to this test.*

Some acoustical tests are also reported as a demonstration of the poly-SiGe CMUT technology. The devices are tested in immersion. Fourier transform of the pulse-echo signal is shown in Fig.8. From this graph, the center frequency and fractional bandwidth for this particular device (dual thickness membrane) are estimated at 2.7MHz and 94%, respectively.

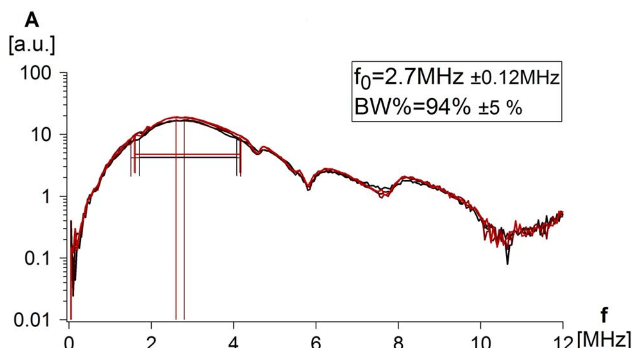



*Figure 8: Fourier transform of the pulse-echo of a CMUT device with dual thickness. Resonance frequency is 2.7MHz and fractional bandwidth is 94%.*

The peak-to-peak transmitted pressure was measured at a distance of 4.4mm for a 2D CMUT array (single thickness membrane) using a calibrated hydrophone. The pressure was then normalized to the surface of the transducer by taking into account diffraction and attenuation losses. The graph in Fig.9 records the acoustical power versus voltage with a maximal value around 580kPa.

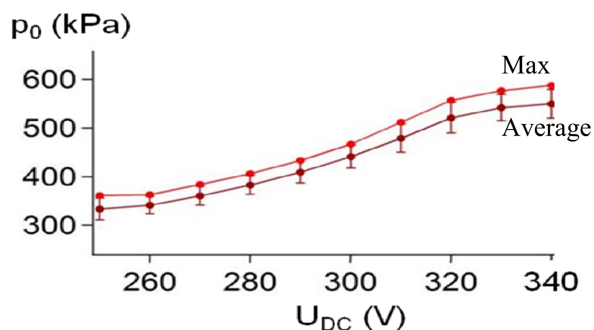



*Figure 9: Normalized acoustical pressure at the transducer surface versus bipolar DC voltage superposed with AC voltage (75V).*

## CONCLUSION

In this paper we demonstrate the potential of a poly-SiGe-based flow for CMUT applications. Initial characterization of the main CMUT parameters shows comparable values to data reported in the literature. In addition, high breakdown voltage and high acoustic pressure are also achieved.

Future work includes design, fabrication and characterization of a 2D array with monolithically integration of CMUT and CMOS to demonstrate focusing and beam forming functions.

## ACKNOWLEDGEMENTS

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