LOW-COST CMOS COMPATIBLE SINTERED POROUS SILICON TECHNIQUE FOR MICROBOLOMETER MANUFACTURING

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ABSTRACT

This paper reports about the development of a low-cost, CMOS compatible process technology to create thermally insulated pixel regions for integrated microbolometers. The enabling technology is based on a modified sintered porous silicon (sPS) technique.

An array of 280 x 240 thermally isolated pixels with lateral dimensions of 30 x 30 μm^2 and epitaxial silicon (Si) thickness down to 500 nm is presented. In the final design the pixel is suspended by silicon dioxide (SiO_2) arms. The design and fabrication process is described and mechanical deformation properties subtracted from profilometer images are presented.

INTRODUCTION

At present, integrated security and safety solutions are a major driver of the automotive industry, causing a strong demand for low-cost, robust night-vision systems. Night-vision systems employ Infrared long-wavelengths (LWIR) detectors which are classified in the two main categories (i) photon and (ii) thermal detectors [1]. In the scheme of the International Commission on Illumination (CIE), LWIR is one subclass of the IR-C band (λ=3 – 1000 μm). It is defined as thermal imaging in the spectral region ranging from 8 to 15 μm wavelengths [2]. The reason why the LWIR spectral region is of high interest for night-vision is, that, at the body temperature of humans and most animals, the spectral radiation emittance has its peak at approximately λ=9.6 μm [3]. Additionally, the atmospheric translucence at this wavelength is very high, meaning that less radiation power is absorbed during the atmospheric transmittance, hence, this enables passive infrared night-vision. Due to the cryogenic operating temperatures required, photon detectors are unsuitable for use in low-cost devices. Therefore, uncooled microbolometers are highly desired as thermal detector arrays [4].

The operating principle of a microbolometer is as follows: Infrared radiation is absorbed within a layer, causing the bolometer to heat up. The temperature increase is measured by a thermometric device. This device should be thermally insulated from the substrate and from other pixels. In the classic design [5] the thermometric device is a temperature depended resistive layer, having a thickness of 50 nm. Due to its high temperature coefficient (TCR), Vanadium-oxide is the material of choice. The problem with Vanadium-oxide is, that it is unsuitable for CMOS process lines, hence, it is expensive to fabricate such bolometers. Therefore, standard CMOS fabrication processes and CMOS compatible materials are preferred. In those approaches p-n junction diodes are the thermometric devices [6].

The fabrication technology outlined in this paper is based on a process that is fully CMOS compatible. Chip-level devices have already been fabricated [7].

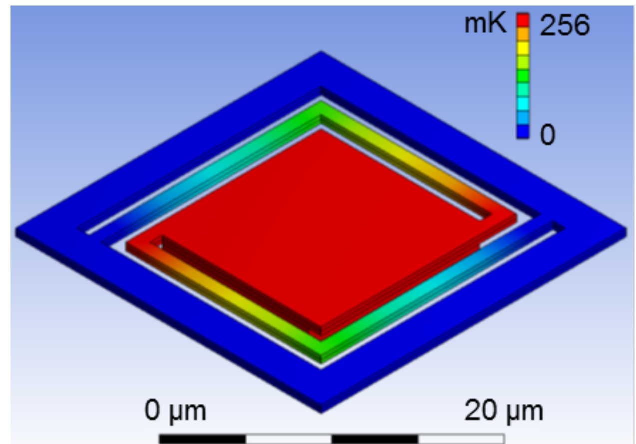

Figure 1: Image taken from thermal FEM simulations (ANSYS). The temperature distribution of one 1 μm arm width, suspended pixel.

Furthermore, this process does not need expensive silicon-on-insulator (SOI) wafer substrates and avoids surface micromachining.

DESIGN

The design was based on mechanical and thermal simulations, using the ANSYS engineering simulation suite. An image showing the temperature distribution of one pixel is shown in Fig. 1. The bolometer pixel occupies an area of 30 x 30 μm^2 and the array under investigation had 280 x 240 pixels. By varying its width and length and by using one or two supporting arms, various pixel structures have been fabricated to investigate its mechanical stability (Fig. 4). Based on the simulation results the best trade-off in mechanical stability and thermal insulation was a pixel structure having two supporting arms in the 'around one corner design' with width of 1 μm (Fig. 4a).

The effective thermal resistance consists of the thermal resistances of the supporting arms, of the cavity underneath and of the trenches at the sides of the membrane. Thermal resistance is computed as

$$R_{th} = \frac{l}{R_{\lambda} * h * w} \quad (1)$$

with R_{th} the thermal resistance in units of K/W, l the length of the thermal conductor, R_{λ} the specific thermal conductivity in W/mK, h the height of the thermal conductor and w the width of the thermal conductor.

The thermal capacitance is dependent on the pixel membrane mass. The heat capacity is defined as

$$C_{th} = V * \rho * c \quad (2)$$

with C_{th} the heat capacity, V the volume of the membrane, ρ the density of the material and c the specific heat

Table 1: Literature values of thermal conductivity and heat capacity of CMOS compatible materials [8, 9]

Material	Specific Thermal Conductivity [W/(m*W)]	Specific Heat Capacity [J/(kg*K)]
Si	156	713
SiO_2	1.25	1052
Si_3N_4	13.79	680
Ti	21.9	523
Al	237	898.7

capacity of the material. The thermal time constant can be calculated by multiplying equations (1) and (2).

$$t_{th} = R_{th} * C_{th} \quad (3)$$

Literature data for the CMOS compatible materials Si, Silicon dioxide (SiO_2), Silicon nitride (Si_3N_4), Aluminum (Al) and Titanium (Ti) are shown in Table 1. The specific thermal resistance of air at ambient conditions is 24 mW/mK [10]. The specific thermal resistance of air at vacuum conditions (298.15K and air pressure of 10^{-2} mbar) was calculated from the diatomic gas theory to be 94.4 µW/mK [11].

The temperature change can be calculated by using an equivalent RC circuit:

$$\Delta T = A * R_{Tth} * (1 - e^{\frac{-t}{t_{th}}}) \quad (4)$$

with A the absorbed power, R_{Tth} the total thermal resistance and t the time. Convection losses and losses due to radiation are not considered.

Using a pixel membrane of 2 µm thick Si, with 600 nm SiO_2 on top, suspension arms of 600 nm thickness with a Ti core of 100 nm thickness, the thermal time constant was calculated to be 15 ms. For a radiation power of 65 nW, the membrane temperature increase was calculated to be 125 mK. Based on mechanical FEM simulations of this structure, the mechanical deformation of the membrane is 20 nm, hence, it can be neglected.

FABRICATION

The fabrication process is illustrated in Fig. 2. Based on previous work the standard Chipfilm™ process [7] was downsized to pixel level. This was done using a ratio ¼ between balk and membrane regions. The process started with the local implantation of n-type regions in a p-type Si substrate. The n-type regions form the balks that later attach to the membrane arms. The formation of a double porous Si layer, consisting of a coarse and a fine porous layer, was achieved through electrochemical etching of the p-type regions. A thermal rearrangement process transformed the fine porous layer into a solid silicon layer with self-contained nano cavities, so-called sintered porous silicon (sPS). Between this sPS layer and the substrate, a continuous cavity was created from the rearrangement of the coarse porous layer [12].

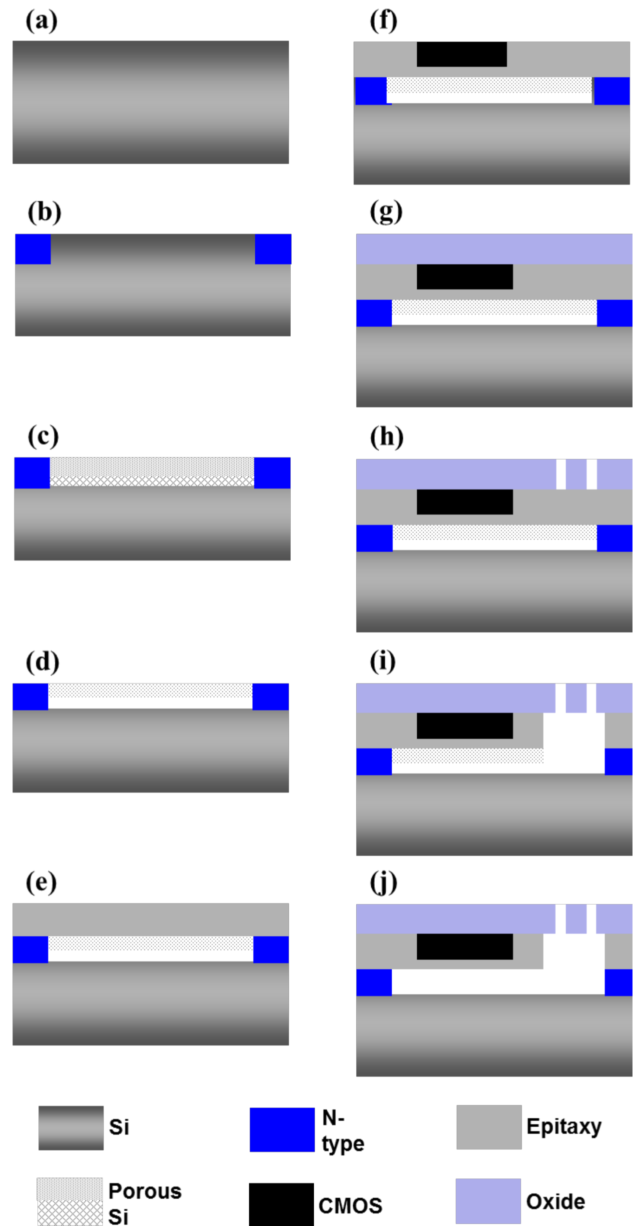

Figure 2: Cross-sectional illustration of the sPS process. (a) P-type Si start-wafer. (b) N-implantation for balk definition. (c) After electrochemical etching, a coarse and a fine porous layer are formed. (d) After rearrangement, the coarse porous Si layer is transferred and a cavity is formed. (e) Epitaxial layer deposition. (f) CMOS device implementation. (g) After oxidation. (h) RIE oxide etch. (i) Modified DRIE, the Si under the oxide is removed. (j) The porous Si is etched away through ClF_3

The cavity height was 500 nm and the thickness of the sPS layer was 1.3µm.

Since the surface of the fine porous layer rearranged into a closed silicon surface during the annealing, a high quality epitaxial Si layer can be deposited onto the wafer. Different thicknesses of epitaxial layers have been explored, reaching down to a deposited thickness of 500 nm (Fig. 3d).

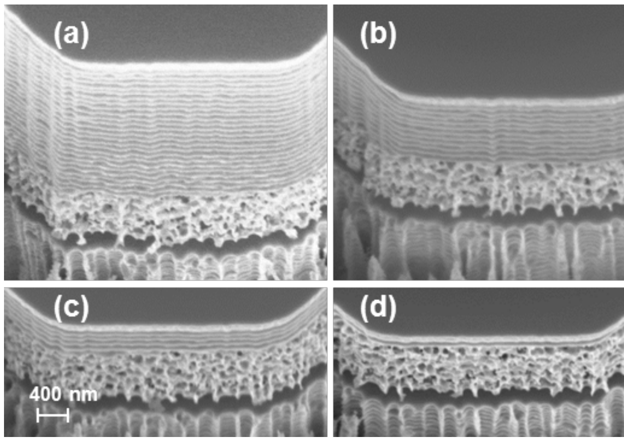

Figure 3: SEM 20° tilted view with different epitaxial thicknesses. (a) 4µm (b) 2µm (c) 1µm (d) 500nm epitaxial Si. Underneath the epitaxial layers porous Si layers and cavities are visible.

The epitaxial layer was then ready for CMOS device implementation. With focus on microbolometer applications p-n junctions can been achieved through n-type implantation in the doped p-type epitaxial layer.

After epitaxy a SiO_2 layer was deposited. The oxide was trenched using a standard reactive ion etching (RIE) technique. This was followed by a modified, strong isotropic Si deep reactive ion etching (DRIE) process (Fig. 5b). This process allowed for etching the Si underneath the oxide, hence, to suspend the membranes merely through oxide arms. Based on the low thermal conductivity of SiO_2, this enables maximum thermal insulation of the membrane and maximum temperature increase in the device region.

The last step was to remove the porous Si layer underneath the membrane by an isotropic ClF_3 etching process. After that step the total cavity height was increased to 1.8 µm (Fig. 5a).

RESULTS

A typical microbolometer pixel structure is shown in Fig. 4a. The middle part is the membrane in which CMOS devices can be implemented. The membrane is supported by two arms in an "around one corner" design. This design allows maximum thermal insulation from the substrate and good mechanical stability. Different designs have been realized. A one arm suspended structure and two arm structures with different arm widths and beam designs are shown in Fig. 4a-d. For the structure shown in Fig. 4a, having an epitaxial layer varying from 4 µm to 500 nm in thicknesses, the membrane sagging of 20 nm was insignificantly small. As visible from optical profilometer images, a step between the balks and the cavity regions can be seen (Fig. 6). This is in good agreement with mechanical ANSYS simulations.

After the deposition of 600 nm SiO_2, for all structures and epitaxial thicknesses, a considerable sagging of the pixel membrane could be observed, shown in Table 2. As assumed, the mechanical deformations of the pixel through the oxide layer were minimal for thick epitaxial layers and became more pronounced with decreasing epitaxial layer thickness. The deformation ratio between

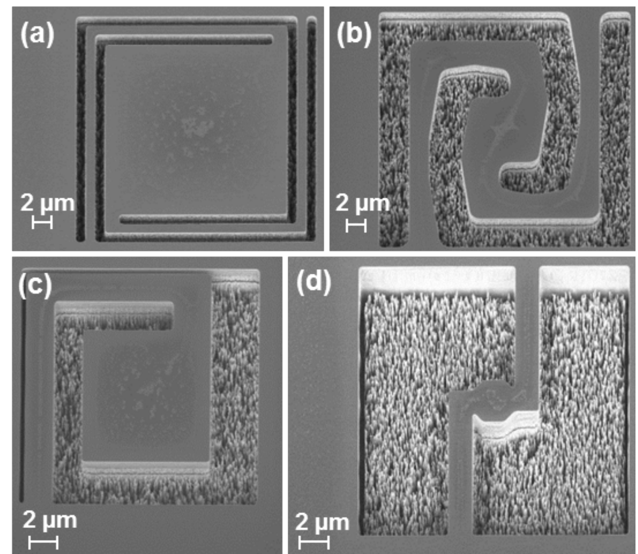

Figure 4: SEM 20° tilted. (a) The classical pixel design, two 1µm width arms hold the membrane. (b) A two concave arm design. (c) A one-arm suspension structure. (d) Bonbon structure, in this image Si grass is clearly visible.

structures that have been oxidized and structures without and with oxide deposition shows that, for an epitaxial layer thickness of 1 µm a maximum deformation ratio occurs. But, due to the cavity height of 1.8 µm, the total sagging after oxide deposition was noncritical in terms of thermal shunting.

The existence of Si grass on the substrate, at the trenched regions is visible in Fig. 4d. This is due to the ion etch through the sPS layer underneath the epitaxial layer. Note, that this result might be of interest as an alternative approach for Si grass fabrication. However, in this work the focus was on the membrane structure formation. Therefore, the Si grass was etched away during a later applied ClF_3 process. With a maximum underetch of 2.2 µm the modified DRIE process showed consistently good results (Fig. 5b). It allows for setting the oxide underetch to 500 nm, hence, to allow for a complete underetch of the oxide arms.

The removal of sPS through ClF_3 was shown to be feasible (Fig. 5c). It was found that this process is mainly controlled by the reaction time. Thereby, a reaction time of 20 minutes gave an optimal result. Using this etch time, the sPS removal was consistent and the effect on the solid Si was minimal.

Table 2: Difference of balk to pixel, without and with 600nm oxide. Data taken after trenching, modified DRIE and ClF_3 processes. All data extracted through optical profilometry.

1 µm arms width around one corner design			
Epitaxial layer thickness [µm]	**Difference balk/ pixel before SiO_2 deposition [nm]**	**Difference balk/ pixel after SiO_2 deposition [nm]**	**Ratio: SiO_2 deposition/ No SiO_2 deposition**
4	19	90	4.7
2	17	160	9.4
1	13	230	17.7
0.5	19	290	15.3

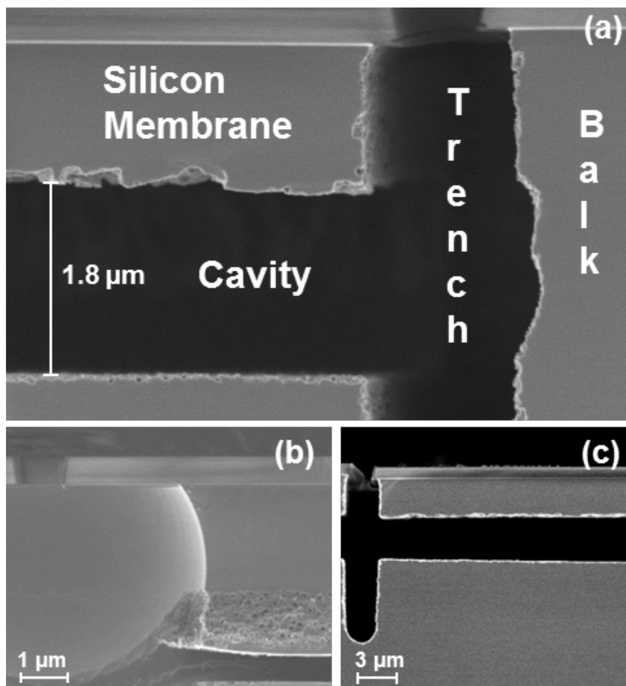

Figure 5: Cross-sectional SEM images. (a) The silicon membrane of one pixel with the cavity and the trench region visible. The after ClF_3 process cavity height is 1.8 µm. (b) Illustration of the under-oxide DRIE etch. The oxide is under-etched by a width of 2.2 µm. (c) One pixel membrane after ClF_3 process. The Si grass and the porous Si are vanished.

CONCLUSIONS

A sPS MEMS process was demonstrated and a pixel array of thermally insulated areas has been fabricated. It has been shown that the observed mechanical deformations are small, hence the illustrated process is suitable for microbolometer manufacturing. This MEMS process enables the cost effective fabrication of thermally insulated pixel arrays. Compared to previous work [6] it avoids surface micromachining processes and the use of expensive SOI wafers. Furthermore, the possibility to create thin, merely oxide suspended structures for the purpose of optimum thermal insulation may supersede present SOI techniques for microbolometer manufacturing.

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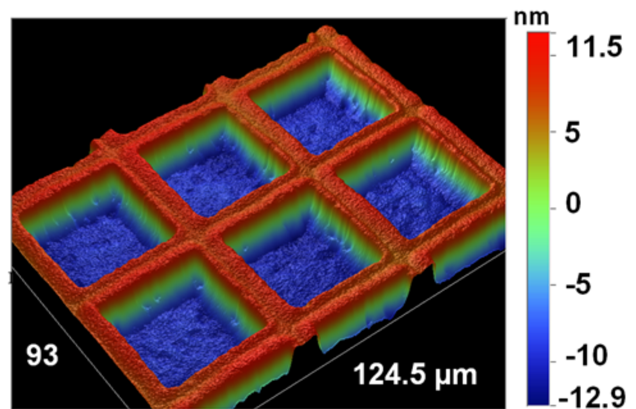

Figure 6: An optical profilometer image of untrenched membranes. A step of 20nm between the balks and the membranes is noticeable.

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