BELOW-IC POST-CMOS INTEGRATION OF THICK MEMS ON A THIN-SOI PLATFORM USING EMBEDDED INTERCONNECTS

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ABSTRACT

This paper describes a new post-CMOS technology for co-integrating thick (> 50 µm) high aspect ratio MEMS beneath a thin-SOI (1.5 µm) CMOS platform, in the low resistivity SOI-handle wafer. MEMS post-processing requires just one photomask step. The low resistance (~ 40 Ω) electrical interconnection between CMOS and MEMS is realized using vertically embedded polysilicon interconnects, formed during standard CMOS processing. Electrical isolation achieved using isolation trenches shows a small leakage current (< 10^{-12} A) and a typical isolation resistance better than 10^{12} Ω. Measurements indicate that backside micromachining adjacently-beneath integrated transistors does not affect their characteristics. This 3D integration technology can be applied for fabricating a variety of MEMS devices like capacitive inertial sensors and electrostatic actuators requiring thick, high aspect ratio microstructures with high density electrical interconnection.

INTRODUCTION

Silicon-on-insulator (SOI) technology is an attractive platform for manufacturing CMOS and MEMS [1-4]. Several interleaved- and post-CMOS technologies have been reported for laterally co-integrating CMOS with MEMS-based capacitive sensors and electrostatic actuators on thick-SOI (8 µm - 50 µm) platforms [1-3]. Thick, high aspect ratio (HAR) microstructures made of single crystal silicon, a mechanically superior material, enable high performance sensing and actuation. For instance, thick HAR in-plane inertial sensors demonstrate enhanced sense capacitance and mode separation, and reduced cross-axis sensitivity. Furthermore, the on-chip realization of short high density electrical interconnections between CMOS and MEMS significantly minimizes the parasitic capacitances, encountered (~ 1 pF) in conventional wire-bonded implementations. However, establishing CMOS-MEMS electrical interconnections and isolation on thick-SOI platform represents a bottleneck and a pressing technology issue [1-3]. This is because in SOI technology, trenches are usually etched around the MEMS periphery for electrical isolation, making electrical interconnection between the CMOS and MEMS regions difficult. Three CMOS-compatible solutions currently reported in literature addressing electrical interconnection and isolation on SOI platforms, employ– dielectric-polysilicon filled deep-trench isolation combined with embedded polysilicon interconnection [1], aluminum microbridge inter-connection with embedded polymer pillar [2] and standard metal interconnection in combination with self-assembled stiction-cantilever electrical contact [3]. While the abovementioned methods do solve the problem, they involve complicated processing. Moreover the third method [3] also raises reliability concerns due to the use of stiction-bar for electrical connection.

In this study, we present a new and simple 3D solution, compatible with standard CMOS processing, for co-integrating thin-SOI CMOS and thick-SOI MEMS using vertically embedded polysilicon interconnects in combination with standard metal interconnection, and by electrically isolating active CMOS and MEMS regions using isolation trenches.

BELOW-IC MEMS INTEGRATION

In this work, NXP Semiconductors' advanced Bipolar-CMOS-DMOS (A-BCD) SOI technology [4] was chosen as the CMOS-MEMS integration platform, as it provides mixed-signal, high voltage, memory (EEPROM) and bus interconnection capabilities. Besides, A-BCD SOI technology is widely used in automotive applications, which will benefit from MEMS integration. However in this SOI platform, the available device silicon layer thickness is just 1.5 µm, which prevents monolithic implementation of high performance inertial MEMS. Therefore to obtain relatively thick structural layer, it is proposed to utilize the bulk silicon available underneath the SOI-CMOS layer, in the low resistivity SOI-handle wafer, as shown in *Fig. 1*. The SOI-handle wafer is usually meant for support and handling purposes, and is seldom used for functional device integration. Our solution is to etch HAR thick MEMS on the handle silicon wafer using deep reactive ion etching (DRIE) process and later release them by either sacrificially etching the buried oxide (BOX) layer in a HF based etchant, or using the charging-dependent footing/notching effect occurring at the oxide-silicon interface in SOI substrates.

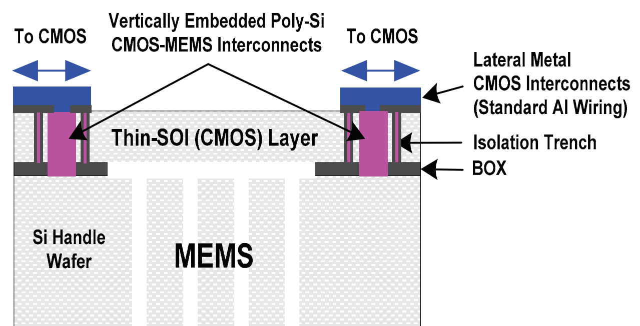

Figure 1: Illustration of below-IC MEMS integration concept.

The electrical interconnection between the thin-SOI CMOS and the thick-SOI MEMS is achieved by modifying and using the already available polysilicon substrate contact as the CMOS-MEMS interconnect [5] in

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combination with standard metal interconnection (*Fig. 1*). The polysilicon interconnect is formed during standard SOI-CMOS processing as follows. At first a shallow trench is etched into the device silicon layer, through the BOX, stopping on the handle silicon layer. Now the trench is refilled with polysilicon using an auto-doping process and annealed. Later excess polysilicon is removed, followed by trench-cap formation using the LOCOS process. Electrical isolation of individual device components and different active regions is achieved simultaneously, alongside the interconnection process. This simple means of 3D electrical interconnection overcomes the process complexity encountered in several other SOI CMOS-MEMS platforms discussed previously. In this way, the MEMS can be post-CMOS processed on the backside of the SOI-CMOS wafer at low temperatures (≤ 300 °C).

However, for functional MEMS integration an optimal structural layer thickness and capacitive gap-size are required. This entirely depends on the achievable AR of the deep reactive ion etching (DRIE) process being used for MEMS definition, which is typically around 1:20 (width:depth). Moreover, the DRIE processing cost increases proportionally with the etch depth. For this reason, the SOI-handle wafer must be thinned down to a reasonable MEMS structural layer thickness in the range of 50 µm - 100 µm. This operation necessitates the use of a carrier wafer for support and robust handling during subsequent processing and is discussed below.

FABRICATION PROCESS

The post-CMOS MEMS processing steps performed on downsized (100 mm) thin-SOI substrate (*Fig. 2a*) are illustrated in *Fig. 2*. After completion of CMOS fabrication and metallization (*Fig. 2a*), the SOI wafer is flipped and adhesive-bonded to an alkaline-free glass carrier wafer (*Fig. 2b*). Adhesive bonding is performed at room temperature using a transparent UV-curable glue [6] by simple spin-processing, without the need for any critical alignment except for the wafer flats. The UV-glue accommodates for the presence of any topography existing on the SOI-CMOS wafer by reflowing during spin processing. A uniform thickness in the range of 5 µm - 12 µm can be obtained for the glue layer upon UV-curing, depending on the applied spin-speed. It is worth mentioning that the maximum allowable post-processing temperature after UV-glue bonding is limited to 300 °C, to avoid decomposition (~ 320 °C) of the glue material. The bonded wafer is then thinned and polished from the backside to the required thickness (*Fig. 2c*). Lithography can easily be performed in a contact aligner or a wafer stepper using front-to-back wafer alignment after adhesive bonding, as both the glue layer and glass are optically transparent. Subsequently, an optional ohmic implantation and laser annealing process can be performed before sputtering a 0.6 µm - 1.4 µm thick Al-1%Si metal layer at 50 °C, which serves as the backside bond pad and DRIE hard-mask layers (*Fig. 2d*). Over this layer, an optional 1 µm thick low temperature PECVD oxide is deposited at 300 °C (*Fig. 2d*), which protects the metal layer and serves as the top DRIE hard-mask. Next, the MEMS structure and backside bond pads are lithographically patterned and the underlying masking layers are etched (*Fig. 2e*), landing on the silicon surface. MEMS and bond pad pillars are etched on the silicon handle layer using Bosch DRIE process [7] (*Fig. 2f*). The fluorocarbon sidewall polymer resulting from the DRIE process is removed in-situ by oxygen plasma ashing. Finally the MEMS are released by sacrificially etching the BOX layer in an HF based etchant (*Fig. 2g*). Alternatively, footing/notching release can be employed. Complex high density CMOS-MEMS electrical interconnections can be accomplished on the front wafer side and key I/O bond pads can be accessed from the backside (*Fig. 2g*).

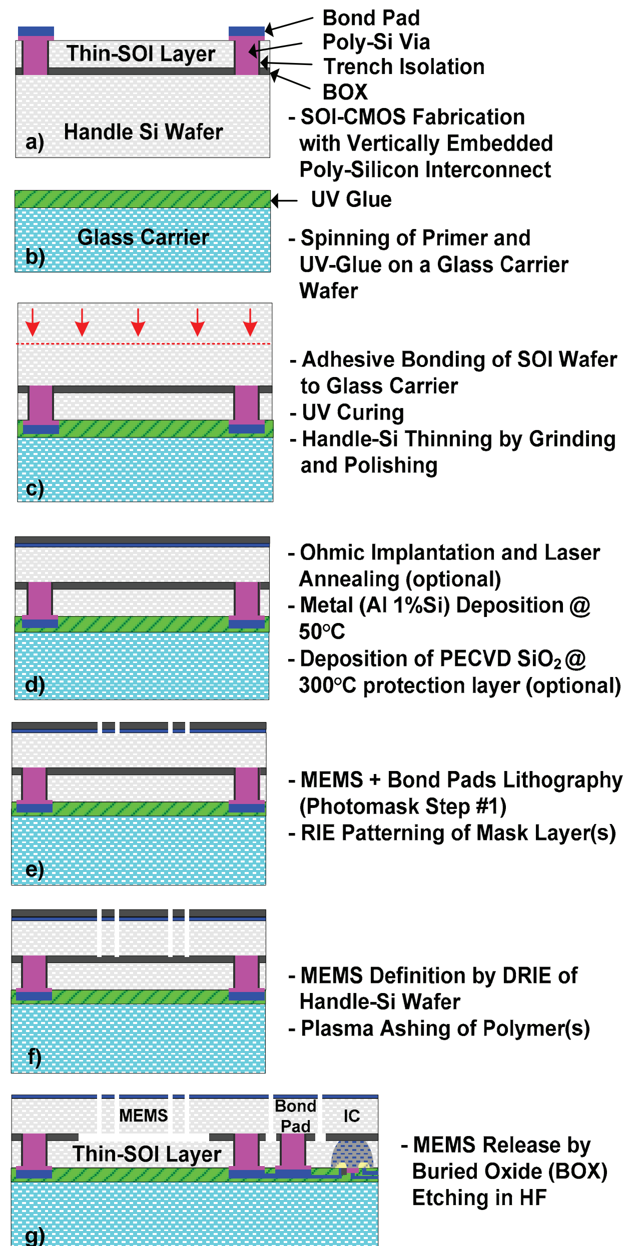

Figure 2: Post-CMOS MEMS process sequence.

RESULTS AND DISCUSSIONS

A thin-SOI device-level module (*Fig. 3a*) consisting of embedded polysilicon interconnects and various active and passive devices was prepared in NXP's A-BCD technology. In this module, lateral metal interconnections between MEMS and CMOS were not implemented.

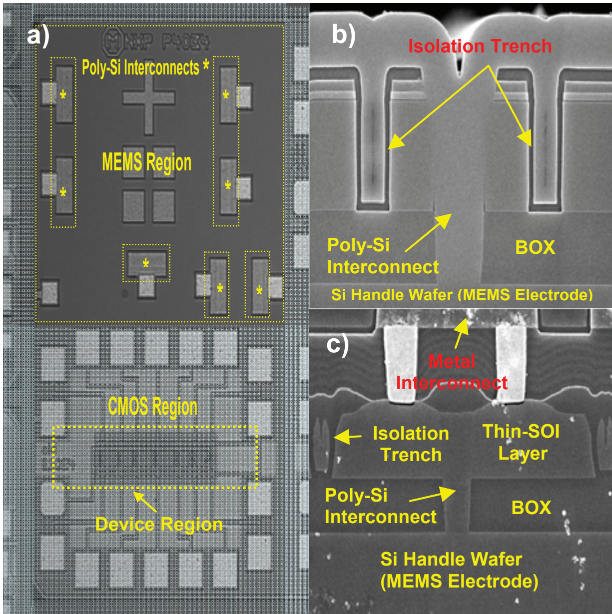

Figure 3: (a)– Photo of a thin-SOI device test module consisting of embedded poly-Si interconnects in the MEMS region, surrounded by CMOS region; (b & c)– SEM cross-sectional images of an embedded interconnect after poly-Si trench re-fill and annealing process (b), and after completion of metallization (c).

Experiments were performed to determine– the electrical resistance of the polysilicon interconnects, the electrical characteristics of the isolation trenches, and the CMOS compatibility of the backside HAR DRIE micromachining process. Two cross-sectional SEM images of the fabricated embedded polysilicon CMOS-MEMS interconnect are shown in *Figs. 3b & 3c*. The metal bond pad can also be seen on the top in *Fig. 3c*. The electrical resistance between two adjacent polysilicon interconnects was measured on a 300 µm thick SOI-CMOS substrate and is presented in *Fig. 4*.

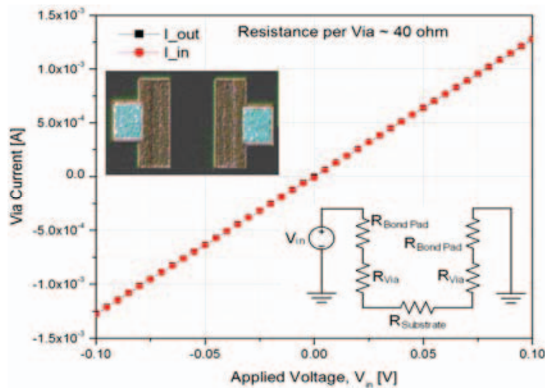

Figure 4: Measured I-V characteristic of the embedded polysilicon interconnect.

The I-V measurement indicates a linear resistance behavior and a typical resistance value of ~ 40 Ω per interconnect. This value is sufficiently low ohmic for reading out most MEMS inertial sensors and electrostatic actuators. Another important electrical property is the isolation characteristics between the individual electrically active MEMS and CMOS regions in the device silicon layer, across their respective isolation trenches, refer *Fig. 5*. The leakage measurement performed on a sample (*Fig. 5*) indicates a small leakage current well below the 10^{-12} A range and a typical isolation resistance better than 10^{12} Ω. Electrical breakdown of the isolation trenches was not observed until 20 V, the highest applied voltage, as expected. The above values guarantee a small leakage and suggest excellent isolation characteristics. The electrical isolation between a released MEMS device and the thin-SOI layer is determined by the gap in-between or the BOX thickness, depending on the release method employed, and the potential difference applied between them.

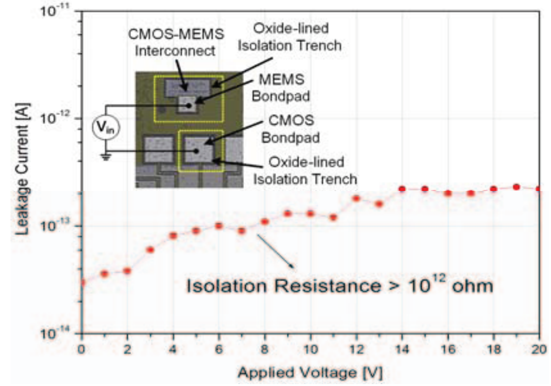

Figure 5: Measured I-V isolation characteristics across the oxide-trench isolated MEMS and CMOS bond pads.

The result of void-less adhesive (UV-glue) wafer bonding is presented in *Fig. 6a,* as in *Fig. 2c*. The CMOS compatibility of this low-temperature process step has already been established elsewhere [6]. The cross-sectional SEM image of a glue-bonded and backside-thinned SOI-CMOS wafer is shown in *Fig. 6b*.

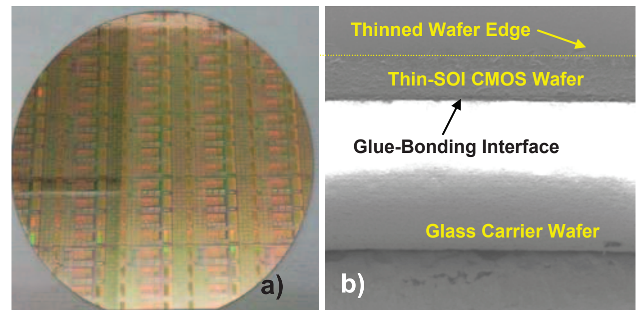

Figure 6: Photo of void-free glue bonded thin-SOI wafer viewed through the glass wafer (a, left); SEM cross-sectional image of a glue-bonded and thinned SOI-CMOS wafer (b, right).

Plasma-charging is known to alter or disrupt CMOS functionality by injecting charges into the gate oxide. In the presented process, the front side of the wafer and thus the gate oxide is not directly exposed to plasma processing. The DRIE backside micromachining process though uses high density inductively coupled plasma (ICP) processing and might introduce trapped charges into the BOX layer from the backside. This potentially might influence the CMOS functionality and needs verification. So a simple experiment was conducted on a thin-SOI CMOS wafer, without bonding, to determine the influence of backside ICP-DRIE micromachining on various device characteristics. Large MEMS cavities were etched into the handle layer of the SOI-CMOS wafer alongside high

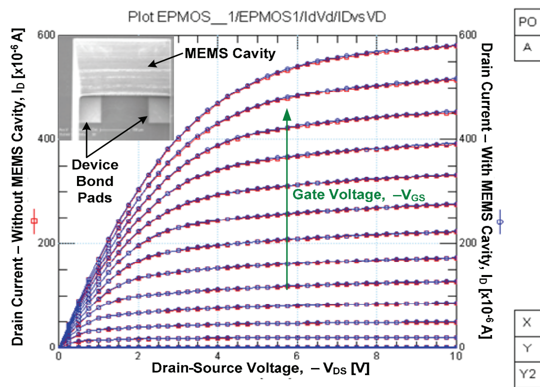

Figure 7: Measured output (I_D-V_{DS}) characteristics of an EPMOS transistor (W/L = 20/3.5), without (reference device) and with the presence of MEMS cavity located adjacently beneath, 30µm away (inset). The gate voltage (V_{GS}) was swept from 0 V to -4 V and the back gate was fixed at low potential by grounding the chuck.

aspect ratio microstructures, representing two different scenarios. The MEMS cavities were located directly-beneath the CMOS device region making the devices fully suspended and also adjacently-beneath the CMOS devices, located at varying distances, d_i = 30 µm, 60 µm and 100 µm, respectively. Measurements were performed on an extended drain P-MOSFET (W/L=20/3.5) shown in *Fig. 3a*, before and after DRIE micromachining, and with and without the backside MEMS cavities. As expected, the threshold voltage and output characteristics of a reference EPMOSFET device remained unaltered after DRIE micromachining, when no backside MEMS cavities were etched in its vicinity. Device measurements performed on another EPMOSFET device confirmed that placing MEMS cavities 30 µm adjacently-beneath the device, already does not affect its threshold voltage or the output characteristics refer *Fig. 7*. This trend was also observed for other tested passive thin-SOI devices.

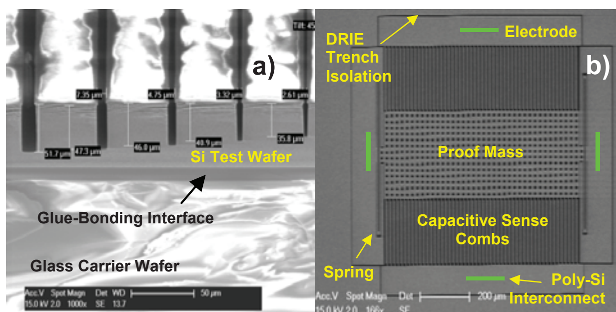

Figure 8: Trenches micromachined on a glue-bonded silicon wafer stack using the Bosch DRIE process (a), and implementation of a ±250g MEMS accelerometer on a 50µm thick-SOI layer (b). The intended poly-Si interconnect locations are indicated in green.

The HAR DRIE micromachining process calibrated for deep anisotropic silicon etching [7] was applied for trench etching in a glue-bonded silicon test wafer, with additional cooling steps. The AR-dependent trench etching results are presented in *Fig. 8a*, showing the possibility of performing DRIE on such wafers. Similar results were obtained for a glue-bonded thin-SOI wafer. This was also confirmed by a comparative FEM analysis of the thermal distribution profile on glue-bonded silicon and thin-SOI wafers due to wafer cooling. Several automotive range in-plane MEMS accelerometer structures and *Z*-axis dual-mass decoupled MEMS gyroscope structures were micromachined on a 50 µm thick-SOI layer. An example micromachining result from a ±250g accelerometer is presented in *Fig. 8b.* In this post-CMOS MEMS technology, the electrical I/O bond pads need to be accessed from the backside due to the presence of a glass carrier wafer on the front side of the thin-SOI CMOS wafer.

CONCLUSIONS

A novel post-CMOS technology for co-integrating thick (> 50 µm) high aspect ratio MEMS in the SOI-handle wafer beneath a thin-SOI (1.5 µm) CMOS platform, using one photomask, was presented. Low resistance (~ 40 Ω) vertically embedded polysilicon interconnects are formed during standard CMOS processing for CMOS-MEMS electrical interconnection, in combination with standard metal interconnection. Electrical isolation having a resistance better than 10^{12} Ω is achieved using isolation trenches, in-between CMOS and MEMS. No electrical degradation was observed on integrated devices, when micromachining adjacently-beneath on the backside. This 3D integration technology is suitable for fabricating a range of capacitive and electrostatic MEMS requiring thick, high aspect ratio microstructures with high density interconnections.

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REFERENCES

[1] T.J. Brosnihan, J.M. Bustillo, A.P. Pisano and R.T. Howe, Embedded interconnect and electrical isolation for high-aspect-ratio, SOI inertial instruments, *Proc. Transducers'97*, pp. 637-640, 1997.

[2] H. Takao, T. Ichikawa, T. Nakata, K. Sawada and M. Ishida, A versatile integration technology of SOI-MEMS/CMOS devices using microbridge interconnection structures, *J. Microelectromech. Syst.*, vol. 19, no. 4, pp. 919-926, 2010.

[3] K. Takahashi, M. Mita, M. Nakada, D. Yamane, A. Higo, H. Fujita and H. Toshiyoshi, Development of multi-user multi-chip SOI CMOS-MEMS processes, *Proc. IEEE MEMS 2009*, pp. 701-704, 2009.

[4] P. Wessels, M. Swanenberg, H. van Zwol, B. Krabbenborg, H. Boezen, M. Berkhout and A. Grakist, Advanced BCD technology for automotive, audio and power applications, *Solid-State Elect.*, vol.51, no.2, pp. 195-211, 2007.

[5] H. Boezen, S.G. den Hartog, P.J. French and K.A.A. Makinwa, NXP/Philips Semiconductors NV, Method of manufacturing an electronic device and electronic device, *US Patent 0141786A1*, 2006.

[6] R. Dekker, M. Duemling, J.-H. Fock, J.R. Haarsten, H.G.R. Maas, T.M. Michielsen, H. Pohlmann, W. Schnitt and A.M. Tombeur, Substrate transfer: an enabling technology for system-in-package solutions, *Proc. IEEE BCTM 2006*, pp. 8 (10.1), 2006.

[7] V. Rajaraman, K.A.A. Makinwa and P.J. French, DRIE and bonding assisted low cost MEMS processing of in-plane HAR inertial sensors, *Proc. ASDAM 2008*, pp. 327-330, 2008.