TUNABLE CAPACITOR SERIES/SHUNT DESIGN FOR INTEGRATED TUNABLE WIRELESS FRONT END APPLICATIONS

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ABSTRACT

This paper describes the design of a novel tunable RF-MEMS capacitor that is fabricated in a 0.18 µm monolithically integrated RF-MEMS, 50 V LDMOS, 5 V CMOS technology. The novelty of the designs begins with the ability to use a single design for series or shunt capacitors and the ability to distribute the actuator plate around the capacitor in order to develop maximum capacitance. The capacitor structure is a metal-oxide-metal composite, which allows the temperature coefficient to be minimized. The MEMS capacitor has been demonstrated in arrays of 64 tunable capacitors that will be used in tunable solutions for wireless front end applications.

INTRODUCTION

RF MEMS technology has been extensively researched to investigate the development of metal contact switches, capacitive switches and the integration of these elements to produce filters, phase shifters, and impedance matching networks [1]. The research has resulted in significant progress towards producing high volume products that include switches and impedance networks based on tunable capacitors. The progress has included advancements in fabrication and integration with CMOS, reliability, power handing, and linearity. The reliability has focused on the cycling lifetime of metal contact switches and of capacitive switches. Whereas the metal contact switch are limited by the metallurgy that can failure due to cold welding, hot welding, or contact erosion, the capacitive switches or tunable capacitors are limited largely by dielectric charging. It is advancements in these areas, especially reliability that will enable RF MEMS to penetrate commercial, high volume applications. One example is the cell phone market that has been further enabled by the integration of MEMS technology in the form of accelerometers, microphones, and displays. The next step will be to integrate RF MEMS switches and tunable capacitors into the wireless handheld front end.

A key element of the commercialization of RF MEMS is the integration of RF MEMS with a CMOS or RF CMOS process. This integration has been investigated by many parties [2] – [7]. The integration usually involves using a base CMOS process that is qualified and in manufacturing then integrating the RF MEMS process into the CMOS flow with minimal impact to the CMOS devices. The CMOS process used for MEMS applications will usually require high voltage devices because high voltage electrostatic actuators are often used. This requires the design and integration of high voltage charge pumps and high voltage switches with the MEMS devices, which reduces the number of available processes and foundries.

The RF MEMS tunable capacitor described in this paper has been developed to address many of the challenges outlined in this section. The RF MEMS tunable capacitor is integrated with a 0.18 µm, RF-MEMS, 50 V LDMOS, 5 V CMOS process technology. This enables the electrostatic MEMS tunable capacitor to be integrated with an on-chip charge pump and high voltage drivers that lead to on-chip control of a complex array of MEMS capacitors. The base element is a 1 pF unit cell that is comprised of four 250 fF bits and includes the necessary high voltage drivers. The result is a monolithic, integrated tunable capacitor array that can be used for tunable front end applications in cell phones. These applications will include impedance matching, Pas, filters, duplexers, and more fully integrated front ends.

FABRICATION PROCESS

The fabrication process begins with a 200mm wafer and a 0.18 m, monolithically integrated RF-CMOS process that includes a 50 V LDMOS and 5 V CMOS technology. The 50 V LDMOS provides the technology to design an integrated charge pump that can provide up to 50V for the electrostatic actuation of the RF MEMS capacitor. The cross-section of the process flow is shown in Fig. 1. The HV CMOS is shown integrated into the wafer FEOL.

The CMOS metal is comprised of 4, standard CMOS metal and ILD layers. The MEMS metal is comprised of a single thick metal layer and 2 tall vias. The total metal and dielectric stack determine the Cmin parasitic capacitance. The RF MEMS capacitor begins its fabrication process on a fully planarized wafer with exposed vias for interconnection to the CMOS circuits that include HV drivers and charge pump.

The first metal of the MEMS capacitor is used to form the fixed actuator electrodes and the fixed RF capacitor plate. The first meal is covered by a thin dielectric that functions as a fraction of the RF capacitor dielectric. In the devices presented in this paper, the dielectric is 80 nm of HDP oxide and 18 nm of ALD Al_2O_3. The MEMS tunable capacitor beam is formed of metal-oxide-metal composite. The 2nd metal on the underside of the beam is used for the moving actuator electrodes and the moving RF capacitor plate. The metal on top of the beam is patterned using a different mask to create actuator electrodes and the RF capacitor plate. The metal under the beam and metal on top of the beam are matched so that the temperature coefficient and stress sensitivity can be minimized. The upper metal has very little electrostatic coupling to the fixed actuator electrodes or the fixed capacitor plate, so the primary purpose of the metal on top of the beam is to provide the balance against thermal and stress mismatch. (Also, the metal on top of the beam improves the ability to measure the

beam shape using a white light interferometer system (Wyko NT8000 by Veeco). The top metal does not float electrically. The top metal is electrically connected to the corresponding feature on the lower metal by vias through the beam.

The lower beam metal is patterned on a 80 nm thick PECVD oxide. In order to maintain a high degree of symmetry, an 80 nm PECVD oxide is deposited on the upper beam metal too. The through thickness symmetry is important for maintaining the low thermal mismatch and the low stress sensitivity.

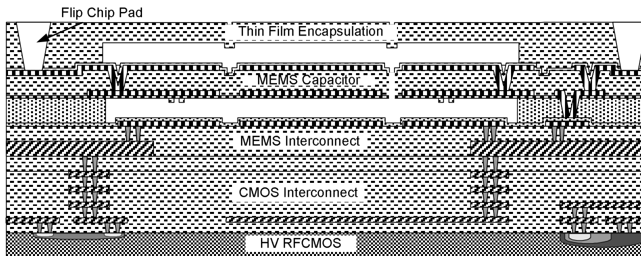

Figure 1: Simplified process cross-section of integrated RF MEMS-CMOS process.

Figure 2 shows an image of the novel tunable RF-MEMS capacitor that is referred to as a sprung cantilever (SC) design. In Figure 2, the anchor of the cantilever is shown. If we follow the cantilever beam to the distal end we find a simple "loop" spring, which is one differentiator with the true cantilever. The loop spring is really a compliant anchor that provides significantly better substrate isolation relative to a fixed-fixed beam design. The addition of the loop spring does increase the pull-in voltage response, but this is in contrast to the advantage it provides to achieve the desired self actuation response. In addition, the loop spring provides reduced sensitivity to process variability, stress variability, and temperature variability. Another advantage of this design is the ability to use the same switch design as a series or shunt element.

In Figure 2, the other characteristics of the SC MEMS capacitor are labeled. The SC is divided into 4 primary elements: Primary Actuator (PA), Secondary Actuator (SA), RF Capacitor (CAP), and the RF Feed. The PA and SA are connected together off the beam, which is the typical use case. It is possible to connect the PA and SA to individual drivers and operate independently. In between the PA and SA is the RF Capacitor, which couples to the fixed RF capacitor plate. The RF capacitor feed runs from the RF capacitor to the anchor of the beam and splits the SA. The RF feed and the SA are separated and isolated by air and silicon oxide. Near the beam anchor, the RF feed is nearly the full width of the beam. The location of the RF capacitor along the beam length has been optimized to provide almost a 2:1 ratio between the self actuation voltage and the pull-in voltage. In addition, this division of the actuator plates and the RF capacitor will result in simultaneous pull-in of the SA and PA. The beam shape will determine the pull-in voltage and whether the PA and SA pull-in simultaneously. A secondary pull-in or release can be observed in the CV, when the PA and SA do not pull-in simultaneously.

In Figure 2, the image shows 2 devices. The device at the top of the image is not actuated so that we can observe the OFF state of the MEMS capacitor. The device at the bottom of the image has been actuated by applying a high voltage (HV) to the fixed SA and PA and applying GND to the SA and PA electrodes on the beam. In this lower image, it is evident that the RF capacitor is flattened during the actuation, which is the purpose of dividing the PA and SA on the two sides of the RF capacitor. The actuated image highlights another feature of the design that is the isolation bumps, which limit the collapse along the beam length and intimate contact between actuator plates. Isolation bumps are located in the PA and SA electrodes on the underside of the beam. Isolation bumps can and have been fabricated on the fixed electrodes instead of on the underside of the beam. In addition, the isolation bumps are optimally placed to minimize contact area between actuator electrodes and to maximize capacitance. If the isolation bumps are too close to the RF capacitor, the maximum capacitance could be reduced. The final features that are visible are the vias that connect the upper and lower beam metallization. The connection between actuator plates is redundant because vias off the beam make this connection too. The RF feed includes vias between the RF capacitor in the lower metal and the upper metal, which is important for optimizing the Q of the device by distributing the RF currents between the lower and upper metallization. The RF via placement is intended to achieve the best possible Q.

When high density arrays of tunable MEMS capacitors are designed, they are designed around a nominal building block that is the 1 pF unit cell. A 1pF unit cell includes four 250 fF bits. A bit in a unit cell can be actuated individually or in tandem. Two RF pads are located at the center of the unit cell. The four bits are grouped as pairs, such that a pair of beams share a single sacrificial layer and are encapsulated under a single hermetic lid. A pair of beams is placed on each side of the RF pads. The unit cells are replicated into m x n arrays to form product die. Within each unit cell, high voltage drivers are included to switch the high actuation voltage to the actuator electrodes. This eliminates the need to flip chip bumps or bond wires to connect to the actuator plates.

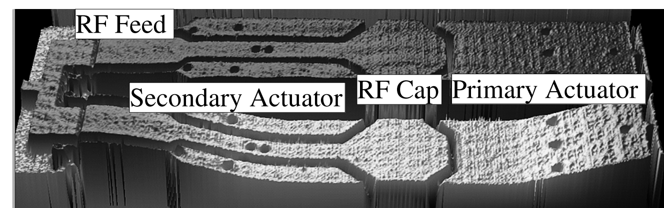

Figure 2: Actuated Wyko image showing actuated tunable MEMS capacitor with functional features defined.

FUNCTIONAL DESIGN

The functional specifications for a 1 pF unit cells is shown in Table 1. The 1pF unit cell is comprised of four 250 fF bits that are designed with a pull-in voltage and self

actuation voltage of 27 V and 40V, respectively. The tunable capacitors are operated with a voltage of 35 V, that is developed on chip by a charge pump with a input voltage of 3.3 V to 5.0 V and a maximum output of 50 V. The operating current is < 100 µA. The RF performance parameters are presented for the 1 pF unit cell that includes four MEMS capacitors. The minimum capacitance, Cmin, is defined when the MEMS capacitors are not actuated. The Cmin is determined by the coupling between the fixed capacitor plate and the moving capacitor plate across a 2 µm air gap. In addition to the minimum capacitance for each beam, the Cmin includes the parasitic capacitance of the flip chip bump pads and the RF feed of the beam to GND. The Cmin is 0.13 pF for 1 pF cell. The Cmax is 1.27 pF for the 1pF unit cell with all four beams actuated. The ΔC is Cmax – Cmin, which is 1.14 pF or a 10:1 tuning ratio. The secod RF parameter of importance is the Q, which is 160 and 87 at 1 GHz and 2 GHz, respectively. The power handling requirement is for 2 W of continuous power.

Table 1: Functional Design Parameters for a 1 pF MEMS RF capacitor cell.

Parameter	Value
Cmin (Off State)	0.13 pF
Cmax (On State)	1.27 pF
Tuning Ratio	10:1
Q at 1 GHz and 2 GHz	160 and 87
Power Handling	2 W Continuous
Pull-in Voltage	27 V
Self actuation Voltage	40 V
Operating Voltage	3.3 to 5.0 V
Charge Pump Output	50 V max
Operating Current	<100 µA

RESULTS

Electromechanical

The electromechanical response of the MEMS capacitor is characterized by the CV curve shown in Figure 3. The bipolar CV curve shows a high degree of symmetry, which means the pull-in voltage, Vpi, the release voltage, Vr, and the Cmax for the bit are the same for the positive and negative voltages. The measured pull-in voltage was 30 V, which is higher than the 27 V target. The measured pull-in differs from the design pull-in voltage because the beam deflects upward after release during fabrication. The CV curve shows the release voltage is 10 V and the release occurs in two steps, which means the secondary actuator electrodes release before the primary actuator electrodes. The Cmax is lower than the design target of 250 fF that is explained by the large curvature at the end of fabrication. The fabrication process is being further optimized to reduce the curvature and lower the deflection of the capacitor.

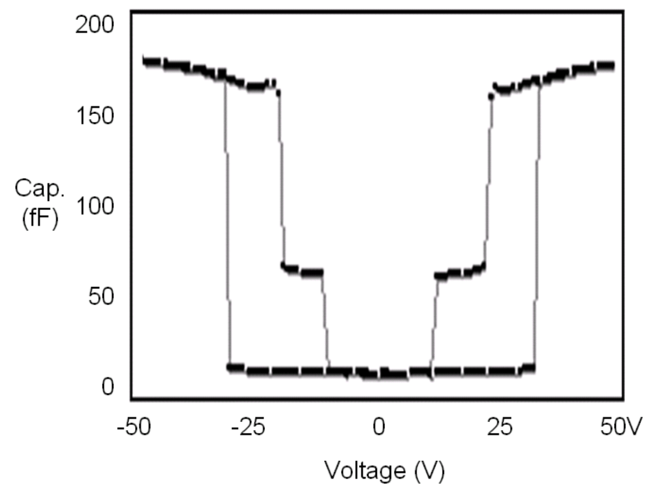

Figure 3. Bipolar CV curve for a 0.25 pF MEMS capacitor.

RF Performance Measurements

The RF performance [8] is described in terms of capacitance and Q measurements that are shown in Figures 4 and 5. The measured and simulated capacitance are shown in Figure 4 for the 1pF unit cell. The simulated and measured Cmin are in excellent agreement. The measured Cmax does not perform to the same level as the simulation suggests. The Cmax underperforms because of the capacitor plate curvature that remains after fabrication. The capacitor curvature is not completely removed during actuation. The measured and simulated Qs are shown in Figure 5. The plot shows excellent agreement between the measured and simulated Qs. The Q is >100 at 1GHz. All simulations are performed using HFSS and half symmetry model of the 1pF unit cell.

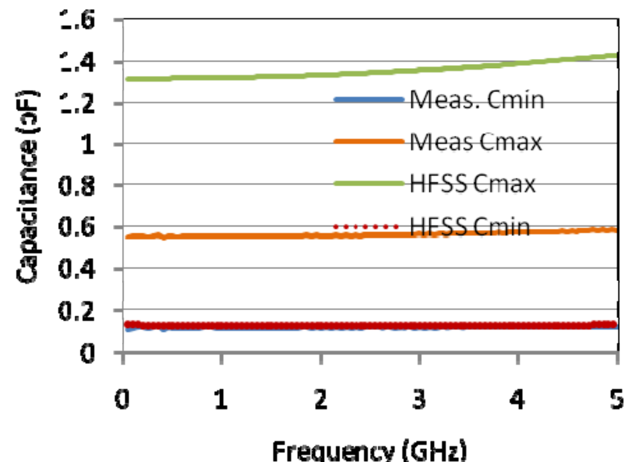

Figure 4: Cmin and Cmax of a 1pF unit cell that contains 2 x 0.25 pF bits. Measured and simulated values are shown.

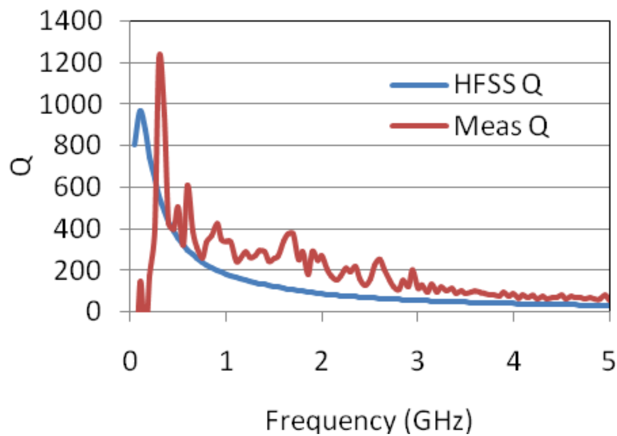

Figure 5: Q factor of a 1 pF unit cell containing 4 x 0.25 pF bits. Measured and simulated values are shown.

CONCLUSIONS

This paper describes a novel tunable RF MEMS capacitor that is fabricated in a 0.18 µm, HV RF CMOS process with wafer level encapsulation. The novel MEM capacitor benefited from a highly symmetric metal-oxide-metal composite that is intended to minimize the temperature and stress sensitivity. In addition, the novel design can be used as a series or shunt design. The electromechanical characteristics have been measured and are in excellent agreement with design targets for the 1 pF unit cell. The measured and simulated RF performance are in excellent agreement for Cmin and Q, with differences in the Cmax that are caused by reduced capacitance density that result from large curvature.

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