HIDDEN-HINGE MICRO-MIRROR ARRAYS MADE BY HETEROGENEOUS INTEGRATION OF TWO MONO-CRYSTALLINE SILICON LAYERS

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ABSTRACT

In this paper we present wafer-level heterogeneous integrated hidden-hinge micro-mirror arrays for adaptive optics applications. The micro-mirrors are made of mono-crystalline silicon and fabricated by two cycles of adhesive wafer bonding on fan-out substrates with addressing electrodes. The fabrication scheme allows the down-scaling of the micro-mirrors in size, the up-scaling of the array size and the implementation of additional material layers. Furthermore, large distances of the micro-mirrors to the electrodes can be achieved and hence a large deflection of the mirrors is possible. The micro-mirrors exhibit excellent deflection stability; no drift or hysteresis can be observed.

INTRODUCTION

For most adaptive-optics applications, micro-mirror arrays (MMA) are required that offer a high mirror planarity and a large and stable analog mirror deflection. Mono-crystalline silicon is well known as a creep-free and stress-free material for micro-mirrors [1]. However, the processing temperatures at which mono-crystalline silicon could be grown exceed 450°C at which CMOS electronics start degrading, so the integration of mono-crystalline silicon mirrors on top of active CMOS backplanes is prohibitive. Therefore, heterogeneous solutions like layer transfer by adhesive wafer bonding are being developed.

Small arrays of piston-type micro-mirrors made from mono-crystalline silicon that allow a large deflection have been reported but do not allow high fill factors [3] or cannot be integrated with CMOS back plane electronics [4]. Large piston-type micro-mirror arrays with comb-drive actuators or hinges underneath the mirror plates made from mono-crystalline silicon were heterogeneously integrated by flip-chip bonding [5][6]. However, they do not allow for small pixel sizes since downscaling of the flip-chip bonds is limited. Large arrays of tilting micro-mirrors and piston-type micro-mirrors made from a single layer of mono-crystalline silicon were reported previously [2][7]. However, single layer micro-mirrors with hinges and mirror plates fabricated from the same material layer are susceptible to micro-mirror deformation upon actuation and are limited in their maximal fill factor due to the space that is needed for the hinges. The aim of this work is to investigate the CMOS compatible heterogeneous integration of multiple material layers with passive fan-out wafers on wafer-level with a large distance between the layers for MOEMS applications. We show hidden-hinge micro-mirror arrays from two mono-crystalline silicon layers.

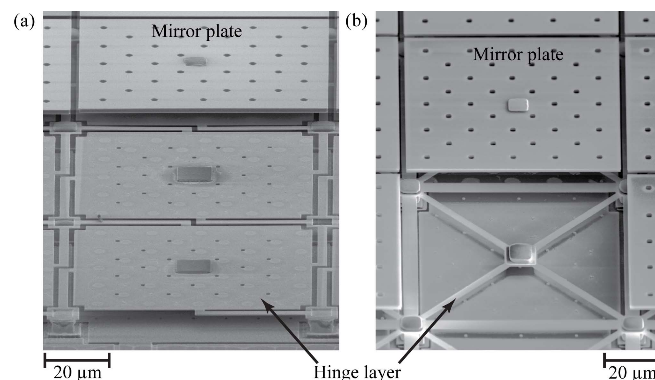

Fig. 1: Side view on the micro-mirror arrays. The top mirror plate is missing and allows a view on the hinge layer. Two hinge variants are implemented. Left: parallel plate hinges. Right: non-linear diagonal beam hinges.

DESIGN

The spatial light modulators in this work are based on a two-level architecture with flexible micro-mirror hinges from 340 nm thick mono-crystalline silicon on the first level and stiff micro-mirror plates from 1500 nm thick mono-crystalline silicon on the second level, as shown in Figure 1. The hinges and micro-mirrors are electrically interconnected and on the same potential. A bottom electrode on the fan-out wafer underneath each micro-mirror structure allows the

TABLE I
CHARACTERISTICS OF THE MICRO-MIRROR ARRAYS

Property	Value
SLM architecture	Piston-type (vertical parallel movement) with hidden hinges underneath the mirror plates. (2-level)
Hinge architecture	Parallel plate / diagonal beam
Array size	48 x 48 mirrors
Hinge material	Mono-crystalline silicon
Mirror material	Mono-crystalline silicon
Crystal type (c-Si)	Diamond-cubic (100)
Plastic deformation (c-Si)	None (brittle material)
Young`s modulus	160 GPa
C-Si roughness (RMS)	<1 nm (for area of 1 µm²)
Mirror size	78.5 x 78.5 µm²
Mirror pitch	80 µm
Hinge layer thickness	340 nm
Mirror-membrane thickness	1500 nm
Mirror air gap to electrode	10 µm
Hinge air gap to electrode	5 µm
Max. deflection (tilt)	~ 1600 nm / > 545 nm

electrostatic actuation and a vertical piston-type parallel deflection of the micro-mirrors in respect to the bottom substrate. The hinge structure is pinned to four posts on the bottom substrate at the edges of each micro-mirror segment and held at a distance of 5 µm to the bottom actuation electrode. Each post is shared with the 4 neighboring micro-mirrors. A post in the center of each hinge structure is used to pin the top micro-mirror plate at a distance of 5 µm to the hinge layer, resulting in a total air gap of 10 µm from the micro-mirror plate to the bottom actuation electrode.

We have included two hinge variants in the layout; parallel plate hinges [Figure 1 (a)] and nonlinear diagonal beam hinges [Figure 1 (b)]. The parallel plate hinge variant is based on the design of single layer micro-mirrors with hinges and mirror plates made in the same layer. This single layer design is extended by an additional micro-mirror plate layer that allows a high fill factor of the array and does not deform upon actuation. In this design the electrically active electrode is the hinge plate and the distance between the hinge plate and the bottom electrode defines the electrostatic gap. The hinges of the diagonal beam hinge variant are string like structures that are bended and strained upon actuation and therefore offer a higher restoring force in comparison. However, in this design the hinge layer contributes only little to the electrostatic attraction, as the total area is much smaller than the mirror plate area. Here the mirror-plate on top of the hinges is the main electrically active electrode at which the electrostatic forces apply.

The signal routing for an individual actuation of each micro-mirror with only one metallization layer on the fan-out wafer is not possible for large actuator arrays, so the bottom electrodes are interconnected in columns and allow the actuation of micro-mirrors in segments. The micro-mirror arrays consist of 48 x 48 square micro-mirrors with 80 µm pitch. The segment size of dependently actuated micro-mirrors is 4 x 24 pixels. Table I lists technical parameters of the micro-mirror arrays.

FABRICATION

The heterogeneous integration of two layers of mono-crystalline silicon from SOI donor wafers in this work has been performed with passive fan-out substrates that mimic the surface properties of real CMOS wafers. However, the fabrication scheme is designed for integration with CMOS wafers including the BEOL metallization layers.

The detailed process flow in Fig. 2 illustrates the fabrication of the micro-mirror arrays. The fabrication starts with the preparation of the fan-out substrate [Figure 2(a)]; the bottom electrodes of the micro-mirrors and the signal wiring including bond pads are patterned from 500 nm thick aluminum layer (AlSiCu) that is sputter deposited onto an oxidized silicon wafer. Micro-mirror posts for pinning the hinge layer will be metal plated at a later stage in the process, so a plating-base from nickel is deposited at those positions in a lift-off process. To prevent short-circuiting of the micro-mirrors in case of a micro-mirror pull-in, small SiO_2 stopper structures are created on the bottom electrodes by plasma enhanced chemical vapor deposition (PECVD) and subsequent reactive ion etching (RIE).

The heterogeneous integration sequence starts with spin-coating of a polymer spacer onto the bottom substrate; it defines the distance of the hinge layer to the bottom electrodes on the fan-out wafer. As the bottom substrate is not planarized, the surface topography is projected to the

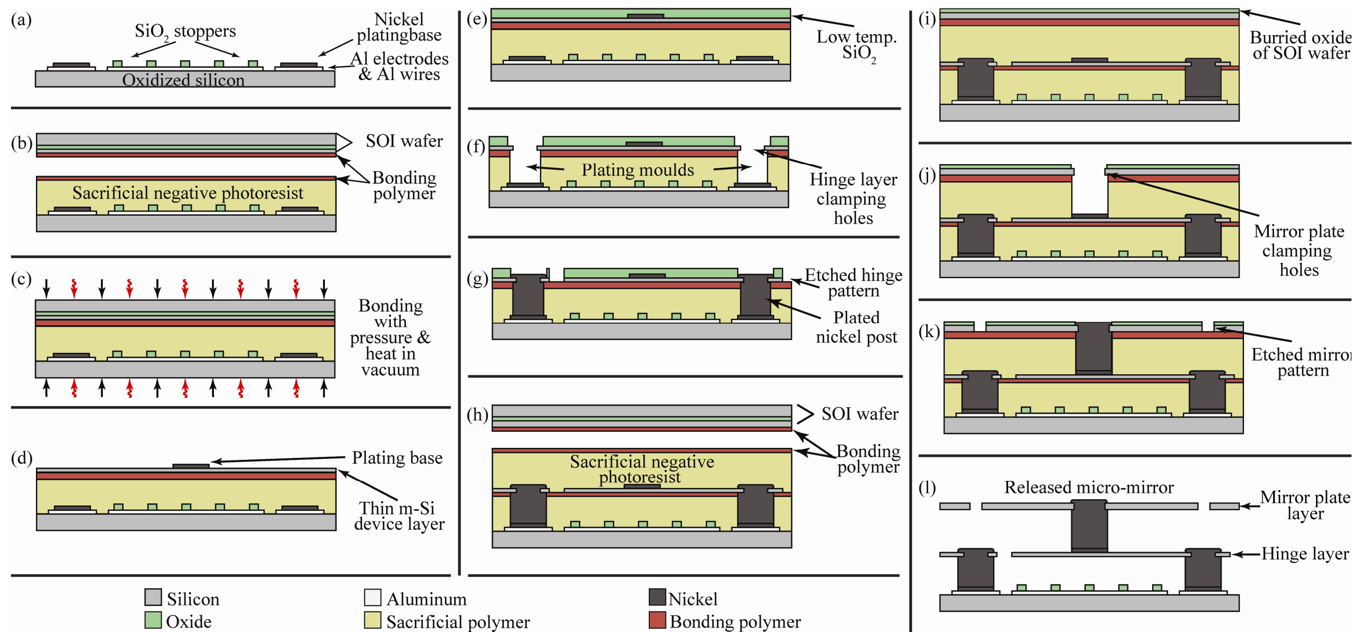

Fig. 2: CMOS compatible fabrication process for the hidden-hinge micro-mirror arrays. Both, the hidden-hinge layer and the micro-mirror plate layer are made from mono-crystalline silicon that originates from SOI donor wafers. The heterogeneous integration with a fan-out wafer that employs actuation electrodes is done by two cycles of adhesive wafer bonding.

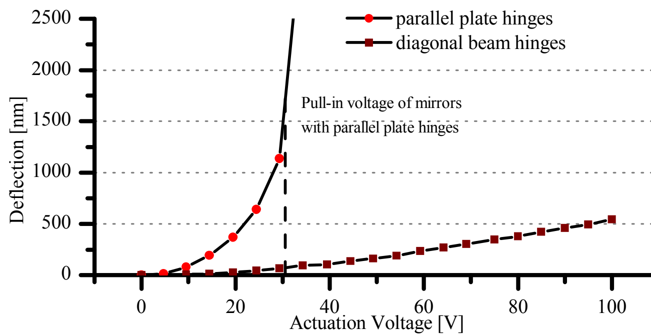

Fig. 3: z(V)-deflection of micro-mirror arrays with parallel plate hinges (1) and non-linear diagonal beam hinges (2). The micro-mirrors with non-linear hinges show an almost linear deflection-voltage dependency. Note: The electrostatic gap for the two designs is different in that the hinge acts as moving electrode in (1) whereas the mirror plate is the moving electrode in (2).

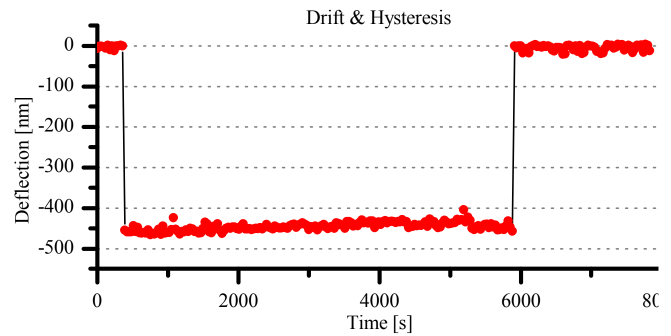

Fig. 4: The deflection stability over time for micro-mirrors with non-linear diagonal beam hinges.

surface of the sacrificial layer if standard spin-coating is used. Therefore, the polymer is applied in multiple cycles, each cycle adding 1 µm to the total sacrificial layer thickness up to a total thickness of 5 µm. In that way the surface topography of the sacrificial layer is reduced by 400 % to 40 nm peak-to-valley as compared to standard spin-coating. The polymer AZ nLof 2000, a high temperature resistant negative photoresist is hard baked at 200°C for 5 minutes in between each step to achieve full curing and preventing a partial dissolving during the following spin-coating cycle. Thereafter, a thin bonding polymer, mr-I 9000, is spin-coated onto the sacrificial layer on the fan-out wafer and onto the 340 nm thick device layer of the first SOI wafer and pre-cured for 2 minutes at 120 °C [Figure 2(b)]. The wafers are loaded into a commercial wafer bonder with the device layer of the SOI wafer facing the sacrificial layer of the fan-out wafer. The wafers are bonded at 200 °C and a pressure of 4500 mbar for 2 hours in vacuum [Figure 2(c)]. After bonding the backside of the SOI wafer is removed by dry etching in SF_6 plasma with subsequent removal of the buried oxide layer in buffered hydrofluoric acid (BHF). A nickel plating base for the later metal plated mirror plate posts is deposited onto the silicon device layer in a lift-off process [Figure 2(d)].

At this stage the transferred mono-crystalline silicon device layer is not permanently attached to the bottom fan-out wafer. Nickel posts will be plated from the bottom substrate up to the hinge silicon layer for permanent mechanical and electrical connection. To prevent the plating at the position of the mirror post that has been prepared for a second plating step later in the process, the device layer is covered with a low temperature SiO_2 cladding that is PECVD deposited at 100 °C [Figure 2 (e)]. The SiO_2 layer is used as a hard mask for etching clamping holes into the silicon device layer and the subsequent anisotropic resist etching of the underlying polymer layers to form via-holes to the bottom plating bases on the fan-out wafer. Thereafter, the SiO_2 mask openings are broadened in vaporized hydrofluoric acid to expose a larger silicon area at the clamping holes and ensure a sufficient surface area for a reliable metal-silicon interface [Figure 2(f)]. The final post formation is done with electroless nickel plating at 92°C in a commercial nickel hypophosphite electrolyte [Figure 2(g)]. Thereafter, the hinge pattern is etched with RIE into the silicon layer and the low temperature oxide layer is removed in buffered hydrofluoric acid.

The second layer transfer starts with application of a second 5µm thick sacrificial polymer layer in multiple 1µm thick cycles, as described earlier. The bonding polymer is applied to the surface of the second sacrificial polymer and to the 1500 nm thick device layer of the second SOI wafer [Figure 2(h)]. In analogy to the first integration sequence, the wafers are bonded and the handling substrate of the SOI wafer is removed [Figure 2(i)]. The buried oxide is now used as a hard mask for etching the clamping holes into the silicon layer and via holes into the second polymer spacer down to the platingbase on the silicon hinge layer [Figure 2(j)]. The oxide layer is broadened at the clamping holes and nickel posts are electroless plated to clamp the silicon layer. Now the mirror plate pattern is etched into the second silicon layer [Figure 2(k)] and the SiO_2 mask is removed in BHF. The micro-mirrors structures are finally released in isotropic oxygen plasma etch [Figure 2(l)].

CHARACTERIZATION

The optical performance of micro-mirror arrays is assessed by their optical properties and static and dynamic mechanical properties. Together, they define the fundamentally attainable device performance. The dynamic mechanical performance of the micro-mirror array is primarily determined by the deflection dependence on the applied voltage, the deflection stability over time and the imprinting behavior, which is the remaining deflection of the micro-mirrors after switching-off the actuation voltage. The static mechanical performance is determined by evaluation of the surface topography in an interferometric measurement.

The MMAs were characterized with a white-light interferometer Wyko NT 9300. For the evaluation of the mechanical mirror performance, dedicated data-acquisition and analysis software was used that allows the evaluation of large numbers of micro-mirrors in parallel. Within the static mechanical measurement 12 micro-mirrors are measured at

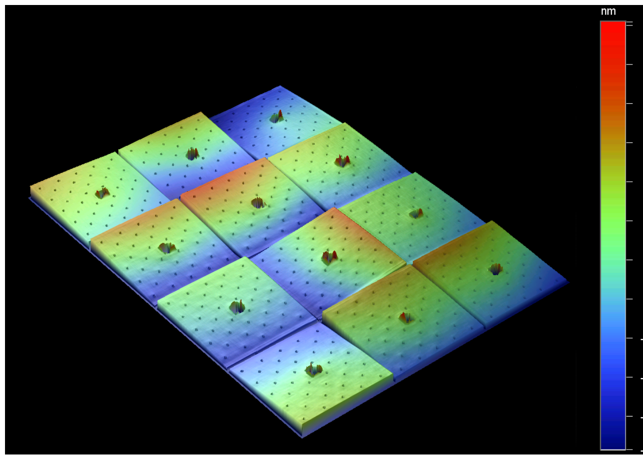

Fig. 5: Surface topography of the micro-mirror array measured with a white-light interferometer and exaggerated in z direction. The micro-mirror arrays suffer from an arbitrary mirror pre-tilt and height variations.

a time. The dynamic properties were determined by actuation and comparison of the micro-mirror deflection at the beginning and the end of a deflection cycle.

RESULTS & DISCUSSION

Dynamic properties

Figure 3 shows the deflection curves in dependence of the actuation voltage for the two micro-mirror variants with parallel plate hinge design and diagonal beam hinge design, respectively. The maximum attainable deflection depends on geometrical hinge-design parameters, and the distance between the "acting" electrodes.

In case of the parallel plate hinge design the acting electrodes are the bottom driving electrode on the substrate wafer and the hinge plate with an effective electrode distance of 5 µm. The deflection curve shows the typical parabolic behavior and the micro-mirrors snap into pull-in at a deflection of about 1600 nm which is roughly one third of the electrode distance.

The contribution to the total electrostatic force of the diagonal beam hinges can be neglected over a wide deflection rage as their total area is small compared to the micro-mirror area. Hence, the micro-mirror plate can be considered the main acting electrode. As the distance of the micro-mirror plate to the bottom electrode is 10 µm, the electrostatic force is smaller compared to the parallel plate hinge micro-mirrors and leads to the deflection difference at the same actuation voltage. However, the deflection curve is substantially different from the parabolic profile of the parallel plate design; it behaves over a wide range almost linear. This is due to the non-linear increasing restoring force that originates from material strain in the beams upon deflection. In theory, the maximum mirror deflection of this design exceeds the maximum deflection of parallel plate designs. However, the large effective electrode distance prevents an evaluation of the maximum deflection.

The deflection stability is shown in Figure 4 for micro-mirrors with diagonal beam hinges. The micro-mirrors were actuated with a fixed driving voltage close to their maximum deflection for a period of about 1.5 hours and the relative micro-mirror height was recorded. A hysteresis free micro-mirror reaches its maximum deflection instantly when the actuation voltage is turned on and returns to its initial position instantly after it is turned off. As expected for actuators made from perfectly elastic mono-crystalline silicon, the micro-mirrors in this work are drift-free and show no hysteresis; the scattering deflection values over time originate from environmental drop-ins. The measurements demonstrate the stable performance and potential of mono-crystalline silicon and of the fabricated micro-mirrors for demanding applications.

Static properties

Figure 5 shows the surface profile of one measurement field on the micro-mirror array without actuation, exaggerated in z-direction. The micro-mirrors suffer from arbitrary height deviation (σ_z) of up to 94 nm, pre-tilt with values of 0.3°, and an array roughness R_a of 73 nm. This behavior indicates a compressive stress relaxation in the hinge layer; several explanations for this behavior are feasible, such as a temperature gradient in the wafer stack during bonding or a pre-strained silicon device layer on the SOI wafer and need to be further investigated.

CONCLUSION

The hidden-hinge micro-mirrors from two mono-crystalline silicon layers exhibit an excellent stability; they provide drift-free operation and show no hysteresis. The ability to heterogeneously integrate multiple mono-crystalline material layers with CMOS electronics enables the fabrication of Microsystems with increased design complexity, higher integration densities and allows for the deployment of special required characteristics for each layer independently.

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