ABOVE-IC GENERIC POLY-SIGE THIN FILM WAFER LEVEL PACKAGING AND MEM DEVICE TECHNOLOGY: APPLICATION TO ACCELEROMETERS

B. Guo[1], L. Wen[2], P. Helin[1], G. Claes[1], A. Verbist[1], R. Van Hoof[1], B. Du Bois[1], J. De Coster[1], I. De Wolf[1], A. Hadi Shahar[1], Y. Li[1], H. Cui[1], M. Lux[1], G. Vereecke[1], H. A C Tilmans[1], L. Haspeslagh[1], S. Decoutere[1], H. Osman[1], R. Puers[2], S. Severi[1] and A. Witvrouw[1]

[1] Imec, Kapeldreef 75, Leuven, B-3001 BELGIUM

[2] MICAS, KUL, Leuven, B-3001 BELGIUM

ABSTRACT

We present an attractive poly-SiGe thin film packaging and MEM (Micro Electro-Mechanical) platform technology for integrating various packaged MEM devices above standard CMOS. The packages, having cavities as large as 1mm^2, make use of pillars designed to withstand subsequent molding during 1st level packaging. Covers on top of the release holes avoid deposition inside the cavity during sealing. Hermeticity is proven in vacuum, air and N_2 atmosphere and at different temperatures. Packaged functional accelerometers sealed at a pressure around 1bar, have an equivalent performance in measuring accelerations of about 1g compared to a piezoelectric commercial reference device.

INTRODUCTION

Above-CMOS MEMS enables the integration of multi-functional devices or arrays on a single chip with increased performance and reduced size. In the past years, several CMOS-integrated MEM devices have been fabricated using imec's poly-SiGe MEMS-last technology [1-3]. Packaging was done by chip capping or by placing a naked die in a 1st level package.

MEMS devices often need a hermetic and/or vacuum package, which is preferably processed on the wafer level, before dicing. However, there is currently no standard for (wafer level) MEMS packaging. Chip capping by wafer bonding techniques is often used for MEMS packaging, yet thin film packaging allows for a fully integrated process flow with small pitch using a batch process. Epi-Si, poly-Si, Alumina, Si-nitride and Si-carbide membranes have already been used for thin film packaging [4-8], but a generic above-IC thin film package process is still missing.

In this paper, with new thin film capping process, poly-SiGe accelerometers and resonators are fabricated together with their poly-SiGe package. Novel covers on top of the release holes avoid deposition inside the cavity during sealing. The whole process flow is run at temperatures ≤455°C. Short-term hermeticity is proven in vacuum, air and N_2 atmosphere and at different temperatures. A modified version of this process has been used to hermetically package SOI resonators lower than 10Pa (0.1mbar) [9].

PROCESSING

Fig. 1 shows a schematic overview of the MEM device and its cap in the poly-SiGe technology. Poly-SiGe electrodes and mechanical structures are fabricated above a planarised standard back-end-finished CMOS wafer, as also described in [1-3].

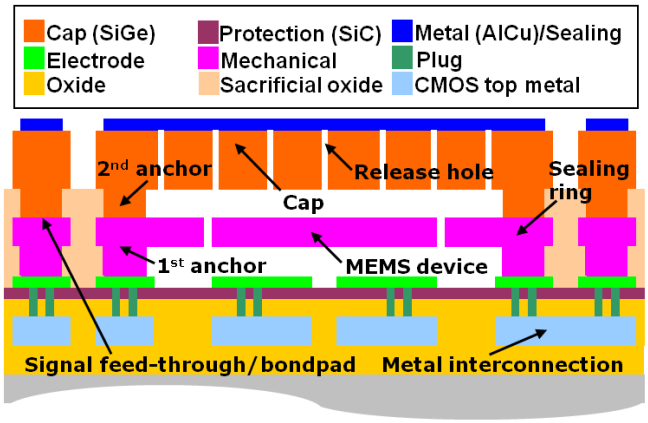

Figure 1 – Schematic cross section of the poly-SiGe based MEMS platform: on top of a CMOS wafer, poly-SiGe electrodes, mechanically functional devices and their wafer level thin film package are integrated using surface micromachining.

In this work, accelerometers and resonant beam structures (Fig. 2) are defined on top of a simple AlCu interconnection that mimics the CMOS. After the mechanical layer patterning, a planarization by HDP Si-oxide filling and CMP is performed to define the sacrificial layer between the MEM device and the package (Fig. 3a).

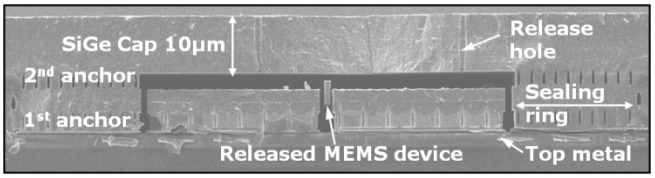

Figure 2 – Thin film wafer level packaging of a 1µm-wide clamped-clamped (c-c) beam resonator: complete stack after release. A sealing film will be deposited on top of the SiGe cap to finish the wafer level package.

Anchors (1µm wide and 3µm deep) are defined and filled with the 10µm thick SiGe cap layer. In this cap, release holes are etched (Fig. 3b) and a micro-crystalline SiGe (µc-SiGe) cover is formed with a process shown in Figure 4a and 4b. All sacrificial oxide inside the cavity is then removed by vapor HF (vHF) through the local micro-channels in the µc-SiGe covers. These micro-channels, with a dimension significantly smaller than 100nm, are formed during the non

conformal µc-SiGe PECVD deposition. The micro-channels prevent AlCu deposition inside the cavity during the sealing process (Fig. 4c). This achievement could be otherwise obtained only with extreme high aspect ratio release holes. The presence of the covers does not change the vHF Si-oxide etch rate (Fig. 5).

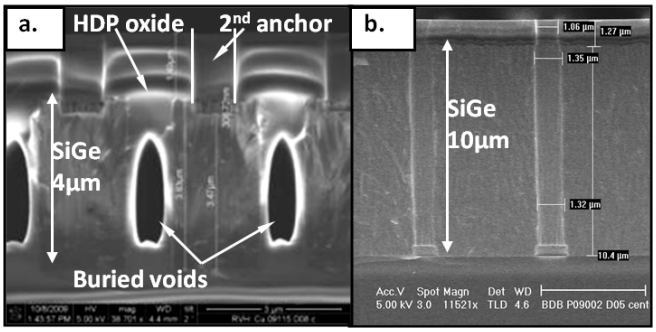

Figure 3 – a. 2nd anchor formation after planarization of the 2nd sacrificial oxide using HDP oxide filling and global CMP; b. release hole opening in the 10 µm thick SiGe cap.

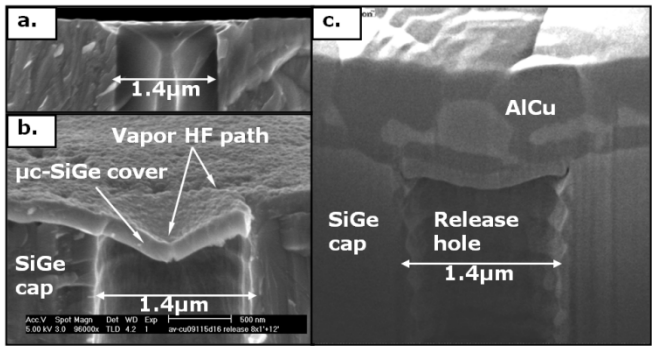

Figure 4 – a. planarised surface after oxide filling in the release hole using oxide dry recess; b. locally porous micro-crystalline SiGe (µc-SiGe) cover formed above the release hole after the oxide is removed by vHF; c. AlCu thin film sealing above the µc-SiGe cover.

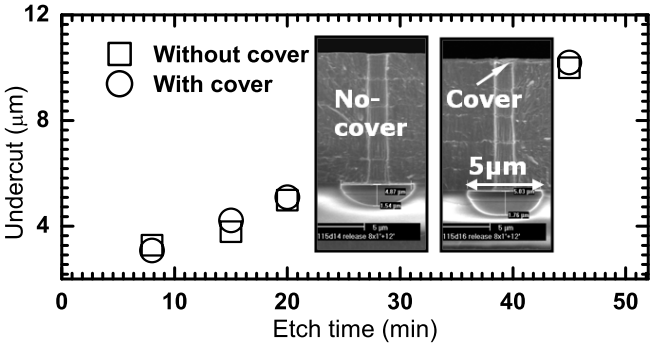

Figure 5 – Undercut in the cavity under the release holes with or without µc-SiGe covers.

After AlCu sealing, the sealing layer and the SiGe cap are patterned (Fig. 6). Note that the anchors supporting the package are surrounded by HDP oxide (see also Fig. 1), thus increasing the package strength and protection towards the environment. The in-plane and out-of-plane accelerometers after removal of the cap are shown in Figure 7. To support the package for subsequent plastic molding, there are 18×18µm^2 SiGe pillars (Fig. 6b and Fig. 7) with spacings ranging from 80µm - 150µm [10] implemented in the design.

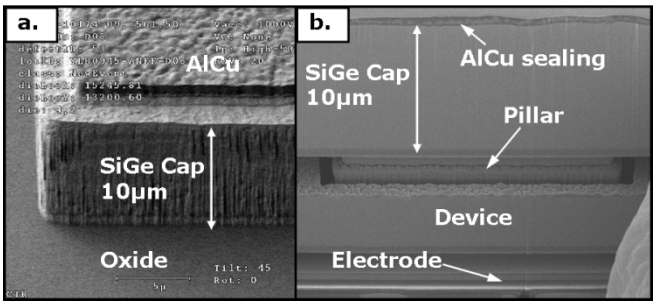

Figure 6 – a. tilted SEM of the finished package; b. cross-sectional FIB SEM showing a 18×18µm^2 pillar and the accelerometer structure, as well as the cap and sealing of a packaged large out-of-plane accelerometer in a 1mm^2 cavity.

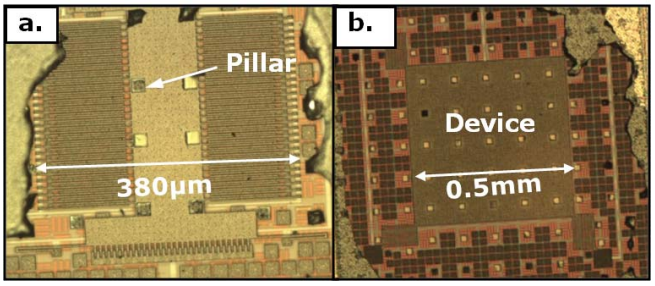

Figure 7 – Two packaged accelerometers after cap removal by tape: a. small in-plane; b. large out-of-plane.

PACKAGING EVALUATION

The Quality factor (Q) of un-packaged devices (resonators and accelerometers), fabricated using the same process flow, is used as a metric for pressure (Fig. 8). A very large pressure range of 10^{-4}-10^{3} mbar is covered.

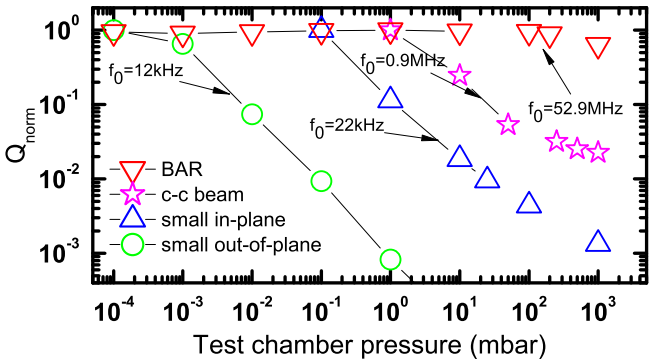

Figure 8 – Normalized Quality factor (Q_{norm}) values for un-packaged devices measured in N_2 at 25°C. The maximum Q is: BAR (2×10^4), c-c beam (3×10^3), small in-plane (1×10^4), small out-of-plane (1.8×10^4).

The variations versus pressure of the Q of c-c beam resonators (unpackaged, packaged but not sealed and after AlCu sealing) show that hermetically sealed cavities with a high sealed-in pressure (around 1bar) are obtained (Fig. 9).

This is further confirmed by the unchanged Q after 6 weeks storage in vacuum, indicating an (at least medium term) hermetic package.

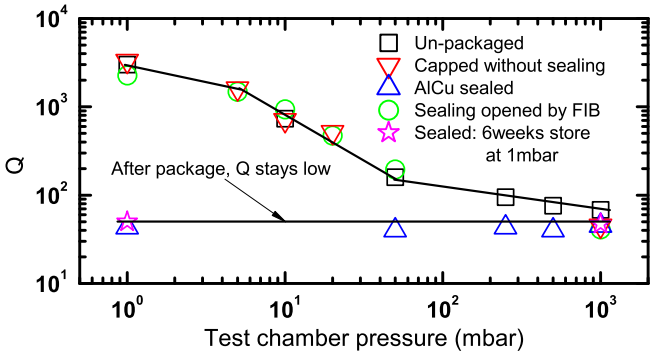

Figure 9 – Q for c-c beam resonators measured in N_2 at 25°C. The solid lines are used to guide eyes.

Moreover, the packaging and sealing processes do not affect the device behavior, as proven by the high Q measured at low pressure for a device with its package opened by Focused Ion Beam (FIB) (Fig. 10).

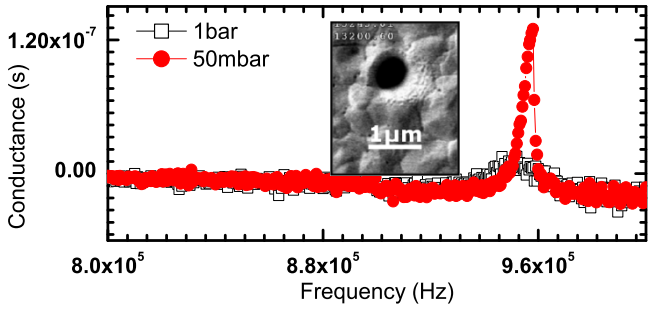

Figure 10 – Resonance of a packaged c-c beam resonator with sealing opened by FIB measured in N_2 at different pressures, 25°C, V_{dc}=30V and V_{ac}=0.5V.

High temperature tests in N_2 further prove the hermeticity under high stress conditions (Fig. 11). The lowering of the Q at high temperature can possibly be explained by a thermally activated loss mechanism.

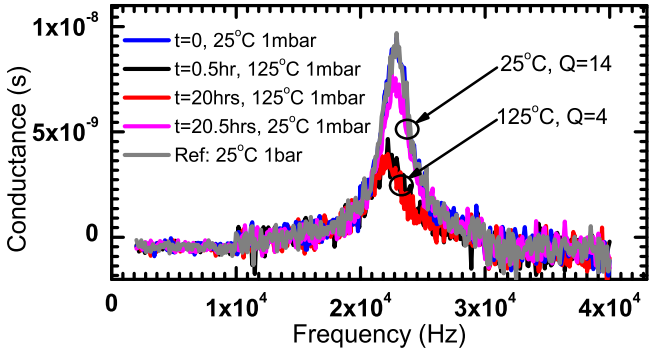

Figure 11 – Resonance curves of a packaged small in-plane accelerometer stored in N_2 at 1mbar and 125°C, V_{dc}=2V, V_{ac}=0.5V.

The high temperature (Fig.11) and low temperature (Table 1) measurements of packaged accelerometers show that for a large range of temperatures, the package stays hermetic and the gas ambient in the sealed package does not affect the device behavior.

Table 1: Quality factors of a packaged small in-plane accelerometer measured at low temperatures.

T=0°C	T=5°C	T=15°C	T=25°C
14	15	14	15

DISCUSSION

The 1bar sealed-in pressure achieved in this work is beneficial for accelerometers which often need controlled damping during operation. However, this pressure level was not expected because the AlCu was deposited by sputtering, during which the working pressure was around 1Pa (0.01mbar). Outgassing and a temporary leak have been investigated as potential causes for this sealed-in pressure.

APIMS measurements (Fig. 12) [11] show that water is outgassed from blanket SiGe layers at 450°C. As an ex-situ anneal at 450°C was done before sealing and as the observed outgassing rates are low, outgassing from blanket layers is not expected to cause a 1bar pressure increase.

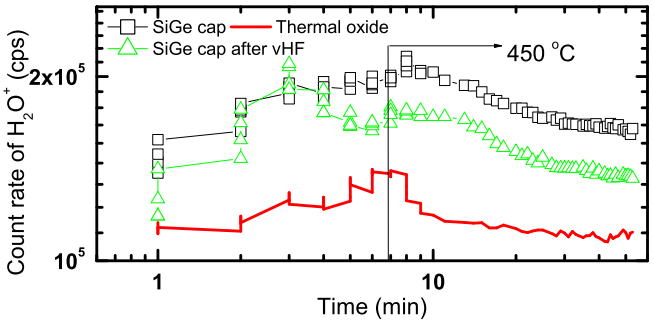

Figure 12 – APIMS measurements at 450°C for blanket SiGe films with or without 90mins vHF etch. 100nm thermal oxide is used as a reference.

Another possible explanation for the 1 bar sealed-in pressure is a temporary leak due to a weak (oxygen-rich) interface (e.g. µc-SiGe to cap). This interface is exposed to the ambient when the AlCu and µc-SiGe are etched (stopping on the SiGe cap) (Fig. 6) after which the pressure inside the cavity could increase rapidly. The leak path is then assumed to be closed by high polymerization during the consequent SiGe cap etch and by SiGe oxidization during the plasma resist ash. Submitting the 1-bar packaged devices to the harsh 85/85 highly accelerated storage test (HAST) resulted in defective devices after 2 weeks. This result, together with the good results in non-humid test conditions, points towards this weakly sealed interface. Moreover, by replacing the µc-SiGe to cap interface with an AlCu to cap interface, the temporary leak path has been removed thanks to intermixing between AlCu and (cap) SiGe at 350°C (AlCu PVD temperature). The sealed-in pressure has thus been reduced to 20-30mbar with an in-situ outgassing step. Packages with this improved interface have survived the severe HAST test for up to 3 weeks (Table 2) (the test is still ongoing). Therefore, to reach

hermeticity for the 1-bar sealed packages under harsh conditions, an extra AlCu sealing layer plus additional litho can be used to protect the exposed µc-SiGe to cap interface.

Table 2: Cavity pressure (calibrated using Fig. 9) for a low pressure sealed package with the improved interface in the HAST (85°C and 85% relative humidity at 1 bar). The pressure change is within the measurement error.

Time (week)	**0**	**1**	**2**	**3**
Cavity pressure (mbar)	23.4	26.8	23.5	23.2

APPLICATION TO ACCELEROMETERS

CV curves for different packaged in-plane and out-of-plane accelerometers were measured (Fig. 13).

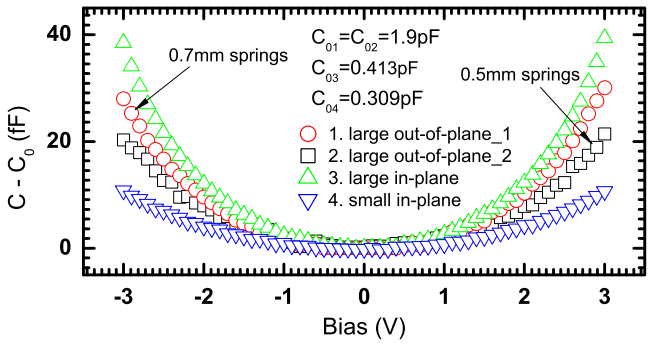

Figure 13 – Measured CV curves for different types of packaged accelerometers, f=1MHz, V_{ac}=0.5V.

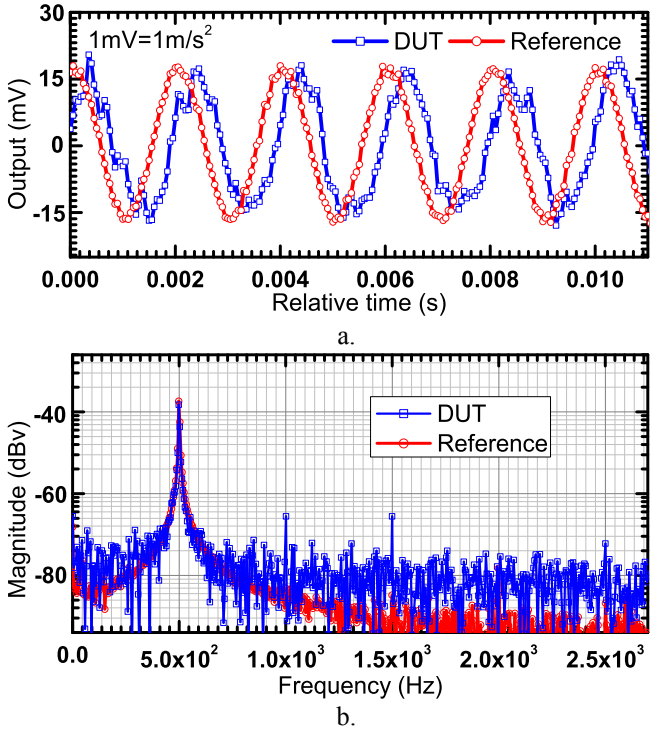

Figure 14 – Vibration tests in a shaker of a packaged small in-plane accelerometer and a Brüel & Kjær 4383 piezoelectric charge accelerometer as reference device. The packaged accelerometer in this work has a similar response as the commercial reference device.

Long spring lengths have been used in order to obtain extremely low spring constant values for low-g sensing.

Dynamic tests were performed for a packaged small in-plane accelerometer on a vibration test setup. Sinusoidal actuation (vibration) tests show similar results for the device under tests (DUT) and a Brüel & Kjær 4383 piezoelectric charge reference accelerometer across the actuation frequency band (Fig. 14).

CONCLUSION

Functional accelerometers and resonant devices are integrated with their hermetic thin film package by using a poly-SiGe based fully CMOS compatible process. The wafer level thin film encapsulation process uses a novel cover-based release process. Both the packaging process and the sealed-in ambient do not affect the device performance. Vibration tests for a packaged accelerometer show that the DUT has a similar response as the commercial piezoelectric reference device in measuring accelerations of about 1g.

ACKNOWLEDGEMENT

The authors would like to acknowledge the help from Gaetano Santoro, Hugo Bender, Myriam Van De Peer, Olalla Varela Pedreira, and Piotr Czarnecki for inspection and characterization.

REFERENCES

[1] L. Haspeslagh *et al.*, "A. Highly reliable CMOS-integrated 11MPixel SiGe-based micro-mirror arrays for high-end industrial applications", *IEDM*, San Francisco, CA, 2008, pp. 655.

[2] S. Severi *et al*, "CMOS-integrated poly-SiGe cantilevers with read/write system for probe storage device", *TRANSDUCERS*, Denver, CO, 2009, pp. 2409.

[3] A. Schreurle *et al.*, "A 10 µm thick poly-SiGe gyroscope processed above 0.35 µm CMOS", *IEEE MEMS*, Golden, Colorado, 2007, pp. 39.

[4] http://www.sitime.com.

[5] H. Stahl *et al.*, "Thin Film Encapsulation of Acceleration Sensors using Polysilicon Sacrificial Layers", *TRANSDUCERS*, Boston, USA, 2003, pp. 1899.

[6] R. He et al., "A low temperature vacuum package utilizing porous alumina thin film encapsulation", *IEEE MEMS*, Istanbul, Turkey, 2006, pp. 126.

[7] Q. Li *et al.*, "Failure analysis of a thin-film nitride MEMS package", *Microelectronics Reliability*, Vol. 48, pp. 1557, 2008.

[8] V. Rajaraman *et al.*, "Robust wafer-level thin-film encapsulation of microstructures using low stress PECVD silicon carbide", *IEEE MEMS*, Sorrento, Italy, 2009, pp. 140.

[9] Y. Naito *et al.*, "High-Q Torsional Mode Si Triangular Beam Resonators Encapsulated using SiGe Thin Film", *IEDM*, San Francisco, CA, USA, 2010.

[10] P. Gonzalez *et al.*, "Design and characterization of thin SiGe membranes for MEMS packaging at wafer level", *Proc. Semiconductor Advances for Future Electronics Workshop (SAFE)*, Veldhoven, The Netherlands, 2008, pp. 548.

[11] G. Vereecke *et al.*, "Wafer thermal desorption spectrometry in a rapid thermal processor using atmospheric pressure ionization mass spectrometry", *IEEE Trans. Semicond. Manuf.*, Vol. 13 No.3, pp. 315, 2000.