HETEROGENEOUS INTEGRATION TECHNOLOGY FOR COMBINATION OF DIFFERENT WAFER SIZES USING AN EXPANDABLE HANDLE SUBSTRATE

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ABSTRACT

This paper reports on the realization of a novel method for batch transfer of multiple separate dies from a smaller substrate onto a larger wafer substrate by using a standard matrix expander in combination with adhesive wafer bonding and an elastic dice tape. We demonstrate the expansion and transfer of about 30000 chips from a 100 mm wafer to a 200 mm wafer with a 22 μm standard deviation of positioning accuracy. Fabrication, evaluation method and results are presented.

INTRODUCTION

Many of the devices and processes of interest in heterogeneous integration [1-3] together with MEMS and CMOS are fabricated using small sized substrates. For example III-V substrates, used in photonic applications, have a typical diameter of less than 100 mm. Commercial silicon MEMS and CMOS production on the other hand is done on wafer diameters of 200 mm and above. This wafer size incompatibility excludes the use of standard wafer level heterogeneous integration technologies for photonics. In addition, the transferred material is typically only needed in a small part of the silicon chip footprint. This implies that a one-to-one wafer bonding between differently sized wafers would result in waste of material in the chip areas were the transferred material is not needed.

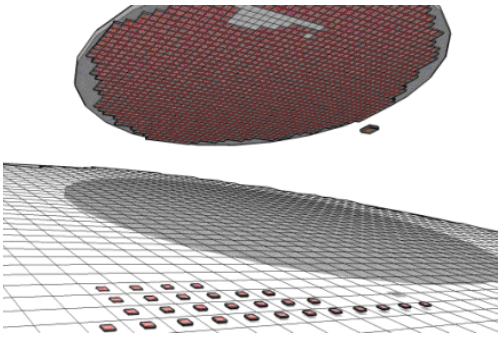

Figure 1a: Illustration of integrating incompatible wafer-sizes. In existing technologies, dies are mapped onto larger substrates one-by-one by chip-to-wafer placement techniques.

An alternative method has been reported earlier [4] were individual dies are pick-and-placed to a silicon target wafer sequentially. Chip wise adhesive bonding also alleviates some of the stress that can be induced by wafer to wafer bonding of wafers that have different coefficients of thermal expansion [5]. The approach presented in this paper yields a faster batch transfer method that allows potentially smaller transferred chip sizes on chips than can be reliably handled by standard pick-and-place equipment.

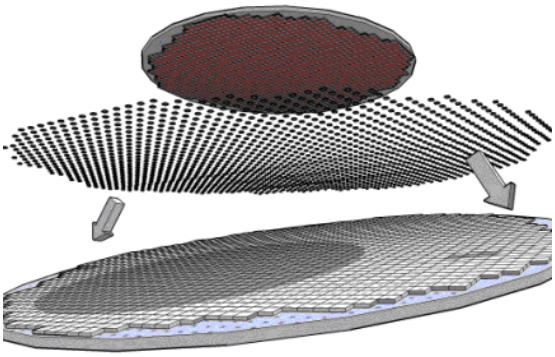

Figure 1b: The novel transfer approach using stretchable transfer substrates that enables simultaneous mapping of all dies in parallel onto larger substrates.

The problem related to difference in wafer size is addressed in this work by making use of stretchable transfer substrates that can bridge the gap and enable wafer-level device transfers between different wafer sizes as shown in figure 1a and b.

This new approach is applicable to wafer-level integration of devices that suffer from incompatible wafer or chip-sizes, including micro-lenses, photonic components and MEMS.

FABRICATION

Figure 3 shows the most important steps in the process chain. The new concept was demonstrated by dicing a 300 μm thick 100 mm diameter silicon wafer on an expandable UV release dice tape (Nitto Denko ELEP UE-111AJ) into approximately 30000 chips, with a size of 460x460 μm^2, using a die saw. This resulted in approximately 40 μm dice lines between the chips. A matrix expander (ULTRON UH-130) expanded the tape by stretching it out so that the separation between the dies increased from 40 μm to approximately 330 μm thus expanding the 100 mm wafer format to a 200 mm diameter wafer format (figure 2). The expanded tape was fastened to a plastic carrier ring to avoid relaxation of the dice tape in the further handling.

The next step consisted of transferring the expanded chip array onto a 200 mm temporary silicon handle wafer covered with thermal release tape. The bonded stack was then illuminated by UV-light to remove the dice

tape. This step was made to simplify further wafer handling in the following wafer bonding step using a Suss CB8 substrate-bonder.

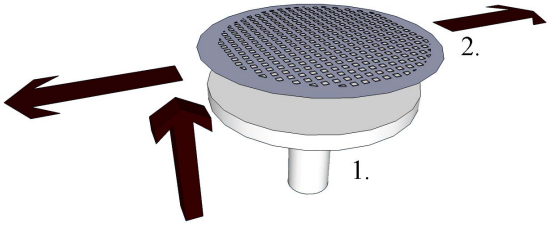

Figure 2: The chips are separated using a matrix expander. A chuck (1) is moving upwards towards the tape. The fixed tape is stretched out and expands to the sides (2).

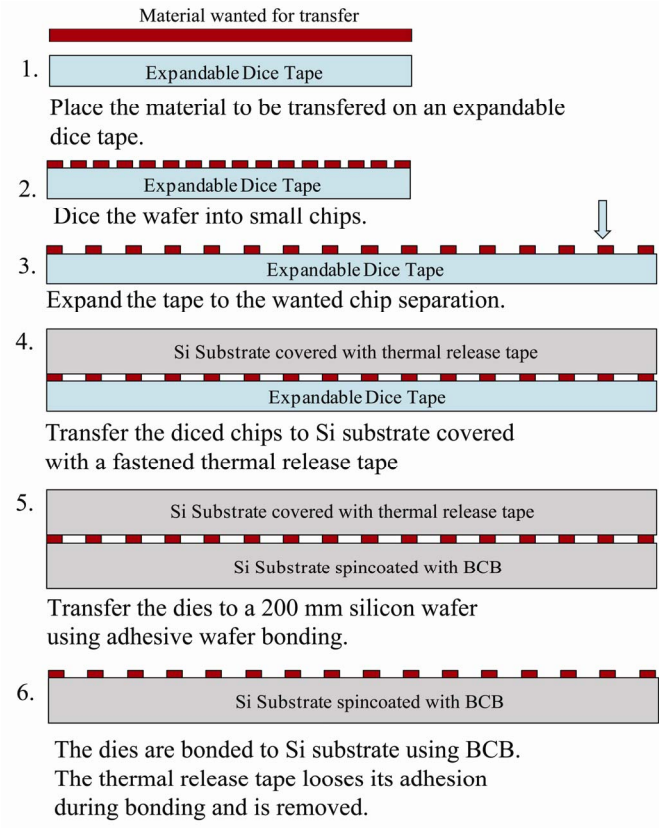

Figure 3: Process sequence for fabrication. In this work we expanded a 100 mm diameter Si wafer to a 200 mm diameter format to demonstrate the concept.

A 200 mm silicon wafer with a 2.6 µm thick spin coated layer of BCB (3022-46) was prepared as the final target substrate. The wafers were bonded in a wafer bonder at a temperature of 160°C, hold time of 20 minutes, and 5kN of applied bond force. Thereafter the thermal release tape was removed from the dies that are now transferred to the BCB-covered wafer. A second bond step was performed in the wafer bonder for an additional 30 min hold time at 250°C and a 2 kN applied bond force to fully cure the BCB adhesive. Both steps were done in a 500 mbar atmospheric pressure. Figure 4a shows an expanded and diced wafer while images of transferred dies can be seen in figure 4b and 4c.

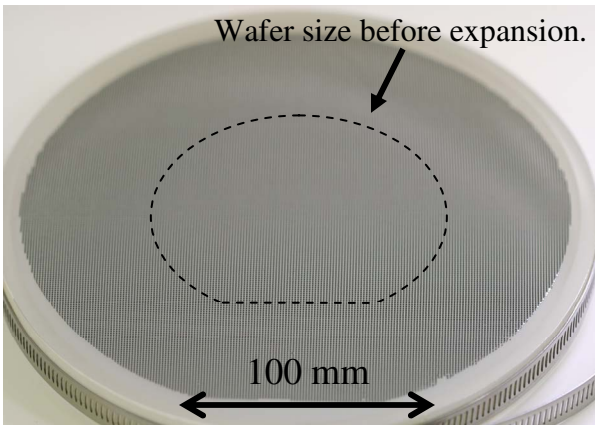

Figure 4a: Picture of an expanded and diced 100 mm wafer on an expandable UV release dice tape. Approximately 30000 chips have been diced in this example (chip size: 460x460 µm^2).

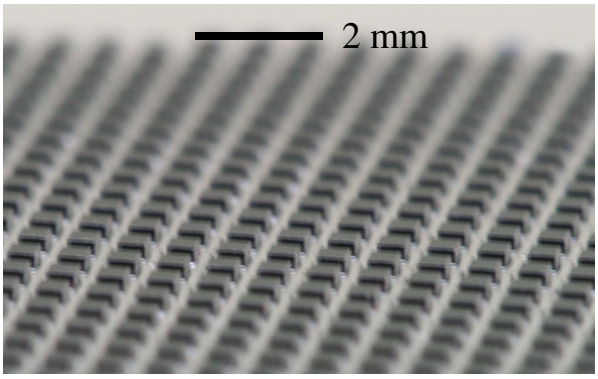

Figure 4b: Picture of chips separated by the matrix expansion and transferred to a 200 mm temporary Si handle wafer covered with thermal release tape.

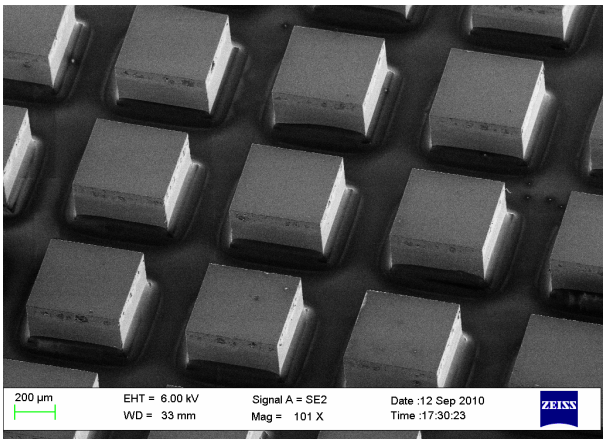

Figure 4c: SEM picture of transferred dies bonded to a 200 mm Si wafer using BCB adhesive wafer bonding.

EVALUATION

Distances between transferred dies on the target wafer were measured using a microscope with an automated XY-stage capable of taking digital high resolution microscopic pictures, followed by image analysis. The microscope stage kept track of the wafer position for each image. Adjustments of the microscope filters created images in which the surfaces of the dies had a lighter color than the darker color of the areas between the dies. The pictures were taken in such a way that crosses were formed by the edges of four different chips (figure 5a).

Figure 5a: Microscope picture before conversion into black and white.

Figure 5b: Same picture as in 5a after conversion into black and white. The distances in X and Y was measured to be 679 pixels and 671 pixels respectively, using a MATLAB script.

The first step of the image analysis converted the pictures into grayscale. Each pixel was then compared with its neighboring pixels and given the average value to avoid having individual pixels with a different coloring than its immediate surroundings. The images were converted to black and white (figure 5b) and a MATLAB-script counted the number of black pixels between the dies. Each pixel was measured to correspond with a 514 nm distance in the images.

Converted and measured images were compared with the original images. Comparisons of manually measured values in randomly picked images were made with the same pictures evaluated with the MATLAB script. This gave an error of evaluation of typically less than 10 μm.

RESULTS

Pictures were taken for every 10 mm over the whole wafer surface with transferred dies. This resulted in a total of 201 images. Each image was evaluated and the die separations in both X and Y direction was determined. Figure 6 is a contour plot of the evaluated distances between the dies at different placements over the wafer. A radial symmetry can be seen in figure 6 where a slightly larger expansion can be seen in the middle of the wafer as compared with the wafer sides.

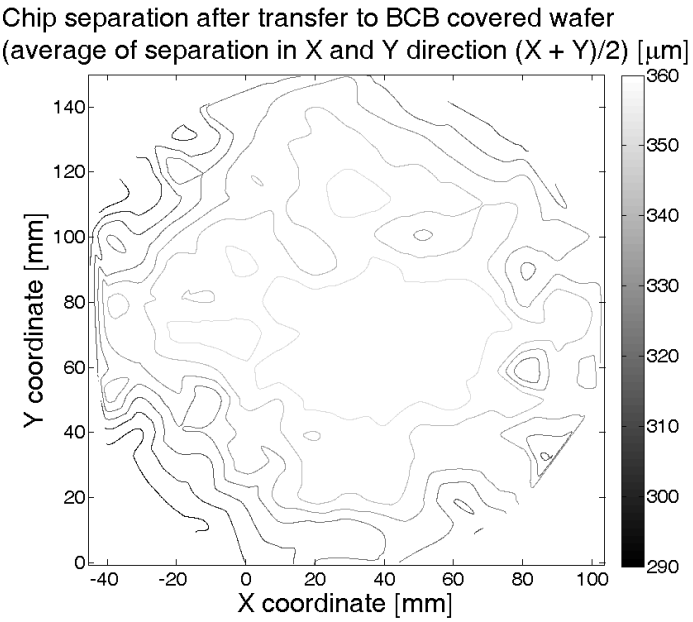

Figure 6: Contour plot over separation distances between dies as a function of their placement on the wafer.

This radial symmetry is shown more clearly in figure 7 were measurements were made from the center point of the wafer. Measurements were made at radial 10 mm steps from the center and the average separation for all dies at that circular perimeter was measured. The standard deviation can be seen to increase with increased distance from the center point of the wafer and is largest at the edge of the wafer. A slight curvature of the die rows was also observed. This effect can be explained by the separation of square matrices of dies with a circular chuck in the matrix expander.

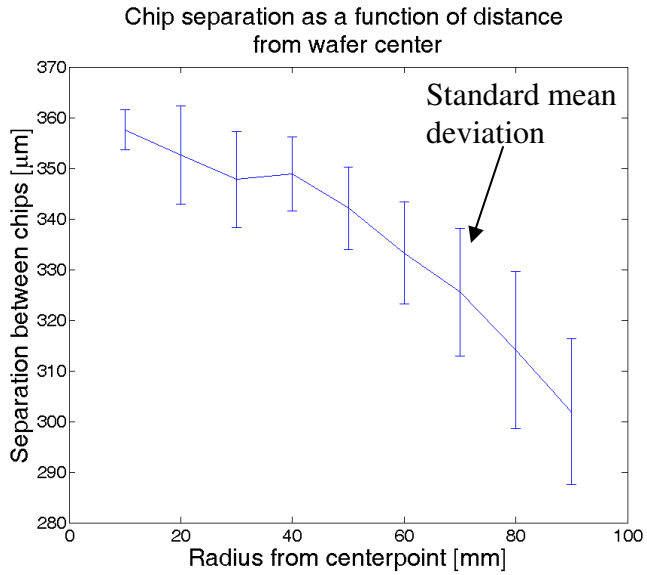

Figure 7: Separation between dies as a function of distance from the center point. A radial symmetry is present. The chip separation is within one standard deviation from the center to about 80 mm from the center point.

Figure 8 shows histograms for the separation distances in X and Y directions. The mean separation distances of the transferred chip were 335±22 μm in the X and 328±19 μm in the Y direction. The maximum difference between separation distances in the measured data was 92 μm. The yield of the entire transfer process is currently about 98%. We believe that the process yield can be further improved by process optimizations.

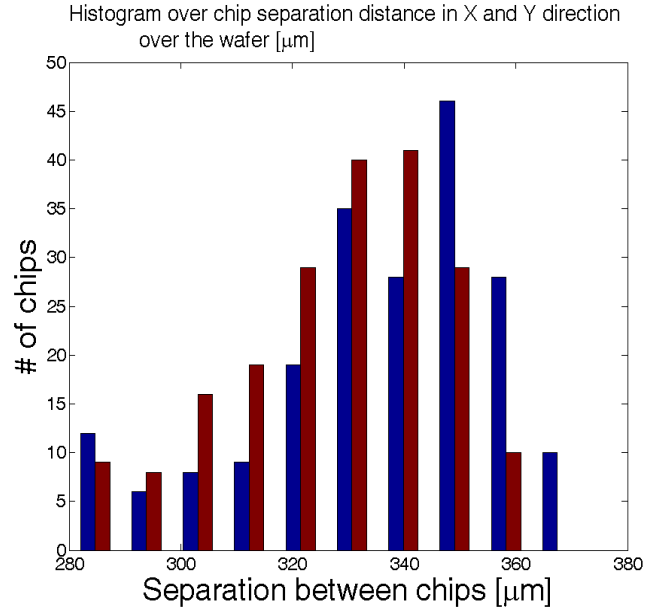

Figure 8: Histogram of separation between dies for dies BCB wafer bonded to a silicon carrier wafer.

CONCLUSIONS

A novel method that can map dies on a smaller wafer onto a larger wafer by transferring expanded chip arrays to larger substrates has been demonstrated. This method can potentially enable cost-efficient heterogeneous integration of MEMS or photonic devices onto large substrates, such as onto standard CMOS wafers.

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