A SIMPLE METHOD FOR EFFECTIVELY RESTRAIN ELECTROCHEMICAL CORROSION OF POLYCRYSTALLINE SILICON BY HF-BASED SOLUTIONS

*J. Xie[1, 2], Y.F. Liu[1, 2], M.L. Zhang[1], J.L. Yang[1, 2, *], and F.H. Yang[1]*
[1]Institute of Semiconductors, Chinese Academy of Sciences, Beijing, P. R. CHINA
[2]State Key Laboratory of Transducer Technology, Shanghai, P. R. CHINA

ABSTRACT

A simple method is described to protect polycrystalline silicon (polysilicon) from electrochemical corrosion which often happens when the Micro-Electro-Mechanical systems (MEMS) device is released in HF-based solutions, especially when the device contains noble metal. We propose to employ a photoresist (PR) layer to cover the noble metal layer, which electrically contacts with the underlying polysilicon layer. This PR cover can prevent HF-based solution from diffusing through and arriving at the surface of the noble metal, thus cut off the electrical current of the electrochemical corrosion and thus protect the polysilicon layer intact. The polysilicon layer can be protected longer than 80 min in 49% HF solutions by 3 μm thick AZ6130 photoresist. This approach is not only simple, effective, IC technology compatible, and suitable for batch fabrication, but also can significantly improve the performance of MEMS devices.

INTRODUCTION

In the past two more decades, the microfabrication technologies were rapidly developed and a number of mature micromaching techniques which are compatible with integrated circuit (IC) fabrication process had been applied to mass production. However, for microfabrication of Micro-Electro-Mechanical Systems (MEMS) devices in volume, there are still many open questions demanding reliable and cost-effective micromaching techniques. For example, electrochemical corrosion of polycrystalline silicon (polysilicon) by HF-based solutions is a long-standing issue in polysilicon MEMS field, thus is also the major concern of this work.

Surface micromaching technique, which is based on depositing and patterning thin films (e.g., polysilicon, silicon nitride, or metallic thin film) over a sacrificial layer (usually silicon oxide SiO_2), is commonly employed to fabricate the polysilicon MEMS devices. When the polysilicon devices containing noble metals are etched in HF-based solutions, the polysilicon is electrochemically corroded due to its lower electrochemical potential than that of noble metal [1]. This corrosion seriously degrades the mechanical and electrical performance of MEMS devices, e.g., increasing the resistivity of structural layer, declining its Young's modulus, changing the stress gradient, etc., in the end the device reliabilities are deteriorated [2]-[4].

Currently, several approaches have been reported to avoid electrochemical corrosion of polysilicon during SiO_2 etching in the HF-based solutions. For example, SiO_2 is etched before metallization of the devices [5], or the release holes on the structure layer are designed to reduce the etching time, and increasing the area ratio of polysilicon to noble metal [6] or adding redox buffering agents in the etchant solutions are also helpful solutions for reducing electrochemical corrosion [7], [8]. However, either these approaches require change of device structures at the expense of performance or complicate fabrication process, finally increase the cost and are not applicable to batch fabrication. Herein, a simple method is proposed to effectively prevent electrochemical corrosion of polysilicon by HF-based solutions, which is compatible with IC technology and suitable for large-scale manufacture of MEMS devices.

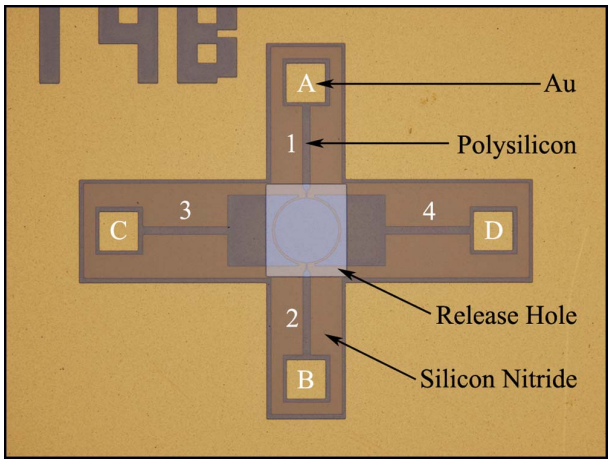

Figure 1: A PR film covers the whole surface of the test device except the release hole.

EXPERIMENTS

The test devices are designed and fabricated in order to get deep insight into electrochemical corrosion and its influence on the electrical properties of polysilicon. The main fabrication steps of the test devices were introduced in [7]. As shown in Figure 1, the test device consists of a disk and four electrical transmission lines (labeled as 1, 2, 3, and 4 in Figure 1) made of polysilicon and having the same dimensions of $280 \times 20 \times 0.3$ μm^3. Transmission lines 1 and 2 are connected with the disk and are in ohmic contact with gold pads A and B, respectively. The disk is released via etching the underlying SiO_2 sacrificial layer. The release time depends on the disk diameter, for example, it takes 72 min to completely remove the SiO_2 sacrificial layer underneath the disk of 160 μm in diameter by the 49% HF solution. During the wet etching process, the polysilicon structure was electrochemically attacked shortly after it was barely exposed to the HF solution and its resistivities rapidly increased.

A 3 μm thick AZ6130 photoresist (PR) film was employed to cover the whole test device except a release hole to protect polysilicon during the wet etching in the 49% HF solutions, as shown in Figure 1. A special post-baking process was performed that the PR film was baked in oven at step-up temperatures of 70 °C, 90 °C, and 110 °C for 20 min respectively. Then the specimen was taken out from the oven and naturally cooled down. In order to better understand how severely polysilicon is attacked, the change of polysilicon resistivity was monitored by measuring the resistance between the pads A and B through a probe station and a digital multimeter before and after the etching process. The contact resistance between the probe and the metal pad is about 2 Ω and independence of immersion time in HF solution, much smaller than the resistance between the pads A and B (20 kΩ–200 MΩ, or even larger), therefore the measurement error caused by the contact resistance is negligible.

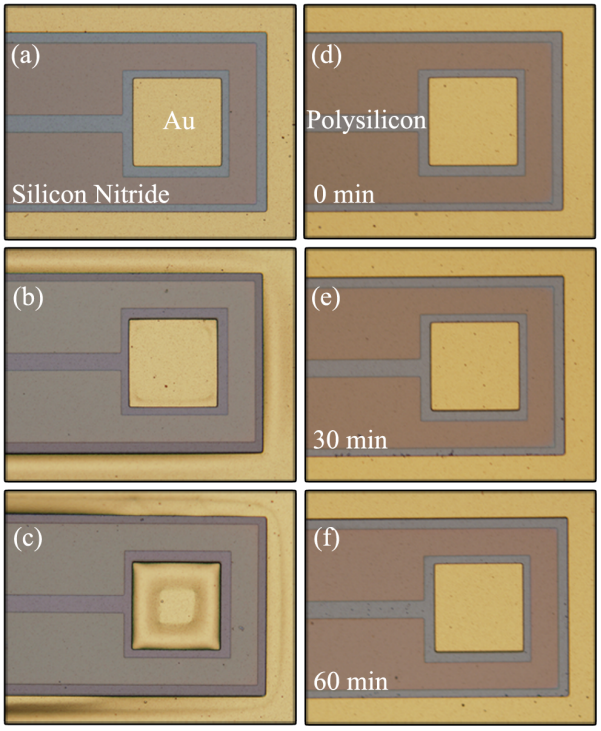

Figure 2: Optical micrographs of polysilicon transmission lines and gold pads before and after the test devices were etched in 49% HF solutions for 30 min and 60 min, respectively. Figure 2 (a – c): the devices without a PR cover; Figure 2 (d –f): the devices with a PR protecting film.

RESULTS AND DISCUSSION

In order to validate the proposed method, two types of test devices were prepared: one with a commercial PR AZ6130 film of 3 μm thick on top of the device surface and another without a PR layer. Figure 2 gives the optical microscopic pictures of the polysilicon transmission lines and gold pads before and after the test devices were immersed in 49% HF solutions for 30 min and 60 min, respectively. Figure 2(a) shows the test device without a PR layer, before etched with 49% HF solution. Whereas, Figures 2(b) and 2(c) show the same structures which were immersed into 49% HF solution for 30min and 60min, respectively. It can be seen that the transmission line and the polysilicon near the gold pad is electrochemically corroded and discolored in the 49% HF solution, and the gold pads gradually delaminate from the edge to the center of the electrodes. The gold pad has no visible warping at the edge after staying in 49% HF solution for 30 min (Figure 2(b)). But after 60 min in 49% HF solution, the gold pad completely peels off from polysilicon at the edge area, as shown in Figure 2(c). However, when we repeated the same etching processes on the test devices covered by a commercial PR AZ6130 film, which is post-baked in oven at step-up temperatures of 70 °C, 90 °C, and 110 °C for 20 min, respectively, different results were observed, as shown in Figures 2(d)-2(f). Delamination of the gold pad does not happen even after etching SiO_2 for 60 min in the same 49% HF solution. In addition, discoloration of the polysilicon transmission line was not observed.

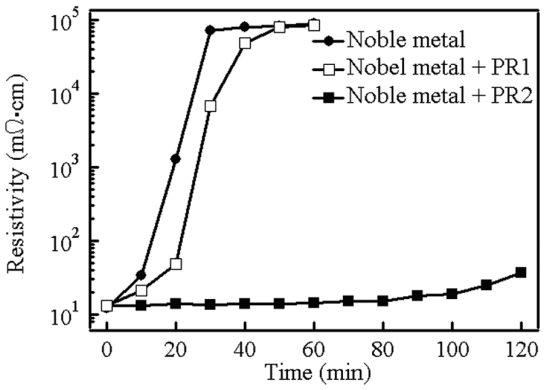

Figure 3: The resistivities of polysilicon versus SiO_2 etching time in 49% HF solutions for different test devices: noble metal without the PR cover; with the PR AZ6130 cover which was post-baked at 110 ℃ for 30 min (PR1); with the PR AZ6130 cover which was post-baked at step-up temperature of 70 ℃, 90 ℃, and 110 ℃ for 20 min, respectively (PR2).

The electrical properties of test devices before and after etching in 49% HF solutions were systematically investigated in order to test the feasibility of this approach. Three kinds of test devices were immersed in 49% HF solutions for various time and the resistivities of polysilicon between the gold pads A and B in these devices were measured. As shown in Figure 3, the polysilicon resistivities in the devices without a PR layer increased from 15 mΩ·cm to 10^5 mΩ·cm (four orders of magnitude up) after 30 min wet etching in HF solutions due to the electrochemical corrosion of polysilicon. For the devices with a PR film which was post-baked at 110 °C for 30 min (PR1), their resistivities also increased from 15 mΩ·cm to 10^4 mΩ·cm within 30 min immersion in the 49% HF solution, although the degradation rate decreased. The resistivities of the polysilicon layer kept

unchanged even after staying in 49% HF solution for 80 min when the PR cover of the test device was post-baked at step-up temperatures of 70 °C, 90 °C, and 110 °C for 20 min, respectively (PR2). Additional 40 min etching results in the resistivity rising from 15 mΩ·cm to 30 mΩ·cm. Above all, the post-baking process is vital for the PR to successfully function as a protecting layer.

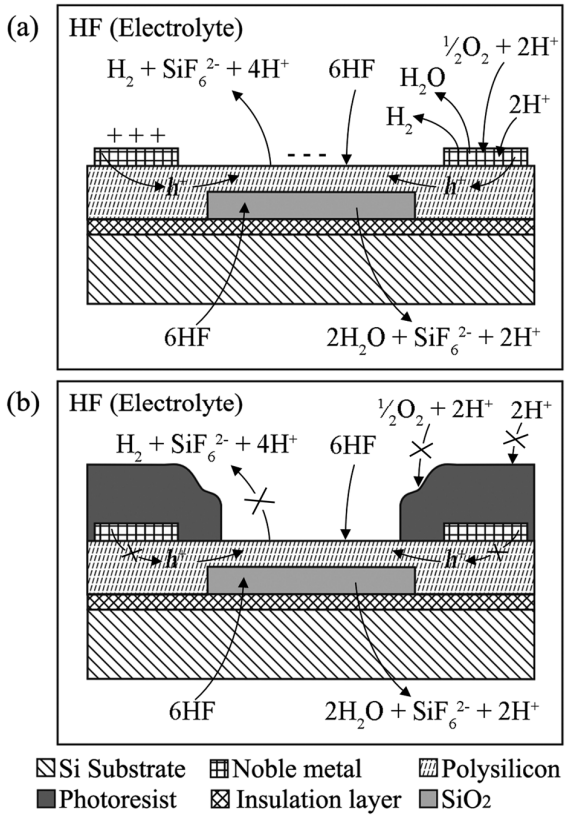

Figure 4: Schematic illustrations of (a) galvanic corrosion of the structural polysilicon by the HF-based solutions and (b) the principle for restraining electrochemical corrosion of the polysilicon by coating the noble metal with a PR layer.

For exploring the potential application of this method, a deep understanding of its working principle is crucial. Figure 4(a) gives a schematic illustration of electrochemical corrosion process of the polysilicon layer of the test device in HF-based solutions. The etching is driven by the electrochemical potential difference between the polysilicon and the electrically-coupled noble metal (e.g., Au) in an electrolytic solution (e.g., 49% HF solution). A galvanic cell is formed in the solution with polysilicon as an anode and the noble metals as a cathode. Galvanic reaction takes place when an oxidizing agent (e.g., O_2) in the solution is reduced at the noble metal surface, which generates an electrical current and results in oxidation of the polysilicon. Anodic corrosion reaction of polysilicon in HF-based solution is described as follows, where h^+ is a valence band hole donated by the noble metal [9]:

$$Si + 2H^+ + 2h^+ \rightarrow Si^{4+} + H_2 \quad (1a)$$
$$Si^{4+} + 6HF \rightarrow SiF_6^{2-} + 6H^+ \quad (1b)$$

Meanwhile, on the surface of the noble metals, the electrons reduce the dissolved O_2 and H^+ via the following reaction [10]:

$$O_2 + 4H^+ + 4e^- \rightarrow 2H_2O \quad (2a)$$
$$2H^+ + 2e^- \rightarrow H_2 \quad (2b)$$

The working principle of the approach provided by this paper to restrain the electrochemical corrosion of polysilicon is depicted in Figure 4(b). Photoresist (PR) is spin-coated and patterned to cover the whole surface of the test device except the release hole, as shown in Figure 1. Thus, the noble metal is covered by this PR film. The PR film could significantly prevent the HF-based solution from diffusing through and arriving at the surface of the noble metal, the reduction reaction (Equation 2(a) and 2(b)) of the oxidizing agent in the solution will not occur. As a result, no electrical current (h^+) is injected into anodic polysilicon to induce the electrochemical corrosion. Two factors are crucial in this method for successful protection of polysilicon. Firstly, the selected PR film does not dissolve in HF-based solution and is able to maintain good adhesion with the device surface in HF-based solution for long time. Secondly, the porosity of the PR film should be reduced by refining the PR post-baking process, thus the PR film could significantly prevent the HF-based solution from diffusing through and arriving at the surface of the noble metal, and is able to hinder formation of the galvanic cell and electrochemical corrosion of polysilicon.

The performance of several commercial PRs is studied in this paper. On the one hand, the adhesion of PR is determined by its own properties. For example, the PR AZ 6130 and S 9912 coated on Si substrate can survive and not peel off from the substrate in 49% HF solution for 120 min, while the PR L 300 and AZ 5200 NJ peel from Si substrate after immersed in 49% HF for only 10 min. On the other hand, the adhesion of PR also strongly depends on the stability of the PR-covered substrate material in HF-based solution. For substrate topped by materials etched rapidly with the 49% HF, such as SiO_2, the PR peels off after wet etching for 5 min. The test structures used in this paper nevertheless have the polysilicon, silicon nitride or gold as the top layers and covered by PR except the release hole. Good adhesion with the PR can be maintained, since polysilicon, silicon nitride and gold is etched by HF solution very slowly. No delamination of AZ 6130 or S 9912 was observed after etching in 49% HF for 120 min.

The molecule chains of PR have weak interaction forces, and the post-bake is required to improve the thermal, chemical, and physical stability of PR as well as to enhance adhesion between the PR and the substrate. Normally post-bake is performed at one targeting temperature (such as 110 °C) in oven for a period. During baking at high temperature, the thermal mismatch between the PR and

substrate exists, and the evaporation rate of the volatile composites on the PR surface is different from that in the inner area of the PR, therefore the micro-cracks often appear in the PR after baking, the thicker the PR, the more apt it is to formation of the micro-cracks. These micro-cracks are not visible even under an optical microscope, but can be penetrated by etchant in wet etching process, thus the underneath layer will react with the etchant. By post-bake at step-up temperatures, the porosity of PR could be reduced, and the PR film can effectively hinder the etchant from reaching the surface of noble metal and avoid formation of the galvanic cell, thus polysilicon is well protected from electrochemical corrosion in HF-based solutions.

CONCLUSIONS

A simple and effective approach is presented to eliminate electrochemical corrosion of the polysilicon layer in MEMS devices during SiO_2 wet etching. This method employs a PR film as the protection layer. By refining the PR post-baking process, e.g., baking at step-up temperatures instead of at one targeting temperature, the porosity of the PR can be minimized. Thus the HF-based etchant cannot penetrate the PR layer and contact with the noble metal, the electrical current of the galvanic cell is cut off, and the electrochemical corrosion of polysilicon is effectively restrained.

In this work, a commercial PR AZ6130 film of 3 μm thick was spin-coated and patterned to cover the whole surface of the test device except the release hole, and post-baked at 70 °C, 90 °C and 110 °C for 20 min, respectively. The devices survived without any electrical degradation in 49% HF solution for 80 min. This method provides a perfect solution for electrochemical corrosion of polysilicon by HF-based solutions, a long-standing issue in polysilicon MEMS field, it has the advantages of simplicity, low cost, and compatibility with IC technology, therefore is applicable to batch fabrication and will significantly enhance the performance of MEMS/NEMS devices.

ACKNOWLEDGEMENT

This work is supported by the MOST of China (2009CB320305 and 2011CB933102).

REFERENCES

[1] M. Huh, Y. Yu, H. Kahn, J. H. Payer, A. H. Heuer, “Galvanic corrosion during processing of polysilicon microelectromechanical systems”, *J. Electrochem. Soc.*, vol. 153, no.7, pp. G644-G649, May 2006.

[2] D. C. Miller, W. L. Hughes, Z. L. Wang, K. Gall, C. R. Stoldt, “Mechanical effects of galvanic corrosion on structural polysilicon”, *J. Microelectromech. Syst.*, vol. 16, no. 1, pp. 87-101, Feb. 2007.

[3] O. N. Pierron, D. D. Macdonald, C. L. Muhlstein, “Galvanic effects in Si-based microelectromechanical systems: Thick oxide formation and its implications for fatigue reliability”, *Appl. Phys. Lett.*, vol. 86, no. 4, pp. 211 919-1-211 919-3, May 2005.

[4] D. C. Miller, B. L. Boyce, K. Gall, C. R. Stoldt, “Galvanic corrosion induced degredation of tensile properties in micromachined polycrystalline silicon”, *Appl. Phys. Lett.*, vol. 90, no. 19, pp. 191 902-1-191 902-3, May 2007.

[5] C. T.-C. Nguyen, “Micromachining technologies for miniaturized communication devices”, in *Proc. SPIE*, 1998, pp. 24-38.

[6] A. Syed, L. Mu, M. Shavezipur, P. Nieva, “Eliminating the galvanic effect for microdevices fabricated with PolyMUMPs®”, in *Proc. MNRC*, 2008, pp. 197-200.

[7] Y. F. Liu, J. Xie, M. L. Zhang, J. L. Yang, F. H. Yang, “An effective approach for restraining galvanic corrosion of polycrystalline silicon by hydrofluoric acid-based solutions”, *J. Microelectromech. Syst.*, in revision.

[8] M. G. Hankins, “Redox buffered hydrofluoric acid etchant for the reduction of galvanic attack during release etching of MEMS devices having noble material films”, U. S. Patent 7 597 819 B1, Oct. 6, 2009.

[9] X. H. Xia, C. M. A. Ashruf, P. J. French, J. J. Kelly, “Galvanic cell formation in silicon/metal contacts: The effect on silicon surface morphology”, *Chem. Mater*, vol. 12, no. 6, pp. 1671-1678, May 2000.

[10] H. Kahn, C. Deeb, I. Chasiotis, A. H. Heuer, “Anodic oxidation during MEMS processing of silicon and polysilicon: Native oxides can be thicker than you think”, *J. Microelectromech. Syst.*, vol. 14, no. 5, pp. 914-923, Oct. 2005.