A SINGLE LITHOGRAPHY VERTICAL NEMS SWITCH

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ABSTRACT

We demonstrate the use of torsion in nanorelays to achieve low voltages, high speeds, single lithography step construction, and a form useful for configurability and electronic design enhancements in three-dimensional integrated implementations. The combined bending and torsion of self-aligned nanopillars facilitates the first top-down fabricated vertical three terminal nanoscale relay. Experimental devices, even at 500 nm features, operate at ~10 V and µs. Scaling suggests operation down to unit volts.

INTRODUCTION

Nanorelays are potentially relevant devices for low standby power and energy exchanging computing [1,2] and for dynamic or non-volatile configurability. To date, nanorelay implementations have used processes that combine single crystal materials and layered structures, thus permitting ultra-small gaps needed for actuation. This allows electronics compatible voltages to be achieved at the expense of complex processes with high temperature deposition and selective removals.

Although recent planar structures based on CMOS-compatible top-down approaches have exhibited promising switching behavior [3,4], they require either more real-estate or more aggressive scaling to achieve the high-aspect ratios necessary for low voltage operation. Vertical switches employing growth approaches based on nanotubes [5] have also been successfully demonstrated at low voltages with small device footprint. However, they require elaborate fabrication processes, use exotic materials and suffer from substantial variability in placement and size. These process variations significantly limit the functionality and performance of CNT-NEMS based switches in circuit configurations [6]. We show here an appealing alternative, leveraging torsion, that has the potential to alleviate the need of single crystal deposition processes, and that can also be used in interposers for 3D integrated programmability. Using a single step of optical lithography, the device combines the benefits of a top down approach with the area savings of a vertical structure to achieve self-aligned nanopillars with aspect ratios up to 100:1.

DESIGN

Figure 1(a) shows vertical device which uses a combination of bending and torsion to physically connect S and D electrodes via a "channel". With S/D grounded, C_{SC} and C_{DC} are in parallel with C_{BC} for a total equivalent capacitance C_{PC}. Therefore, the gate to "channel" capacitance (C_{GC}) in series with C_{PC} form a voltage divider which determines the potential of C, and the electrostatic force on the channel is proportional to V_{GC}^2. Electrostatic

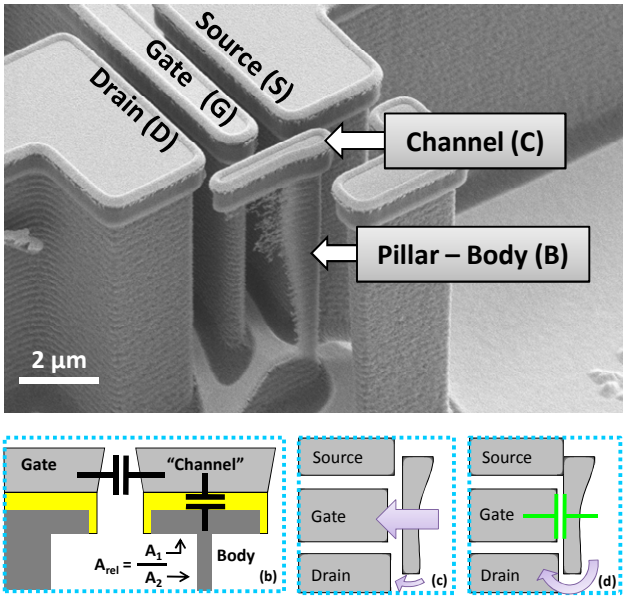

Figure 1: (a) SEM micrograph of vertical torsion based NEMS switch. (b) Cross-sectional schematic of device as seen perpendicular to channel. Voltage of island determined by capacitor divider. (c) Top view schematic of device. Before initial pull-in, device operates as voltage divider, with actuation dominated by bending of pillar. (d) After pull-in, device simplifies to a parallel plate configuration, and actuation is primarily torsional.

actuation of the "channel" results primarily in bending of the pillar until pull-in occurs. Torsion allows self-correction for S/D offsets arising from line edge roughness or metal grain size. This is critical to achieving reproducible contacts in small geometries, an issue with conventional nanorelays. A first implementation of this device incorporated a wide nanoribbon rather than a nanopillar. The torsional rigidity of the ribbon prevented the structure from twisting or rotating, thereby inhibiting physical contact of the channel to both the Source and Drain. By reducing the mechanical element to a pillar, and offsetting its position to the Source side, torsion was introduced into the structure.

Initial pull-in converts the device to a simple parallel plate configuration (Figure 1(d)) with new gap size determined by a predefined offset between a recessed gate and S/D, ~100nm for current device. The recessed gate prevents gate–channel contact. *This "new" gap is much smaller, thereby strongly enhancing torque on the channel.* The device achieves an "ON" state when torsion overcomes the small S/D offset, establishing a low resistance metal to metal contact.

FABRICATION

The device is fabricated with a single step patterning which precisely places source, drain and gate perfectly aligned with the nanopillar. Devices employ a variety of tricks to decrease the critical dimensions (Figure 2). The pillar thickness can be controllably reduced using oxidation and wet etching for silicon based devices. Alternatively, stiction-free processing can be achieved using an isotropic SF_6/O_2 etch. A key feature of the fabrication is the thin Si_3N_4 insulating spacer. This layer serves as a diffusion barrier for the oxidation method. It also endures an SF_6/O_2 etch, thereby giving the device its unique flower pedestal form. The Si_3N_4 enables low voltage operation by making possible independent optimization of gap and pillar sizes. Therefore, pillars can be reduced while maintaining small gap sizes. Figure 3 shows the design for a torsion based device. Isotropic processing of a non-uniform channel profile allows pillar formation, as opposed to a ribbon-type structure. Gaps were a conservative 200 – 350nm for our devices given the sensitivity of our optical measurement system, and the need for substantial signal level arising from pillar oscillation. Also, starting with larger gaps enables deeper etching for taller pillars and reduces the likelihood of stiction during wet processing. Gap reduction is easily achievable by longer blanket evaporation of metal in the final process step. Electrical isolation is maintained between the body and the other electrodes by virtue of the silicon undercut beneath the Si_3N_4.

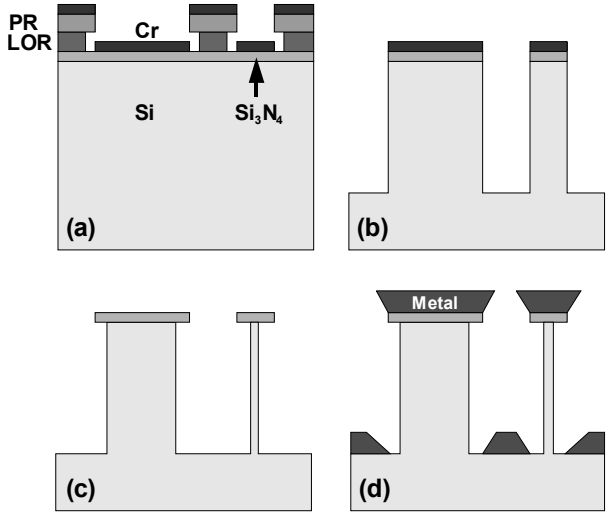

Figure 2: Single lithography process for vertical nems switch. (a) Liftoff process for self-aligned nanopillar fabrication. (b) Deep RIE Bosch process using Cr etch mask. (c) Reduction of silicon pillar diameter. (d) Decrease gap size using blanket metal evaporation.

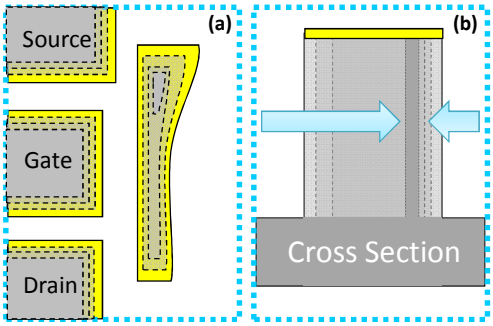

Figure 3: (a) Top view of device undergoing isotropic etching to remove silicon under majority of channel. (b) Cross-sectional view parallel with channel. Demonstrates pillar formation due to a non-uniform channel profile.

RESULTS

Operation of a typical device at 10V in air is shown in Figure 4. It has a gap of ~230nm measured from the S/D, and non-uniform *pillar thickness* ~130nm at the bottom and ~180nm at the top. Figure 5 shows the measured device after pull-in is achieved. In Figure 6, another device demonstrates pull-in at ~19.5V. However, the same device consistently turns on at ~15.5V during repeated sweeps. An SEM image confirms that the "channel" is pinned to the D, and a small gap remains between the S and "channel". The operation voltage in the first sweep is dominated by $V_{pull\text{-}in}$ due to bending of the pillar. Subsequent sweeps show torsion based actuation. Although the structure is more resistive to torsion than to bending, improved electrostatics after initial pull-in produce lower operation voltages with torsion.

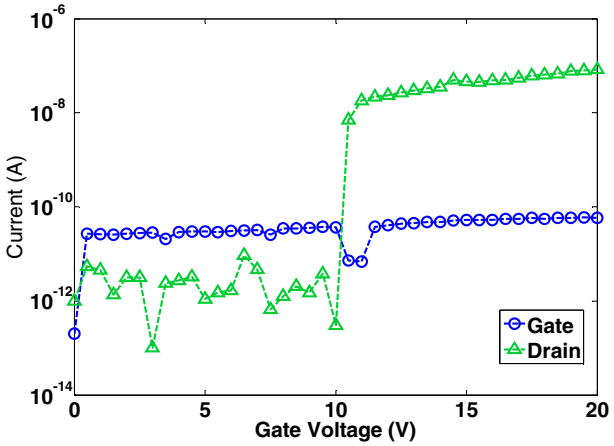

Figure 4: Measured I_{DS}—V_G characteristics with V_D = 0.1 V, and V_S = V_B = 0 V. Abrupt switching can be seen for V_G = 10 V. Gap ~230 nm measured from the S/D, and non-uniform pillar thickness ~130 nm at the bottom and ~230nm at the top.

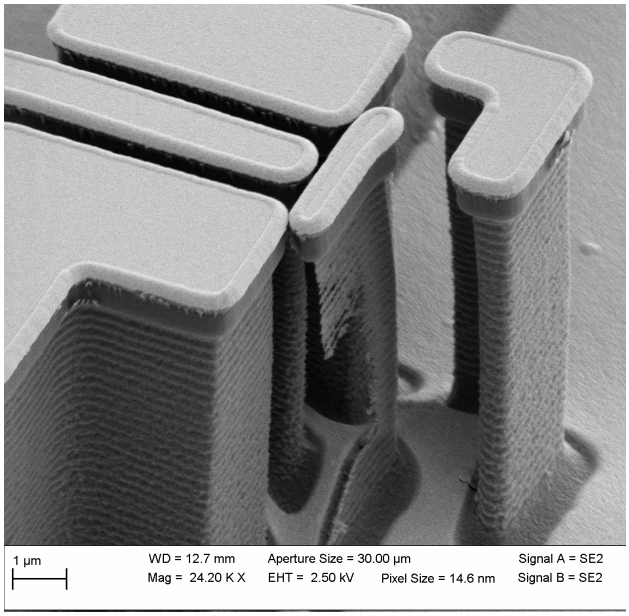

Figure 5: SEM micrograph of 10V device after pull-in achieved. Channel formed permanent contact with Source and Drain during actuation. Gate remained electrically isolated from Channel.

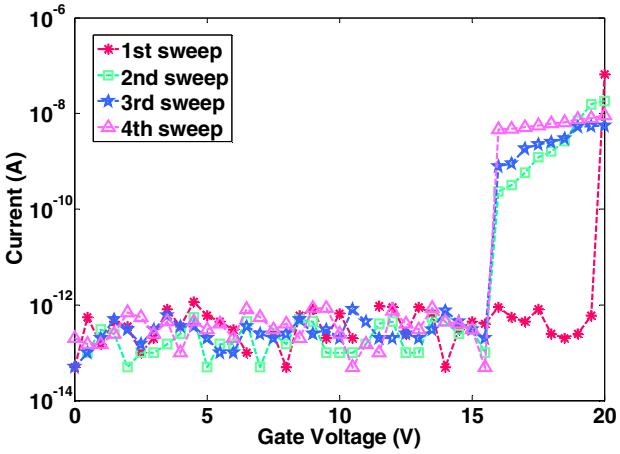

Figure 6: Measured I_{DS}—V_G characteristics with V_D = 0.1 V, and V_S = V_B = 0 V. Device shows initial pull-in voltage of 19.5 V. Repeated sweeps show 15.5 V operation.

We extract the mechanical properties using an optical knife-edge technique in vacuum [7]. By employing an objective lens to focus a HeNe laser (λ = 632nm) on the edge of a pillar, reflected power from a diffraction limited spot is modulated by the nanopillar's movement. Electrical excitation gives rise to the mechanical oscillation of our device. This method was used to ascertain the modes of our torsion based device. Figure 7 shows f_o ~331 kHz. Figure 8 shows the torsional mode with a measured frequency of ~2.6 MHz. Given the complexity of a non-uniform pillar, these values were verified using COMSOL 3D FEM. For a simulated structure, f_o ~370 kHz with the torsional mode at ~3 MHz. Switching speeds are estimated to be on the order of $1/f_o$.

Resonances for ribbon-type devices were also detected with f_o ~310 kHz to 1.5 MHz, for devices with *pillar thickness* ~90nm to 200 nm, and a constant *pillar height* of 9 µm. The resonance data points to the characteristic decrease in Young's Modulus (E) of silicon at the nanoscale [8], with E_{eff} ~70 GPa for *thickness* ~90 nm. As the surface area to volume ratio increases for small devices, surface stresses reduce the effective Young's modulus of nanowires and nanopillars. We verified this effect using the absolute value of the resonant frequency to extract the Young's Modulus of silicon. Ribbon-type devices with uniform rectangular cross-section lend themselves to easy analysis. However, simulations of torsion based devices with non-uniform cross-section do not include a thickness dependent Young's Modulus.

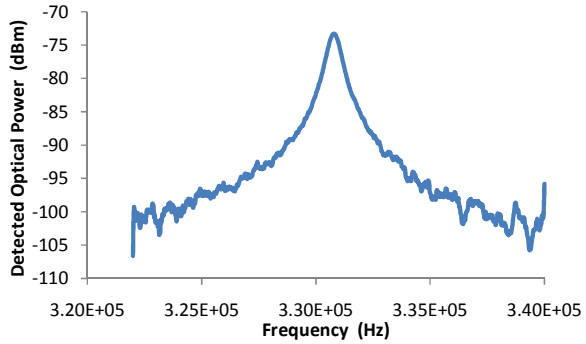

Figure 7: Fundamental mode of torsion structure. Height ~9.5µm, non-uniform pillar thickness ~150nm at the bottom and ~230nm at the top, varying pillar width of ~475nm at the bottom to ~950nm at the top, channel width of ~3.6 µm with ~500nm of metal atop.

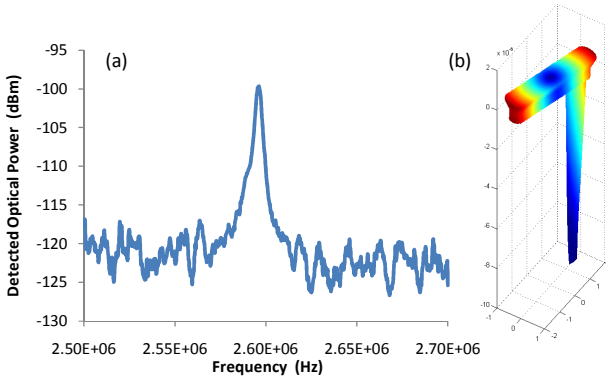

Figure 8: (a) Torsional mode of structure from Figure 5. Measured frequency of ~2.6 MHz. (b) 3D FEM simulated torsional mode of structure with non-uniform pillar thickness and width. Simulation verifies the torsional mode to be at ~3 MHz.

We also used FEM analysis to enhance the electrostatic force on the island. The electrical force can be increased by optimizing the ratio C_{GC} /C_{PC}, but that constrains the reduction of the mechanical stiffness. *Significant reduction in $V_{Pull\text{-}in}$ is achievable if the area of capacitive coupling between the pillar and the channel can be increased by a factor A_{rel} over the pillar cross section*, and by accomplishing this, we optimize the mechanical stiffness and electrostatic coupling independently. We increased A_{rel} by retaining a silicon layer underneath the channel (Figure 1(b)) and protected it from etching using a nitride sidewall. The device is still fabricated with a single step of lithography by using a self-aligned nitride sidewall process before the deep RIE step. Similarly, the nitride thickness can be independently reduced to attain a significant decrease of pull-in voltage, but only at the expense of the breakdown voltage of the insulator. Also, using a bending stiffness of $k \approx 0.04$ *N/m* extracted from FEM combined with a simulated force curve for the electrostatics of the device, the pull-in voltage was evaluated to be ~12.5V, in agreement with our 10V device. The inclusion of a thickness dependent E would further reduce the simulated pull-in voltage and resonant frequencies. Given linear scaling of all dimensions, the operation voltage should decrease to ~1V for 45nm features. Finally, we note that the approach lends itself to implementation in non-crystalline structures, and that interposers fabricated with these devices can be employed for configuring in 3D integration. In such implementations, the simple technology of this approach and its separation from CMOS may be of benefit.

CONCLUSIONS

A prototype of a low voltage vertical silicon based NEMS switch utilizing a straightforward top-down approach has been demonstrated. We take advantage of the true three dimensionality of this structure by using bending and torsion to overcome the obstacles posed to vertical devices. The mechanical layer need not be SCS; a-Si and other materials can be used with ease atop multiple device layers. These structures used in configuring matrix could also be employed on a separate wafer to provide interposer based programmability in 3D integration, and for enhanced functionality to logic [9].

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