TITANIUM NITRIDE SIDEWALL STRINGER PROCESS FOR LATERAL NANOELECTROMECHANICAL RELAYS

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ABSTRACT

This paper reports on lateral nanoelectromechanical (NEM) relays based on variations of a two- or three-mask titanium nitride (TiN) sidewall stringer process. Electrically isolated TiN perimeter beams are fabricated from stringers formed on the inside walls of polysilicon trenches, yielding 200nm wide TiN fins and 200nm gaps; these dimensions are 3X smaller than the resolution limit of the optical lithography tool (600nm) utilized. The reduction in the operating voltage is about a factor of 5 compared to 600nm wide polysilicon beams. Simple scaling could potentially enable sub-1V operation. Five-terminal NEM relays demonstrate successful switching in both directions over 1000 DC-sweep cycles with low drain bias (100mV).

INTRODUCTION

NEM relays offer four key features compared to CMOS transistors [1,2]: zero leakage current, infinite subthreshold slope, scalable threshold voltage, and hysteretic characteristics. The first three features allow zero off-state power dissipation, ultra-low dynamic power dissipation, and ultra-low voltage operation, respectively. The fourth feature enables the NEM relays to be used as memory cells [3,4]. If scaled, they offer an ultra low power alternative to CMOS transistors. The required dimensions of the NEM relays for CMOS-compatible low voltage actuation are estimated to be around 10nm for the gap size and beam thickness [1].

Lateral relays have several advantages over vertical relays [1], including simplified fabrication using fewer masks and a wider device design space (*e.g.*, varying gap size) for the same process flow. For conventional process flows, the gap is set by the lithographic resolution, resulting in high operating voltages.

Our approach overcomes this limitation by fabricating electrically isolated TiN beams from sidewall stringers formed on the inside walls of polysilicon trenches, yielding narrow beams with reduced gaps. For an initial trench width of W and a TiN deposition thickness of t, the gap between electrodes (g) is reduced to $W-2t$. The polysilicon mold is selectively removed by isotropic etching, resulting in released TiN beams, which will be referred to as "perimeter beams" in this paper. TiN is chosen as a structural layer due to its low electrical resistivity of 20$\mu\Omega$-cm, high Young's modulus of 600GPa, and chemical inertness suitable for NEM relay contacts [2,5]. A polysilicon beam is not suitable for relays since it requires a large drain bias for conduction due to native oxide formation on its surfaces.

Sidewall stringer processes have been developed for composite beams [6] and for high aspect-ratio springs used in a MEMS display [7,8]. These complex processes require more masks [6,7] and do not provide the electrical isolation or the small gaps required by relays [1]. Previous MEMS lateral switch fabrication processes used SOI [9] substrates or multiple wafers [10].

FABRICATION

The TiN sidewall stringer process has been developed in three variations. The first, two-mask variation creates released contact points for the gates and drains as well as the beam, which can cause unintentional contact between the gate and beam at pull-in. The second variation changes the second mask of the first version to create stiffer gates and drains, but yields an undesired polysilicon-TiN interface in series at the electrodes. Finally, a three-mask variation incorporates both stiffer gates and drains and TiN coated electrodes.

The first two-mask process starts with a 1.1μm thick LTO and 1.1μm thick doped-polysilicon deposition, followed by an RTA at 1075°C, as shown in Fig. 1. The polysilicon is patterned (Mask 1) using i-line optical lithography and a reactive-ion-etch (RIE) with a minimum feature size of 600nm. A 200nm-thick TiN layer is conformally deposited using MOCVD and patterned using Mask 2 (1a). The TiN etching creates electrically isolated beams, defines the electrodes, and creates openings for subsequent polysilicon etching (1b). The masking layer from Mask 2 is placed away from

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critical contacting features to ensure proper electrical isolation of the beams. The exposed polysilicon is removed by isotropic XeF_2 etching, which has high selectivity to TiN, LTO, and photoresist. The process is completed with a 49% wet HF release followed by critical point drying (1c). If the isotropic XeF_2 etching is skipped, TiN-coated polysilicon beams can be fabricated instead.

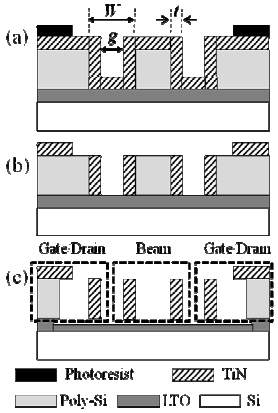


Figure 1. Two-mask TiN sidewall stringer process flow: (a) Conformal deposition of 200nm thick TiN layer on the patterned 1.1μm thick polysilicon mold (Mask 1) followed by the second lithography (Mask 2), (b) Anisotropic etch of TiN to electrically isolate beams, define the electrode, and create opening for the subsequent polysilicon etching, (c) Removal of the exposed polysilicon by isotropic XeF_2 etching with high selectivity to TiN and LTO. Then the device release in 49% wet HF followed by critical point drying. For an initial trench width of W and a deposition thickness of t, of TiN, the gap between electrodes (g) is reduced to $W-2t$.

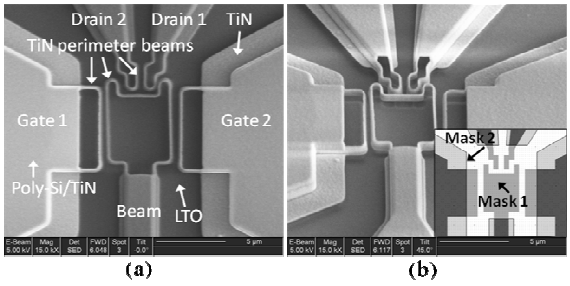


Figure 2. SEMs and mask layout of a fabricated lateral five-terminal NEM relay actuated in an SEM using the process in Fig. 1: (a) Top view, (b) 45 degree oblique view (Inset: Mask layout). The beam-to-gate and beam-to-drain spacing is 350nm and 200nm, respectively. The drains functions as a mechanical stop.

Figure 2 shows SEMs and layout of a five-terminal relay consisting of a beam, two gates, and two drains; all thicknesses are 200nm. The beam is actuated by the charge input by the scanning electron beam. The beam, gates, and drains consist of TiN perimeter beams, TiN caps, and anchors. The TiN perimeter beams have closed boundaries and are formed along the boundaries of the polysilicon mold structures that are not protected by Mask 2. The anchors consist of LTO-TiN and LTO-polysilicon-TiN stacks. The separated arrangement of the drains and gates in Fig. 2 allows an increased overlap between the gates and the beam for lower voltage actuation.

For reliable in-plane actuation with low relay actuation voltage, high aspect-ratio beams and narrow gaps are critical. To achieve these goals, this process requires vertical sidewalls on the polysilicon mold, conformal deposition of the TiN layer, and high aspect-ratio etching of the TiN.

Figure 3 shows a cross-sectional SEM of single-crystal silicon trenches coated with the TiN layer. The trench depth and the width are 1.1μm and 650nm, respectively. The TiN on the sidewall is shown to be thicker (200nm) than that on the top and the bottom (120-140nm) of the trenches. This is preferred to a conformal deposition since less TiN needs to be etched to electrically isolate the beams. During the TiN etching, the electrical isolation of the beams was achieved relatively easily for the trenches with an aspect-ratio below 3.5:1 whereas excessive etching was required when the aspect-ratio was above 5:1.

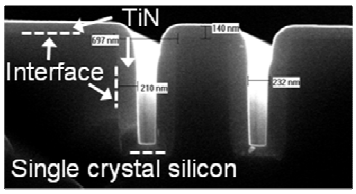


Figure 3. Cross-sectional SEM of single-crystal silicon trenches coated with the TiN layer using MOCVD. The trench depth and the width are 1.1μm and 650nm, respectively. The TiN on the sidewall (200nm) is thicker than that on the top and the bottom of the trenches (120-140nm).

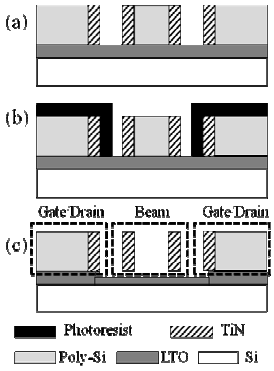


Figure 4. A variation of two-mask process: Compared to the process in Fig. 1, a blanket TiN etch in (a) precedes the second lithography in (b), leading to stiffer gates and drains with polysilicon electrodes in (c). The photoresist is used as an additional etching mask in isotropic XeF_2 etching.

Figure 4 shows the two-mask variation that yields stiffer gates and drains in addition to polysilicon electrodes. The variation consists of a blanket TiN etching prior to the second lithography. Figure 5 shows a SEM and layout of a switch actuated in an SEM. Openings for the beam release in the second mask are designed to have boundaries along the center lines of the trenches for maximum misalignment tolerance. This patterning step is self-aligned.

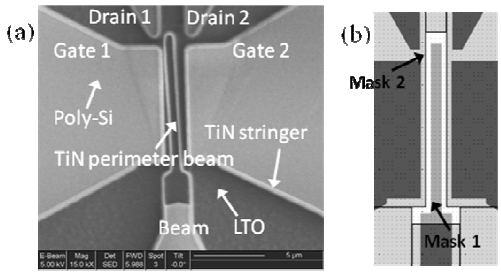


Figure 5. (a) Top view SEM and (b) mask layout of a fabricated lateral five-terminal NEM relay actuated in an SEM using the process variation in Fig. 4. The beam-to-gate and beam-to-drain spacing is 200nm and 250nm, respectively. The drains could not work as mechanical stop.

The two-mask processes in Figs. 1 and 4 can be easily combined into a single three-mask process so that stiffer gates and drains and TiN coated electrodes are obtained. After patterning the TiN in the first process, the second mask in the second process is applied to protect the gates and the drains from the subsequent XeF_2 etching. Figure 6 shows an SEM and layout of a switch actuated in an SEM.

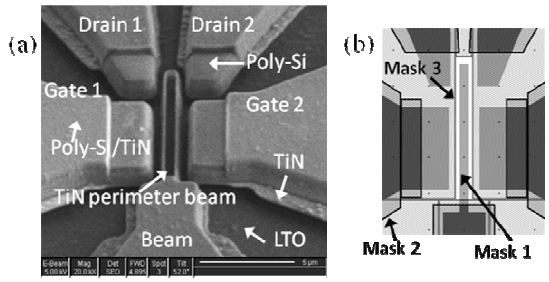


Figure 6. (a) Oblique-angle SEM and (b) mask layout of a lateral five-terminal NEM relay actuated in an SEM using a three-mask process that combines the two processes in Figs. 1 and 4.

MODELING

The perimeter beam formed along a rectangular shaped cantilever mold as shown in Figs. 5 and 6 can be approximately modeled as half of a fixed-fixed beam since its movable end works as a guided end. The spring constant and pull-in voltage can be given by [11]

$$k = \frac{4Eht^3}{L^3},\ V_{PI} \cong 0.604\sqrt{\frac{kg^3}{\varepsilon hL}} \quad (1)$$

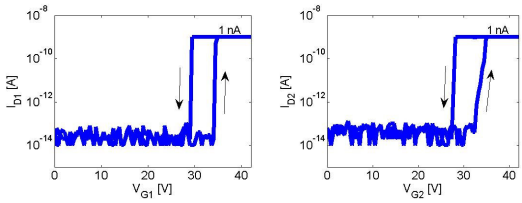
where ε is the permittivity and L, h, E are the length, height, and Young's modulus of the beam, respectively. A full overlap between the gate and the beam is assumed; *i.e.*, the overlap is the same as the beam length. Partial overlap increases the pull-in voltage.

For a given trench width of W, V_{PI} of the perimeter beam is maximized at $t=W/4$ with its maximum proportional to W^3/L^2. Compared with a cantilever beam with $g=t=$W and the same material, V_{PI} is reduced by a factor of 10.3. Either $t<<W$ or $g<<W$ makes V_{PI} approach zero. In practice, for a given beam aspect-ratio, set by the limitations of the etcher and the structural metal deposition, t/W, g/W, and h/W are determined to minimize V_{PI}. In this case, V_{PI} is still proportional to W^3/L^2 indicating the importance of scaling W. The initial trench width set by the lithographic resolution can be further reduced by conformally depositing oxide followed by a directional etch. This could enable a CMOS-compatible low voltage actuation. Note that the perimeter beam could be separated into two beams with an additional isotropic etching of TiN and an additional mask. This results in a further reduction in V_{PI} by a factor of 2.2.

RESULTS

For the device in Fig. 2, the beam-to-gate and beam-to-drain spacing is 350nm and 200nm, respectively, with 200nm thick TiN and zero beam bias. Switching operations in both directions were successfully demonstrated with a pull-in and pull-out voltage of 34V and 29V for the left gate actuation, and 34V and 27V for the right gate actuation with drain bias of 100mV, showing adequate symmetry (Fig. 7). The finite subthreshold slope in I_{D2} vs V_{G2} was observed indicating an inconsistent initial contact resistance. The test equipment used was Agilent 4156C, and the operation was quasi-static. After 1000 DC-sweep cycles of switching in both directions with low drain bias (100mV) in room air, the device continued to operate successfully.

Figure 8 shows drain current versus gate voltage characteristics with varying drain bias for a similar device as in Fig. 6. The length of the beam is 16μm with the same spacing values as the device above. The pull-in and pull-out voltage is 18.6V and 13.2V, respectively. Clear transitions of the switching were obtained at a drain bias as small as 5mV. The pull-in and pull-out voltage of the polysilicon beam (E=169GPa) in the same design with a drain bias of 3V was measured to be 90V and 84V, respectively.



(a) (b)

Figure 7. Drain current vs gate voltage characteristics of the NEM relay in Fig. 2 with drain bias=100mV in room air. Successful actuations in both directions are achieved with adequate symmetry in I-V curves: (a) Gate 1, (b) Gate 2 actuation. The current compliance is set to 1nA.

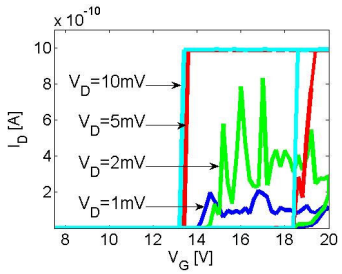


Figure 8. Drain current vs gate voltage characteristics of a NEM relay similar to the relay in Fig. 6 with varying drain bias. Clear transitions of the switching were obtained at a drain bias of 5mV. The current compliance is set to 1nA.

Devices with less beam-to-gate spacing mostly suffered from failure mechanism of the relays; *i.e.*, the beam collapses into the gate at pull-in with a spike in the drain current. All the devices fabricated had a single island of polysilicon mold for each electrode. This layout required precise control over the isotropic XeF_2 etching step to avoid excessive polysilicon etching, which contributed to the failure mechanism and lower yield. Better control can be achieved by using two separate islands of polysilicon mold for each electrode, which are electrically connected with the TiN layer. The additional island provides an etch stop for the polysilicon etch step.

Due to the symmetry of the TiN structures, deflection due to stress gradients is mitigated. Issues with stress gradient were not observed, so post-deposition TiN annealing was not used. However, annealing may affect the switching characteristics and reliability, which are being investigated.

CONCLUSIONS

We present lateral NEM relays based on variations of a two- or three-mask TiN sidewall stringer process. The process enables minimum feature size below the lithographic resolution, yielding a significant reduction in the pull-in voltage. In theory, the pull-in voltage can be scaled down to below 1V for CMOS-compatible low voltage actuation. The actual limit will depend on the verticality of the initial mold sidewall, conformality of the TiN layer deposition, and the aspect-ratio limit of the TiN etch process. This process technique can be directly applicable to other coating and sacrificial materials for the study of optimum beam materials with desired mechanical and electrical properties and compatibility to Back-end-of-line (BEOL) processes. Extensive studies of the reliability and the failure mechanisms of the perimeter beams are in progress.

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