HIGH CURRENT LOW CONTACT RESISTANCE PLATINUM-COATED CMOS-MEMS PROBES

J. Liu, L. Draghi, M. Noman, J.A. Bain, T.E. Schlesinger and G.K. Fedder
Carnegie Mellon University, Pittsburgh, Pennsylvania, USA

ABSTRACT

We report on high current, low contact resistance, platinum-coated, lever-based CMOS-MEMS electrothermal probes with embedded displacement and force sensors for MEMS Instrumented Self-Configuring Integrated Circuits (MISCICs). The MISCIC vision is to use MEMS conductive probes to reconfigure ICs, mainly RF ICs such as inductors, by mechanically addressing and passing current pulses through resistance change vias which are embedded within chip circuitry. With a platinum-coated conductive tip of 2.6 × 2.6 μm^2 and a contact force of around 20 μN, the achieved contact resistance is 0.64 Ω. The tip and its routing path survive after passing a 20 mA DC current for 60 minutes without failure.

INTRODUCTION

Since the introduction of the STM by Binnig and Rohrer in 1981, probes have been widely used in surface and friction measurements, SPMs [1], AFM nanolithography [2], IC chip testing [3] and high areal density data storage [4]. In these applications, probes are either stationary or actuated by piezoelectric, electrostatic, electrothermal (ET), or magnetic mechanisms. Compared with other mechanisms, ET actuation generally achieves larger stroke and higher stiffness but with the possible penalties of slower tuning and greater power dissipation.

The MISCIC vision is to use MEMS conductive probes to reconfigure ICs, mainly RF ICs such as inductors, by mechanically addressing and passing current through resistance change vias (RCVs) embedded within chip circuitry. In the envisioned implementation, vertically actuated probes are arrayed on a single movable platform which is suspended by lateral actuators. The use of the x-y platform carrying the probe array follows the concept employed in probe-based data storage to attain complete areal coverage [4]. The probe itself and the contact to the circuitry (with area of 1 μm^2-order) must be conductive enough to support current pulses of 10 mA or larger to reconfigure 500 × 500 nm^2 or larger RCVs [5]. Thus a small contact resistance is desired for this application.

Though the spring constant of the active probes may be as high as 100 N/m, it is impractical for sub-mm sized active probes with sub-1 μm^2 contacts to achieve mN-order forces [3] to break through the oxide layer on top of the tips due to the yield stress limit of the probe contacts. Therefore, non-oxidizing metal such as nickel (Ni) and platinum (Pt) must be deposited on the tips to enable contact forces to decrease to values between 1 to 50 μN. These values of force can be implemented with compact MEMS springs. With contact forces on the order of 1 μN, contact resistance of 10 - 100 Ω was reported with sub-1 μm^2 contact in Ni-plated push-down probes [6]. With contact forces on the order of 10 μN, contact resistance of 1 - 10 Ω was reported with sub-1 μm^2 contact in Ni-plated push-up probes [7]. However, the Ni-plated tips oxidized after exposure in air for a few weeks and did not make reliable contacts. Pt sputtering was developed to achieve non-oxidizing reliable contacts [8].

High currents can be used to generate large enough heat to open MEMS fuses [9] and to de-tether microsystems [10]. In MEMS relays [11], high current carrying capability is crucial for their actual applications, while heat as small as possible is desired to be generated at the relay contacts to extend their lifetime. Typically, the relay contacts failed in a few hours or less at pulse current densities on the order of 10^7 A/m^2. No failure mechanisms are discussed and developed in these papers.

Systematic current carrying capability is assessed on chips to identify failure mechanisms and to guide future design.

PROBE DESIGN

The probe mechanisms discussed here are made in a CMOS-MEMS process using the metal-dielectric layers of the CMOS as the composite micromechanical material. The push-up actuation is achieved by the lever structure shown in Fig. 1a. The probes are rotated 45° and placed at the chip edge and a backside silicon etch is under development to create overhanging probes to transform RCVs in upcoming tests. The thermally actuated flexures are made from 8 parallel 50 μm-long, 3 μm-wide, 1.8 μm-thick "metal 1" (M1) beams comprising the lowest CMOS metal and oxide layers. The central "metal 3" (M3) flexure folds back toward the M1 anchor and employs 10 parallel 3 μm-wide, 5 μm-thick beams with an average length of 155 μm and maximum length of 180 μm, made from the metal 1-2-3 stack, to keep probe stiffness to achieve low constant resistance.

Due to residual stress gradient in CMOS-MEMS beams, upon release, the M1 flexures self-assemble upward away from the substrate, and the M3 flexure and tip are levered downward toward the substrate. Upon actuation due to the thermal bimorph effect, the M1 flexures move downward and the M3 flexure and tip move upward. The thinner M1 beams are chosen for the thermal bimorph probe to reduce the bending moment of inertia, which helps provide high drive sensitivity. Polysilicon resistors forming actuation heaters are placed at each end of the M1 flexures. Dummy heater beams are added to eliminate the thermal buckling caused by temperature non-uniformity across the parallel beams [6]. They have the same features as the M1 flexure beams in every respect except that they are mechanically disconnected from the M1 flexure beams, which ensures they do not affect the M1 flexure actuation. Improved metal-slotted thermal isolation structures [8] are placed on both ends of the M1 flexure to increase the

temperature uniformity and drive sensitivity. This design prevents heat from directly passing through aluminum interconnect to the anchors, instead having to pass through the CMOS tungsten vias.

A platinum (Pt) sputtering process was developed to coat the tips aiming to achieve small and reliable contact resistances (Fig. 1b) [8]. Two independently actuated probes are located 5 µm apart to provide two simultaneous contacts that form a direct current return path during reconfiguration to minimize capacitive parasitics (Fig. 1c). Piezoresistive sensors [12] are embedded to detect relative vertical position and mechanical contact of the probe and substrate and to aid in future tip registration to patterned substrates.

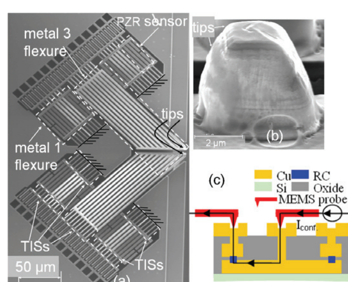

Fig. 1: Two lever-based ET probes with piezoresistive (PZR) sensors to reconfigure RF IC's. (a) SEM, (b) Pt-coated tip, and (c) Concept of two probe reconfiguration.

PROBE PROCESS

The particular CMOS MEMS process employed here begins with a custom-designed CMOS chip, followed by a directional oxide etch to define dielectric/metal microstructures [13]. A Si deep-reactive-ion etch (DRIE) is used to set the etch pit depth followed by a timed silicon isotropic etch for structural release.

Probe tips are designed by stacking CMOS vias and metal layers as shown in Fig. 1b. The aluminum top layer must be coated with a non-oxidizing metal to be effective as a dc contact. Our initial metallization studies used an electroless Ni plating [6-7] but this was not truly inert. In this new design, tip-platform Pt sputtering [8] is employed to achieve reliable contact with low contact resistance.

The M1 flexures self-assemble upward by 4.4 µm and the tips are levered downward by 14.1 – 14.4 µm. Attributed to the TISs and flexural beam length extension from 80 µm to 180 µm, the probe achieves an upward stroke of 29.6 µm at a 10 V, 19.65 mW drive with a linear 1.46 µm/mW sensitivity (Fig. 2a), a 9× improvement from previous generations [12]. Thermal cross-talk is 1.5% to the adjacent probe located 5 µm away. The thermal cut-off frequency is 182 Hz, the resonant frequency is 40440 Hz, and the quality factor is 45.4 (Fig. 2b).

CONTACT RESISTANCE TEST

A contact test setup was created by carefully positioning a 0.6 µm-radius tungsten (W) probe over the MEMS probe tip using a custom 6-DOF x-y-z-tilt test-stand. A 10 V, 19.65 mW "background" drive was employed to move the tips upward by 29.6 µm to enable contact testing. Electrical contact was not observed immediately upon the physical contact of the W probe and the MEMS probe tip. The physical contact was judged by the reflection change under an optical camera. The W probe was then pushed downward further to achieve a force strong enough to establish electrical contact.

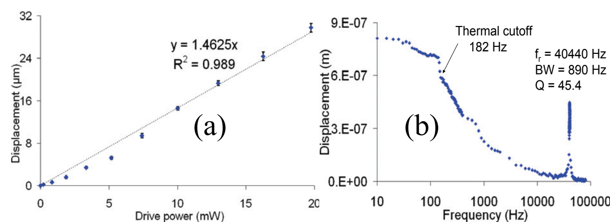

Fig. 2: Actuation (a) and frequency response (b) of probe

The change of the total resistance, which was extracted from I-V scans and included a routing resistance of 475 Ω, versus the vertical W probe position was plotted in Fig. 5. A 4.7 µm displacement beyond the physical contact, corresponding to a 3.62 µN force, was needed to establish electrical contact (Fig. 3). A 0.7 µm hysteretic displacement was observed, corresponding to a 0.54 µN force. Generally, the resistance decreases with increasing force as expected. The bump in resistance during transition to the contact state is believed to be caused by the test-stand vibration during test. Tens of tests show force-dependent contact resistances better than 1 Ω and the minimum is 0.64 Ω, which is close to 0.36 Ω, the expected resistance from our previous model [7].

By fixing the probe drive and W probe position, a 2.5% resistance variation was observed over two thousand I-V scans at 10 mA, which lasted 2 hours (Fig. 4).

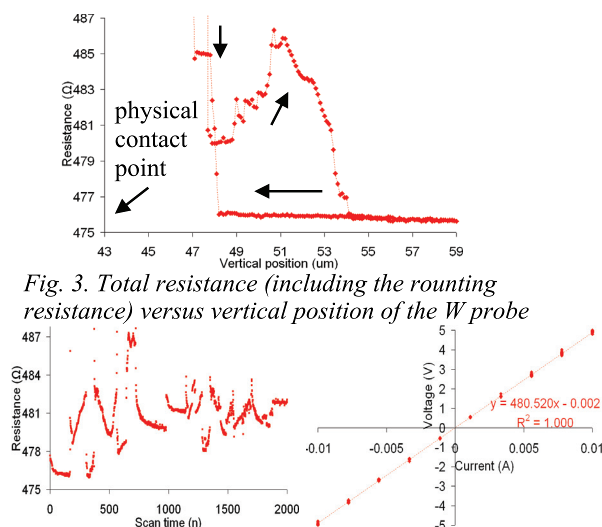

Fig. 3. Total resistance (including the rounting resistance) versus vertical position of the W probe

Fig. 4. Resistance extracted from two thousand I-V scans (left) and average value plotted in I-V scan curve (right)

CURRENT CARRYING TEST

Electromigration is the transportation of materials caused by the gradual movement of the ions in a conductor due to the momentum transfer between conducting electrons and diffusing metal atoms. As feature/structural sizes in

electronics such as ICs decrease, the practical significance of this effect increases. The electromigration decreases the reliability and lifetime of ICs. In the worst cases, it leads to the eventual loss of one or more connections and intermittent failure of the entire circuit.

In late 1960s, J.R. Black developed an empirical model to estimate the mean time to failure (*MTF*) of a wire, taking the electromigration into consideration [14]:

$$MTF = A\left(J^{-n}\right)e^{\frac{E_a}{k_B T}} \tag{1}$$

where A is a constant based on the cross-sectional area of the interconnect, J is the current density, E_a is the activation energy (*e.g.*, 0.7 eV for grain boundary diffusion in aluminum), k_B is the Boltzmann's constant, n is a scaling factor, which is usually 2 based on [14], and T is the temperature. Larger current density and/or temperature leads to smaller *MTF*.

The *MTF* in (1) is a mean lifetime usually statistically extracted from multiple measurements at a group of samples. In our tests, only one or a couple of measurements are done at each point, and we admit that there may be some difference between the *MTF* and the failure time we extract. But here we still use the failure time to replace the *MTF* to roughly predict the relation between failure time and failure current density.

The material melting induced by high temperature and the electromigration induced by high current density are the two main effects to cause connection failure in CMOS-MEMS structures. Melting is observable with shape/color change under a microscope or SEM. The electromigration may be checked and verified with the microscope/SEM if it happens on top metals. Otherwise, a focused ion beam cut is needed to check possible voids or shape change in cross sections to verify.

The currents in the tests are usually less than 150 mA, which is smaller than the failure currents in interface and contact. It is believed that all the failure in the following sections does not happen in the interface or contact. Rather, it is believed that all the failure is mainly caused by electromigration which happens within the CMOS chip such as metal wires, connection vias, or probe tips.

Systematic current carrying tests are run on metal wires, vias, and/or tips to search for failure time, *i.e.*, the time where electrical connection is broken, thus developing a quantitative way to assess maximum current densities.

In our cases, the current density J is high enough, thus the temperature T changes with passing current due to Joule heating. When J increases, T increases. (1) is revised as

$$\log_{10}(MTF) = \log_{10}(A) - n\log_{10}(J) + 0.4343 \times \frac{E_a}{k_B T(J)} \tag{2}$$

Thus, in our experiment, we are conceptually picking up data points from idealized *MTF* vs. current density curves defined by (1) with different temperatures, which is shown conceptually in Fig. 5. It is expected that the slopes may be much larger than the idealized value, 2, in (1).

The failure time versus DC failure current densities for interconnects such as M1 wires and vias in unreleased and released chips are plotted in Fig. 6 Compared to the unreleased chips, the failure current densities decrease 8× in the M1 wires, and 0.2× in the vias.

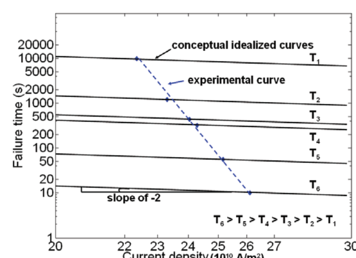

Fig. 5. Conceptual explanation for our experimental data

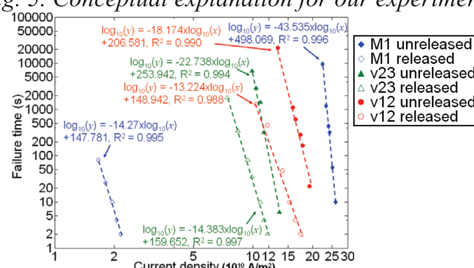

Fig. 6 Failure time versus current densities for the interconnects on unreleased (filled symbols) and released chips (symbols unfilled)
Note: vmn is the connection via between metal m and n.

Generally, the failure current decrease is caused by higher temperatures. In unreleased chips, the heat generated when passing current is easily dissipated to the silicon substrate. However, in released chips, the interconnects are suspended over the silicon substrate and the heat has to mainly flow through the metal wires and vias to thermal anchors, i.e., chip surface with room temperature T_0. Thus the suspended interconnects should have higher temperature. From (1) the higher temperature degrades failure current densities.

At high current density, the electromigration failure may be delayed or eliminated if the current is pulsed at low duty cycle, apparently owing to the long "rest" periods during pulses [15].

Systematic current pulse carrying tests were run on Ni-coated tips connected to metal wires and vias in released chips. In these pulse cases, the failure time is defined as the total passing current time, *i.e.*, physical test time times the duty cycle. No failure is found at the tips with post-experiment examination.

With 100 Hz 80% duty cycle, pulse failure times versus failure current density for M1 wires and vias are plotted in Fig. 7. It is extrapolated that the DC curve and pulse curve will cross each other. For example, the two M1 curves should cross at 1.26×10^{10} A/m^2, the two v12 curves at 8.14×10^{10} A/m^2, and the two v23 curves at 3.66×10^{11} A/m^2. When current densities are larger than these critical densities, failure times for pulse drives are larger. Otherwise, failure times for DC drives are larger.

Generally, failure times for pulses are larger than those for DC, which are explained by lower effective temperature in pulse drives. For instance, at a current density of 2 ×

10^{10} A/m^2, failure time for M1 wires increases from 6s for DC drives to 817s at 100 Hz, 80% duty cycle pulses, with an increase of 135×.

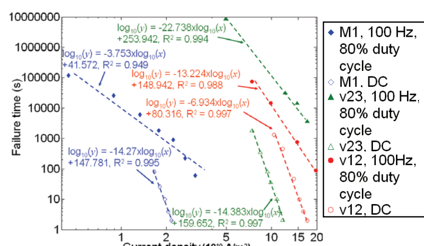

Fig. 7 Comparison of the failure time at DC and pulse currents from released chips

In unreleased chips, at fixed pulse frequency and current magnitude, the relation between failure time and pulse duty cycle is linear when plotted in log-log scale (Fig. 8). At smaller duty cycles, the rest periods are longer and the effective temperature over each pulse cycle is smaller. Therefore a smaller duty cycle leads to longer failure time or larger failure current density.

Failure time at very low frequency, say 0.01 Hz, should be close or equal to that at DC current. As shown in Fig. 9, for v23s, at density of 1.73×10^{11} A/m^2 and duty cycle of 80%, the failure time at 0.01 Hz is 13s, which is the same as the failure time at DC current. The failure time increases from 13s to 1.43×10^6s when the pulse frequency increases from 0.01 Hz to 10 MHz. Compared to the failure time at DC, the failure time increases by 110,000×. A linear relation exists between the failure time and pulse frequency in log-log plot.

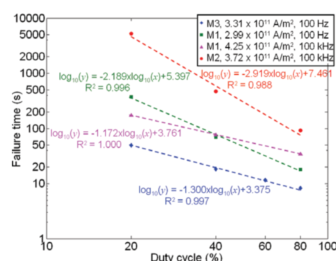

Fig. 8. Failure time versus pulse duty cycle at different frequencies and magnitudes

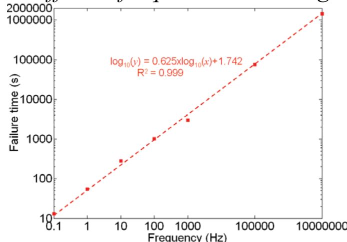

Fig. 9. Failure time versus pulse frequency at 80% duty cycle and current density of 1.73×10^{11} A/m^2

The mechanism development for the smaller pulse failure time at small current density (Fig. 7) and the pulse failure time increase with increasing pulse frequency (Fig. 9) is under way.

The routing path to the Pt-coated tip (Fig. 1b) is constructed with 3 µm-wide wires with one via. The tip and its routing path survived after passing a 20 mA DC current for 60 minutes.

The shape and optical color change induced by electromigration is observed under an optical microscope and SEM when it happens on the top metal (Fig. 10). The obvious material transportation is observed on the top metal layer: the metal is lumped and stacked in some places and discontinuous or voided in some other places.

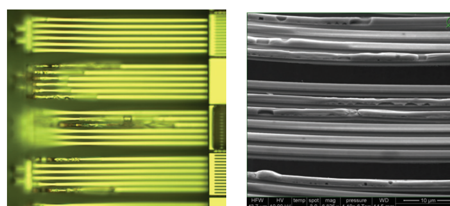

Fig. 10. Electromigration observed with microscope (left) and SEM (right)

CONCLUSIONS

Lever-based platinum-coated CMOS-MEMS probe tips are demonstrated to be able to achieve sub-1 Ω contact resistance and pass a 20 mA DC current for 60 minutes without failure. More experiments are under way to test pulse carrying capability and reliability of sensors and electrical contacts.

ACKNOWLEDGMENTS

This work was funded in part by the FCRP Focus Center for Circuit & System Solutions (C2S2), under contract number 2003-CT-888, and the DARPA N/MEMS S&T Fundamentals Program MISCIC Center, under contract number HR0011-06-1-0047. We thank Dr. Suresh Santhanam and the Carnegie Mellon Nanofabrication Facility for processing support.

REFERENCES

[1] B.P. Jena et al., Force Microscopy: Applications in Biology and Medicine, Wiley, NY, 2006.
[2] S.C. Minne et al., Appl. Phys. Lett., vol. 73, no. 12, pp. 1742-1744, 1998.
[3] C. Tsou et al., J. Micromech. Microeng., vol. 16, pp. 2197-2202, 2006.
[4] http://www.zurich.ibm.com/st/index.html.
[5] H. Lo and J. Bain, Proc. of IMECE2008, pp. 687-696.
[6] J. Liu et al., Proc. MEMS 2008, pp. 515-518.
[7] J. Liu et al., Proc. MEMS 2009, pp. 1111-1114.
[8] J. Liu et al., Proc. Sensors 2009, pp. 1911-1914.
[9] G.K. Fedder, Ph.D. thesis, University of California at Berkeley, CA, 1994.
[10] K.S. Colinjivadi et al,, Microsystem Technologies, vol. 14, pp. 1621-1626, 2008.
[11] H.S. Lee et al., Proc. of the 50th Holm Conference on Electrical Contacts & 22nd international Conference on Electrical Contacts, pp. 242-247, 2004.
[12] J. Liu et al., Proc. Transducers 2009, pp. 2425-2428.
[13] G.K. Fedder et al., Sen. Actuators A, vol. 57, pp. 103-110, 1996.
[14] J.R. Black, IEEE Transactions on Electron Devices, vol. ED-16, no. 4, pp. 338-347, 1969.
[15] A.T. English, K.L. Tai and P.A. Turner, Appl. Phys. Lett., vol. 21, pp. 397-398, 1972.