# A GENERALIZED FOUNDRY CMOS PLATFORM FOR CAPACITIVELY-TRANSDUCED RESONATORS MONOLITHICALLY INTEGRATED WITH AMPLIFIERS

Wen-Chien Chen<sup>1</sup>, Che-Sheng Chen<sup>2</sup>, Kuei-Ann Wen<sup>2</sup>, Long-Sheng Fan<sup>1</sup>, Weileun Fang<sup>1</sup>, and Sheng-Shian Li<sup>1</sup>

<sup>1</sup>National Tsing Hua University, Hsinchu, Taiwan <sup>2</sup>National Chiao Tung University, Hsinchu, Taiwan

### ABSTRACT

A generalized foundry CMOS-MEMS platform suited for integrated micromechanical resonator circuits have been developed for commercial multi-user purpose and demonstrated with a fast turnaround time and a variety of design flexibilities for resonator applications. With this platform, different configurations of capacitively-transduced resonators monolithically integrated with their associated amplifier circuits, spanning frequencies from 500kHz to 14.5MHz, have been realized with resonator Q's around 2,000. This platform specifically featured with various configurations of structural materials, different arrangements of mechanical boundary conditions, large transduction area, well-defined anchors, and performance enhancement scaling with IC fabrication technology, offers a variety of flexible design options suited for sensor and RF applications.

# **INTRODUCTION**

The present wireless transceivers composed of conventional off-chip mechanical resonators and filters limit the miniaturization of communication devices as well as impede the cost-down and system integration for portable electronics. In order to reduce size, power consumption, and increase Q, vibrating micromechanical circuits fabricated using IC-compatible MEMS technologies have been developed towards the integration with on-chip RF transistor circuits [1]. However, prior approaches for CMOS-MEMS integration, such as mixed process [2][3], MEMS-first [4][5], and MEMS-last [6][7] strategies, requires enormous complexity and compromise of fabrication processes, impeding the fast cycling time of nowadays product development and of course causing huge barrier for industrial design houses. As a solution to aforementioned issues, foundry CMOS-MEMS platform such as dry-release-based [8] and wet-release-based [9] approaches provides ease of use, fast prototyping, and circuit integrated characteristics for vibrating RF-MEMS applications. Nonetheless, [8] confronts high motional impedance of their fabricated



Fig. 1: Perspective-view schematic of (a) a CMOS-MEMS free-free beam resonator monolithically integrated with amplifier circuits. (b) Cross-section view (A-A') of resonators fabricated using the proposed platform.

resonators due to the relatively large electro-to-resonator gap spacing from RIE-etched constraint while both [8] and [9] suffer the deficiency in design flexibilities on structural material configurations, mechanical boundary conditions, vibrating modes, multi-dimensional motions, and well-defined anchor geometry without affection of release undercut.

To overcome the abovementioned deficiency, this work develops a generalized platform utilizing TSMC 0.35µm 2-Poly-4-Metal process with a simple maskless release process, demonstrating ease of use, low cost, fast turnaround time, and innate MEMS-circuit integration. Various configurations of capacitively-transduced **CMOS-MEMS** resonators monolithically integrated with circuits have been demonstrated using this platform with resonance frequencies spanning from 0.5MHz to 14.5MHz and with Q's up to 2,200. In addition, the major bottleneck of capacitive resonators due to high motional impedance  $R_x$  is alleviated when the electrode-to-resonator gap spacing, of which  $R_x$  is proportional to the 4<sup>th</sup> power, can be scaled down with advanced IC technology, e.g., 0.18µm or even smaller feature-size CMOS process.

## **PLATFORM & DEVICE OPERATION**

To demonstrate most of the new features used in this platform, a laterally vibrating free-free beam resonator [10] with via-supported scheme, as shown in Fig. 1, is exemplified here to present that a composite resonator structure is formed utilizing metal (i.e., aluminum and tungsten) and SiO<sub>2</sub> while supported by vias (VIA) and contacts (CO) which serve not only electrical interconnects but mechanical supports to effectively conserve vibrating energy within resonator bodies due to the tiny size of these supports. As shown in Fig. 1(a), an on-chip trans-impedance amplifier is also integrated with resonators to resolve (1) parasitic feedthroughs from bond pads and (2) impedance mismatches between resonators and the  $50\Omega$ -based testing facilities, allowing us to directly measure the motional current induced by vibrating motions of resonators without the masking effects from feedthrough parasitics. To maximize the electro-mechanical coupling, the minimum electrode-to-resonator gap spacing of 0.5µm in this foundry process is formed between two smooth sidewalls of metal/via composite where the transduction areas are greatly improved, allowing smaller motional impedance for the resonators.

As shown in Fig. 1(b), CMOS-MEMS resonators fabricated using the proposed platform specifically possess several unique features including (1) complex structural materials which can be made of metal/oxide composite (case I), metal composite (case II), and pure metal (case III); (2) various mechanical boundary conditions of resonators such as fixed (not shown here), simply-supported (case II), and free end (case I & III) designs; (3) multi-dimensional displacements of resonators capable of in-plane (case I & II) and out-of-plane (case III) motions to the substrate surface; (4) standard CMOS vias (VIA) and contacts (CO) acting as tiny supports of resonators (case I & II), to effectively isolate the vibrating energy from resonators to their anchors, (5) well-defined anchors without undercut issue which is often seen in conventional CMOS-MEMS or SOI process; (6) better transducer



Fig. 2: Finite element simulated mode shapes for CMOS-MEMS free-free beam resonators. (a) In-plane mode. (b) Out-of-plane mode.



Fig. 3: (a) Top-level circuit schematic and (b) detail circuit schematic of the single-stage trans-impedance amplifier used in this work.

efficiency attained by utilizing via-connected walls (case I & II) to form a flat sidewall electrodes, all of which offer a variety of flexible options suited for sensor and RF applications.

To excite this device (shown in Fig. 1(a)), an ac signal  $v_i$  together with a dc-bias voltage  $V_P$  would generate an electrostatic force driving the beam into the corresponding vibration mode shape shown in Fig. 2(a) while Fig. 2(b) presents vibrating motion of case III in Fig. 1(b) for comparison. This motion creates time-varying capacitance between the beam and output electrode, sourcing out an output current  $i_o$  which would enter an on-site amplifier with a designed impedance gain. Fig. 3(a) presents the top-level schematic of the trans-impedance amplifier circuit used in this work to transfer the input motional current of vibrating resonators into voltage output with certain amplification factor  $R_{f}$ . In the detailed circuit schematic of Fig. 3(b), transistors  $M_1$ - $M_5$  comprise the basic single stage, differential op amp while  $M_6-M_{13}$ constitute a common-mode feedback circuit that sets its output dc bias point. The MOS resistor  $M_{Rf}$  provides resistance  $R_f$  and serves as shunt-shunt feedback element that allows control of the trans-impedance gain via adjustment of its gate voltage.

#### FABRICATION

To fabricate resonators using the presented platform, chips were manufactured utilizing standard  $0.35\mu$ m 2-Poly-4-Metal CMOS service from TSMC with a cross-section view shown in Fig. 4(a). Then a commercial SiO<sub>2</sub> etchant with very high selectivity to metal layers, vias, and contacts is utilized to release



Fig. 4: Cross-sections depicting the fabrication process used to achieve CMOS-MEMS resonators. (a) After standard CMOS process. (b) After wet release process. Various types of resonators are realized using this platform, including (i) via-supported free-free beam (B-B' of Fig. 1(a)), (ii) simply-supported beam, and (iii pure-metal free-free beam.

the resonator structures depicted in Fig. 4(b) without the helps of critical point dryers while the transistor circuits is protected by the passivation layer of silicon nitride. Please note that the via-connected sidewalls not only increase the transduction areas but also protect the inner SiO<sub>2</sub> without attacks by the release etchant, providing metal/oxide composite which might benefits temperature compensation scheme for future timing reference devices.

Fig. 5 presents the SEM's of fabricated CMOS-MEMS resonators, including (a) a chip global view, (b) a via-supported in-plane free-free beam, (c) a pure-metal out-of-plane free-free beam, (d) an in-plane simply-supported beam, and (e) an in-plane clamped-clamped beam, showing that this platform is capable of producing resonators with various modes, different mechanical boundary conditions, in-plane and out-of-plane directions of motions, and diversified supporting structures. During the wet release process of Fig. 5(b), via/contact supports of Fig. 6 are clearly seen, providing enough mechanical strength to support resonator body even when dc-bias voltage of more than 100V is applied. Please note that the anchored plane in Fig. 6(d) is still intact, offering a rigid anchor structures without affection of undercut issue often seen in other fabrication technologies.

## **EXPERIMENTAL RESULTS**

The fabricated resonators with their amplifier circuits in Fig. 5 were tested under controlled pressure of  $20\mu$ Torr using a custom-built chamber with an electrical hook-up of Fig. 7 for a conventional two-port measurement. The RF-Out port of an HP 8753ES network analyzer is connected directly to metal electrode of the CMOS-MEMS resonators inside the vacuum chamber while the analyzer's RF-In port is



Fig. 5: The SEM views of fabricated CMOS-MEMS resonators. (a) Overall-view of a chip. (b) Via-supported in-plane free-free beam. (c) Pure-metal out-of-plane free-free beam. (d) In-plane simply-supported beam. (e) Clamped-clamped beam.

connected to the output electrodes of CMOS amplifier circuitry. The dc bias voltage is connected to the body of the resonator.



Fig. 6: The SEM views of wet release process for CMOS-MEMS resonators with (a) 25-min, (b) 30-min, (c) 35-min, and (d) 40-min release time.



Fig. 7: Schematic illustrating the measurement scheme showing detailed connections for measurement instrumentation.

Fig. 8 presents the measured spectra for the CMOS-MEMS resonators with their integrated amplifiers spanning frequencies from 0.5MHz to 14.5MHz with Q's in a range of 800 to 2,200, verifying the efficacy of this platform. Furthermore, Fig. 9 shows the measured frequency characteristics for a stacked comb-drive resonator in Fig. 5(a) under different measurement conditions. The transmission spectrum of the resonator integrated with its amplifier under vacuum obviously outperforms the measured results of other conditions such as resonators tested with amplifier circuit in air (red spectrum) and devices tested without circuit under vacuum (green spectrum), indicating integration of MEMS and circuits is crucial for device performance enhancement.

## CONCLUSIONS

This work presents a general and easy-to-use platform provided for users to facilitate design and development of high-*O* MEMS resonating devices integrated



Fig. 8: Measured frequency characteristics in vacuum for fabricated CMOS-MEMS resonators. (a) Via-supported in-plane free-free beam of Fig. 5(b). (b) Out-of-plane free-free beam of Fig. 5(c). (c) In-plane simply-supported beam of Fig. 5(d). (d) Stacked comb-drive resonator of Fig. 5(a).



Fig. 9: Measured frequency characteristics for stacked comb-drive resonators of Fig. 5(a) under different measured conditions, including vacuum with amplifier, air with amplifier, and vacuum without amplifier.

with circuits, capable of achieving single-chip implementation for sensors and communication applications. In addition, fully-integrated CMOS-MEMS resonator circuits, occupying die area of only  $340\mu m$ x  $110\mu m$  in this work, offers very small form factor and low power consumption suited for future portable applications.

## ACKNOWLEDGMENT

This work was supported by the National Science Council (NSC) of Taiwan under grant of NSC -97-2218-E-007-014. The authors also wish to appreciate the TSMC and National Chip Implementation Center (CIC), Taiwan, for supporting the IC Manufacturing.

## REFERENCES

- [1] C. T.-C. Nguyen, *Trans. Ultrason., Ferroelect., Freq. Contr.*, vol. 54, no. 2, pp. 251-270, 2007.
- [2] T. Core, et al., Tech. Digest, Solid State Technology, pp. 39-44, 1993.

[3] C. T.-C. Nguyen, *et al.*, *J. Solid-State Circuits*, vol. 34, no. 4, pp. 440-455, April 1999.

[4] J. H. Smith, et al., Tech. Digest, IEDM'95, pp. 609-612, 1995.

[5] A. B. Graham, *et al.*, *Tech. Digest, MEMS'09*, Sorrento, Italy, pp. 23-26, 2009.

[6] W.-L. Huang, et al., Tech. Digest, MEMS'08, Tucson, Arizona, pp. 10-13, 2008.

[7] J. Costa, *et al.*, *Tech. Digest, Hilton Head'08*, Hilton Head Island, South Carolina, pp. 18-21, 2008.

[8] C. Lo, et al., Tech. Digest, Transducers'05, Seoul, Korea, pp. 2074-2077, 2005.

[9] J. Teva, et al., Tech. Digest, MEMS'08, Tucson, Arizona, USA, pp. 82-85, 2008.

[10] K. Wang, et al., J. Microelectromech. Syst., vol. 9, no. 3, pp. 347-360, Sept. 2000.