CHIP SCALE PACKAGE OF A MEMS MICROPHONE AND ASIC STACK

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ABSTRACT

Most MEMS microphone systems on the market are packaged by conventional chip bonding and wire bonding.. A significant step towards miniaturization was achieved earlier by applying flip-chip bonding to MEMS microphone packaging. This technology is called chip scale MEMS package (CSMP). Thereby the package size could be reduced to 2.8 x 2.05 x 0.9 mm³ compared to a standard size of 3.76 x 2.95 x 1.1 mm³. In this paper the next step in miniaturization is presented. A further reduction to a total size of only 2.05 x 2.05 x 0.95 mm³ was achieved by placing the ASIC directly under the microphone chip inside a cavity in the substrate. This design is called stacked CSMP.

Keywords: MEMS, Packaging, Microphone, Flip chip, Chip size MEMS package, CSMP, Frequency response

INTRODUCTION

Electret condenser microphones (ECM) get more and more replaced by MEMS microphones [1], with their main advantage being that exposure to high temperatures does not affect the sensitivity. Consequently, MEMS microphones can be assembled by standard reflow soldering on the PCB of a customer system. They also have the potential for a significant reduction of footprint and height. But most MEMS microphones on the market do not take full advantage of this because they are packaged by conventional die bonding and wire bonding of MEMS and ASIC chips on a laminate substrate. These packages are then closed by preformed lids [2, 3, 4], leading to package sizes much larger than the size of the chips.

To overcome this limitation in miniaturization, a microphone package using flip-chip technology instead of chip and wire bonding was developed [5], see figure 1. This package has now become even smaller and more sophisticated by placing the ASIC in a cavity of the substrate underneath the MEMS as shown in figure 2 and 3.

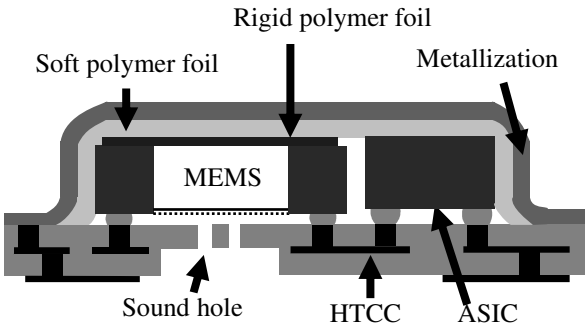


Figure 1: Schematic cross section of MEMS microphone packaged with CSMP.

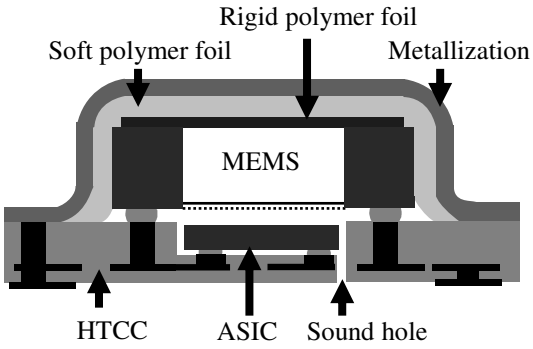


Figure 2: Schematic cross section of packaged MEMS microphone with the new stacked design.

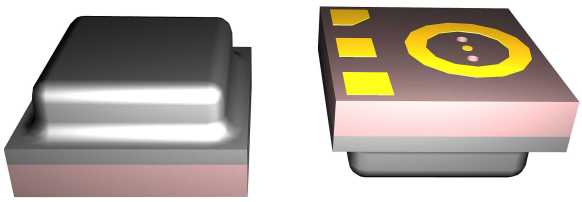


Figure 3: MEMS microphone in stacked CSMP. Package size is only 2.05 x 2.05 mm², package height typically 0.95 mm.

MEMS MICROPHONE PACKAGING

Comparison of old and new design

The microphone chip set employed in the packages described was developed and is produced by Infineon [1]. The MEMS transducer is a condenser microphone

with a flexible poly-silicon membrane of about 300 nm thickness. The rigid highly perforated counter electrode has a thickness of about 2 µm. The air gap between membrane and counter electrode is also around 2 µm. The MEMS chip has a total size of 1.35 x 1.35 mm² and a thickness of 400 µm while the ASIC has a size of 0.77 x 0.65 mm².

For both package types the same chip set is used, but in the new package the ASIC is thinned to a height of only 120 µm before assembly. The process flow is also slightly different. Instead of first bonding the MEMS chip, now the ASIC chip is flip chip bonded first into the cavity. After soldering the ASIC chip to the substrate the MEMS chip is bonded by a thermosonic process. Another change in the package is the reduction of the number of holes in the substrate for the sound inlet. Since the available space of the ceramic surface is significantly reduced in the new design, only 2 instead of the original 4 sound holes are placed. Because the sound holes have a strong resistive behavior on the acoustic wave, the diameter of both sound holes has slightly been increased from 100 µm to 125 µm.

Process of stacked CSMP

In figure 4 the CSMP process steps which are made on MEMS wafer level are shown. Infineon supplies undiced MEMS wafers (a). The first CSMP process step is the bonding of Au-stud bumps (b). For the connection to the HTCC substrate, Au-studs are used because the under bump metallization of the MEMS chip was developed for wire bonding and thus is not well suited for solder balls.

As second step a rigid polymer foil is laminated on the wafer to close the acoustic back volume (c). The foil is removed by a laser process in the dicing grid (d). Then the wafer is singulated by a stealth dicing process (e).

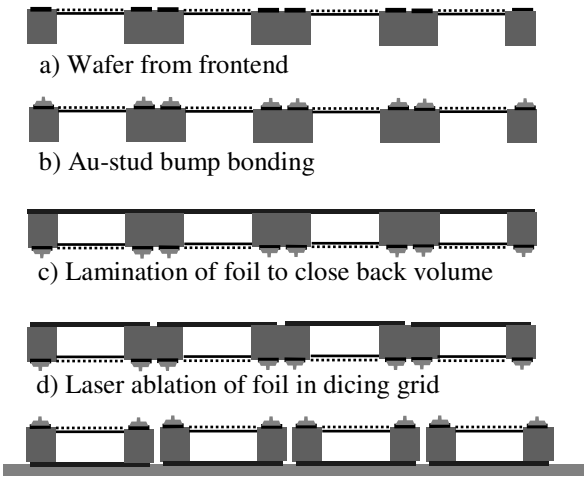


Figure 4: CSMP process steps on MEMS wafer level.

In figure 5 the stacked CSMP process steps which are made on the level of the ceramic panel are shown. A high temperature cofired ceramic (HTCC) is used as substrate and forms the bottom part of the package. In the substrate are two sound holes with a diameter of 125 µm. They can easily be integrated into the substrate because they are formed by the same process which is used to punch the holes for the vias into the ceramic. After punching, the vias are filled with metal while the sound holes remain unfilled. The cavity is also punched before laminating the green ceramic sheets prior to sintering the ceramic substrate.

The two small holes provide good protection of the MEMS chip against contamination by particles, droplets or fume from the soldering process. On the other hand they do not significantly reduce the sensitivity of the microphone in the acoustic frequency range.

The first backend process step is the flip chip bonding of the ASIC into the cavity of the substrate (a). The ASIC wafer is bumped with SnAgCu solder balls before wafer dicing. The ASIC chips are flip chip bonded with a tacky flux. After the bonding of chips on all units the panel passes a reflow process to solder the chips on the ceramic.

As next step the MEMS chip is connected to the HTCC substrate. This is done by thermosonic bonding of the MEMS chip on the Ni/Au bond pads of the substrate (b).

After bonding both chips, a soft polymer foil is laminated over the MEMS and the substrate to close the top side of the package (c). The soft foil also acts as a compliant buffer layer to reduce the mechanical stress on the MEMS chip caused by the package. In addition, the foil provides an electrical insulation between the Silicon chips and the top metallization which is grounded for good HF immunity of the microphone. A special lamination process has been developed to achieve small tolerances of the foil geometry at the gap between MEMS chip and substrate.

Between the chips the foil is laser ablated on the ceramic substrate (d). This is done for a direct contact between the ground connection in the substrate and the top metallization.

The top metallization is made by sputtering a plating base and by galvanic plating of Cu and Ni layers (e). The thickness of the metallization is above 50 µm to provide a package which is mechanically robust and can be assembled with standard pick and place equipment.

To separate the microphones the ceramic panel is mounted on a dicing foil and diced with standard wet wafer dicing equipment (f). Afterwards the

electroacoustic performance of all components is tested before packaging in tape and reel.

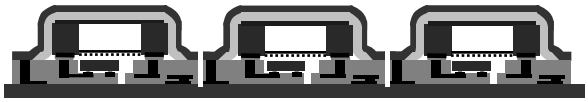
a) Flip chip bonding and soldering of ASIC

b) Thermosonic bonding of MEMS

c) Lamination of soft polymer foil

d) Laser ablation of foil

e) Metallization of package top



f) Singulation by dicing of ceramic substrate

Figure 5: CSMP process steps on ceramic substrate.

MODELLING THE FREQUENCY RESPONSE

As described in detail in [6], an analytical simulation model for calculating the frequency response of the microphone system was used. This model is based on the description of the air flow in the system [7]. The air flow is simulated by an analogous electrical circuit, see figure 6. For different parts of the microphone unit various analogous equations were used. The parts are separated into mechanical and acoustical components [8].

The model itself is applicable for both package types. Only the values of some parameters change, especially in the entry of the ceramic. The affected values are R_{in} (friction between the moving air and the wall of the sound hole), M_{in} (mass inertia of the air in the sound hole) and C_{in} (compression of the air in the front volume). In the new stacked package design the front volume is a little bigger than in the original CSMP. As a consequence C_{in} increases. Also the number and diameter of the holes are different which affects the values of R_{in} and M_{in}.

Figure 7 shows the calculated frequency response for both CSMP package types compared to a simulated conventionally packaged microphone assuming a 40 times higher front volume and a sound inlet with a diameter of 1 mm. As can be seen, the bigger front volume of the stacked design generates a slightly higher unwanted resonance peak than the original CSMP. But compared to conventionally packaged microphones the resonance is still negligible. This is due to the comparably small front volume and also due to an acoustical low pass filter generated by the small entry holes in the ceramic. This low pass filter can be mathematically described by an RLC oscillator.

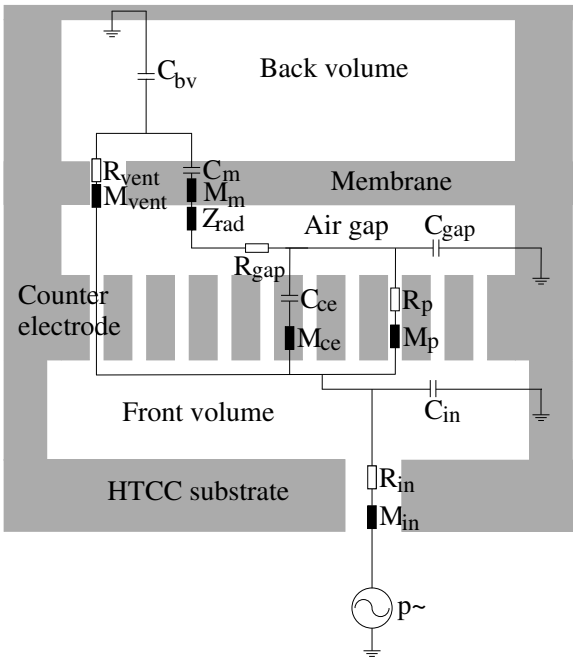


Figure 6: Electroacoustic equivalent circuit of the microphone system.

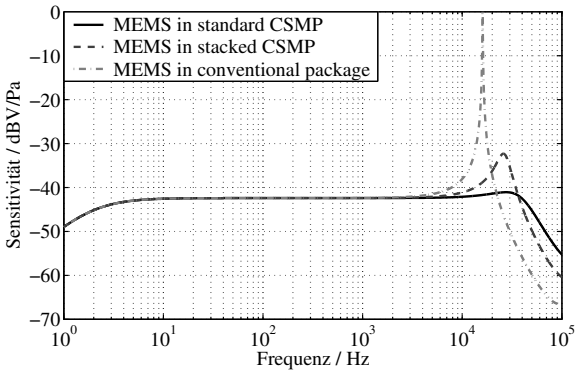


Figure 7: Theoretical frequency response of both package types compared to a conventionally packaged microphone.

MEASUREMENT RESULTS

Figure 8 shows a comparison between the measured and the simulated frequency response of the MEMS microphone in the stacked chip scale MEMS package. The measurement was performed in free field and is in remarkably good agreement with the calculation.

Another small influence of the package on the electroacoustical performance is caused by mechanical stress on the MEMS chip. The thermal expansion coefficient of ceramic material is 8 ppm/K, the thermal expansion of silicon is about 3 ppm/K, and so the mismatch is quite small. Nevertheless, when cooling down the microphone from a soldering temperature of up to 260°C the shrinkage of the substrate is larger than the shrinkage of the MEMS chip which causes compressive stress at room temperature on the MEMS chip. The compressive stress leads to a decrease of the intrinsic tensile stress of the poly-silicon membrane thus the sensitivity of the microphone is increased.

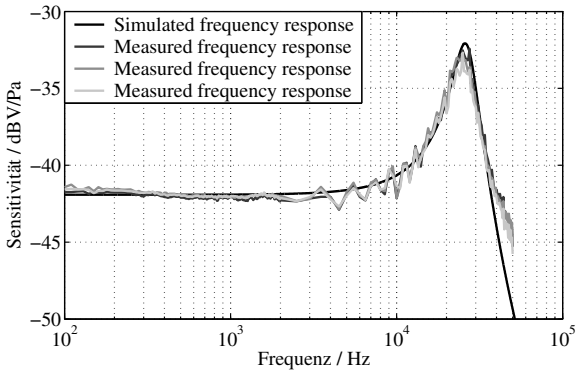


Figure 8: Comparison between simulated and measured frequency response of the new CSMP package. Three microphones were measured in a free field measurement setup.

Since the mechanical stress caused by temperature changes influences the sensitivity of the membrane, the effect of a reflow process on a PCB was investigated (see figure 9). The sensitivity shift by a soldering process was measured to be less than 0.5 dB.

CONCLUSION

In this paper the next step in miniaturization for a chip scale MEMS package is presented. This was achieved by placing the ASIC inside a cavity in a HTCC substrate underneath the MEMS microphone. A rigid foil closes the acoustic back volume of the device. ASIC and MEMS chips are flip chip bonded on an HTCC substrate with holes for the sound entry. The package is closed by conformal lamination of a polymer foil and metallization. The frequency response was calculated using an analytical model and the calculations were verified by acoustic measurements in free field. Measurement showed that the change of sensitivity in a reflow process caused by package stress is small.

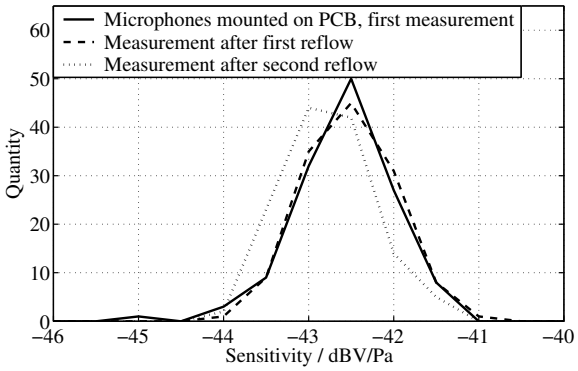


Figure 9: Distribution of sensitivity after soldering, first and second reflow.

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