WAFER SCALE ENCAPSULATION OF LARGE LATERAL DEFLECTION MEMS STRUCTURES

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ABSTRACT

Packaging of microelectromechanical systems (MEMS) is a critical step in the transition from product development to production. This paper presents a robust, hermetically-sealed encapsulation method that can accommodate many traditional MEMS devices by allowing large lateral deflection structures within a clean environment. Using the new technology described in this paper, trench widths ranging from 1µm to 100µm were successfully encapsulated at the wafer level while maintaining devices as thick as 20µm. Devices produced with this method have proven durable enough to withstand harsh post-processing such as dicing and wire bonding. Two different types of MEMS resonators are also discussed, demonstrating the use of both large and small trench widths within the encapsulation.

INTRODUCTION

Microelectromechanical systems (MEMS) are increasingly moving from expensive prototypes to commercial products. A critical step in this process is the packaging of such devices. Not only does the packaging serve as protection from the external environment, but it must provide a controlled environment in which to operate the device. A detailed description of the challenges involved in the packaging and assembly of MEMS is provided by *Najafi* [1]. Packaging methods can be broadly categorized into two categories: device level and wafer level packaging. Because device level packaging often involves handling each individual part (typically decreasing yield and increasing cost), wafer level packaging has experienced increasing attention.

The most commonly used method of encapsulating at the wafer level is bonding a separate substrate (typically glass or silicon) onto completed structures [2]. While this method has been successful, thin-film encapsulation (depositing a structural cap layer on top of a sacrificial layer) has several advantages. By encapsulating as part of the fabrication process, the overall package footprint only needs to be slightly larger than the device itself, leaving just enough material to maintain structural integrity. This method also allows for vertical electrical interconnects, which has the potential to further reduce die area. Alternatively, bonded packages require sufficient bonding area to fully enclose the structure, and they typically increase the overall package thickness due to the bonding cap. For these reasons, we have chosen the method of encapsulating by means of a deposited cap layer.

In work preceding that discussed here, *Candler et al.* demonstrated the encapsulation of piezoresistive and capacitive structures by depositing a thin film epitaxial polysilicon cap, etching vent holes in the cap to provide access to the sacrificial oxide, etching the sacrificial material, and closing the access holes using a low pressure chemical vapor deposition (LPCVD) silicon dioxide [3]. In addition, the sealing step was performed directly after the release etch in a cleanroom environment, with no intermediate processing that could cause additional contamination. This process had greater than 90% yield for capacitively actuated, double-ended tuning fork resonators. Similar resonators were later used by *Kim et al.* to demonstrate the stability of an 'epi-seal' encapsulation in which the etch access holes were sealed using a second epitaxial silicon deposition rather than LPCVD silicon dioxide [4]. Their work showed that the resonant frequency stayed within the measurement uncertainty for a period of over one year.

While the 'epi-seal' encapsulation technique developed jointly by Stanford and Bosch has produced devices in a very stable and robust environment, many common MEMS structures cannot be encapsulated using such a technology due to its design constraints. For example, the current rules for designing in such a process limit maximum trench widths to 2µm, preventing the incorporation of even basic comb-drive structures. *Ayanoor-Vitikkate et al.* attempted to address this using a timed thermal oxidation of sacrificial beams to fill in trenches as wide as 10-20µm, but working devices have yet to be demonstrated using this method [5].

In this paper, we describe a clean, robust, hermetically-sealed encapsulation method that can accommodate more traditional MEMS devices by allowing large lateral deflection structures. The process addresses the previous trench width limitations by filling in wider trenches via the deposition of a very thick plasma enhanced chemical vapor deposition (PECVD) silicon dioxide layer (up to 23µm). Devices produced with this encapsulation method have proven durable enough to withstand harsh post-processing such as dicing and wire bonding. We also present two different types of functioning MEMS resonators fabricated within this encapsulation.

FABRICATION

The fabrication process begins with silicon-on-insulator (SOI) wafers having a 2µm thick buried oxide and device layer thicknesses that varied among 5µm, 10µm, and 20µm. As shown in Fig. 1(a), the first step is to define the functional layer using a deep reactive ion etch (DRIE). Because this step includes both high and low aspect ratio trenches, an etch recipe was developed that eliminates "grassing" in wide trenches while maintaining feature critical dimensions in narrow trenches. This recipe included adding decreasing C_4F_8 passivation gas during the first few minutes of the etching, similar to the process outlined by *Liu* [6].

A thick silicon dioxide is then deposited via PECVD

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using a silane and nitrous oxide chemistry, as shown in Fig. 1(b). PECVD was chosen over the two LPCVD (low pressure chemical vapor deposition) methods available to us for its rapid deposition rate, good conformality and low stress. While the standard 'epi-seal' process only needs 2-3μm of oxide to seal over the narrow trenches and provide the upper sacrificial layer, as much as 23μm of oxide is deposited here to fill in the wide trenches found on the 20μm device layer wafers. This ensures that the minimum height of the oxide is above the top of the device layer. The film stress of the PECVD oxide was measured to be -160MPa.

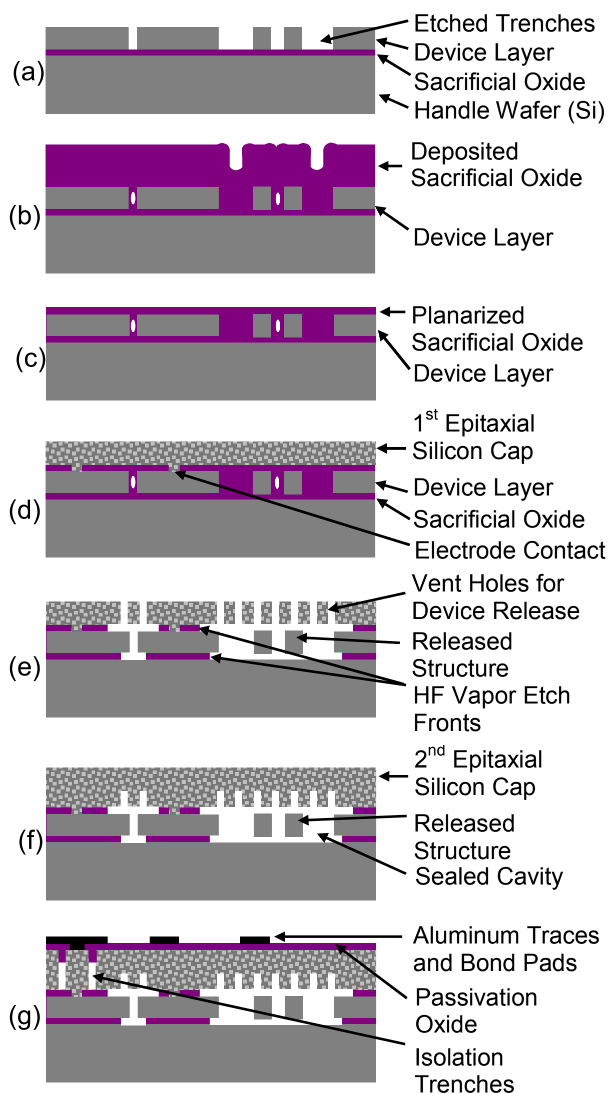

Figure 1: Wafer-scale encapsulation fabrication steps (a) SOI wafer after deep reactive ion etching (DRIE). (b) Thick silicon dioxide deposition. (c) Plasma planarization. (d) First epitaxial silicon deposition. (e) DRIE vent etch and HF vapor etch to release devices. (f) Epitaxial silicon deposition to seal devices. (g) Electrical isolation and metallization for bond pads and metal traces.

A combination of plasma planarization and chemical-mechanical polishing (CMP) is then used to planarize this sacrificial layer. After coating with photoresist, the plasma planarization is performed using CHF_3, CF_4, Ar, and O_2 as etch gases, followed by a short CMP using silicon dioxide specific slurry. This results in a surface topology that is suitable for subsequent lithography steps while resulting in oxide-filled trenches, shown in Fig. 1(c). Electrical contact vias are then etched in the silicon dioxide to allow contact with various device layer electrodes.

The 20μm thick epitaxial silicon encapsulation layer, shown in Fig. 1(d), is deposited at 1080°C using Dichlorosilane, hydrogen, and Phosphine as a dopant gas. Small trenches (approximately 0.7μm by 8μm) are etched through the cap to provide access to the sacrificial oxide for the subsequent release etch. To prevent stiction problems, devices are released using a hydrofluoric acid vapor etch, seen in Fig. 1(e). As the HF vapor etches the sacrificial and buried silicon dioxide layers, etch fronts are monitored using an infrared microscope to determine when the release etch is complete.

Wafers are then immediately sealed using a second epitaxial silicon deposition, shown in Fig. 1(f). Performed at 1080°C and 40mbar, this deposition includes gaseous hydrochloric acid to achieve a recipe that is selective between the silicon and oxide. This prevents silicon deposition on the silicon dioxide layers separating the handle wafer, device layer, and encapsulation layer, which would create electrical shorts. An important feature of the sealing process is that it results in a single crystal silicon device layer free of native oxide. As the deposition chamber is being brought up to temperature, the released and unsealed wafer is only exposed to hydrogen gas. By reacting hydrogen with the thin native oxide at temperatures in excess of 1000°C, the native oxide is consumed leaving a pure silicon surface [7]. The primary gas remaining in the encapsulated cavity following the seal is hydrogen.

Several straightforward steps are then taken to complete the fabrication, as shown in Fig. 1(g). An isolation trench is etched to isolate electrical contacts, followed by the deposition of a silicon dioxide passivation layer. After opening contacts in the oxide, aluminum is deposited, patterned, and etched to create the wire traces and bond pads necessary for testing.

To reduce the pressure inside the sealed cavity, the wafers are placed in a nitrogen furnace at 400°C. As discussed by *Candler et al.*, although nitrogen will begin to slowly diffuse into the cavity, the much smaller hydrogen molecules diffuse out at a much higher rate, reducing the pressure inside the encapsulation [8]. A high temperature vacuum anneal would allow a further reduction in the amount of hydrogen, however a tool capable of this was not available at the time of processing.

RESULTS AND DISCUSSION

Using the process described, numerous functioning devices were successfully encapsulated. Among these are structures that include design features not possible in any previous iteration of the 'epi-seal' fabrication process, most notably trenches ranging from 1μm to 100μm wide. An important outcome of the increase in allowable trench widths is the inclusion of comb-drive structures. As examples, Fig. 2 shows a fully released comb-drive structure prior to the sealing step and Fig. 3 shows the interdigitated comb-drive fingers of a sealed device. Note that the structure in Fig. 2 broke as part of the preparation of the sample for the SEM.

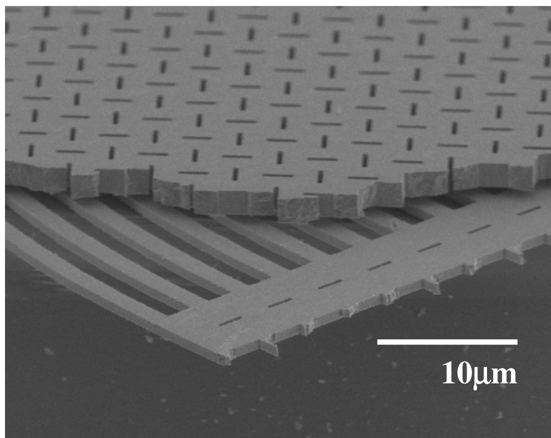

Figure 2: SEM cross-section showing vents etched into the first epitaxial silicon cap layer (top-most layer) over part of a released comb drive resonator.

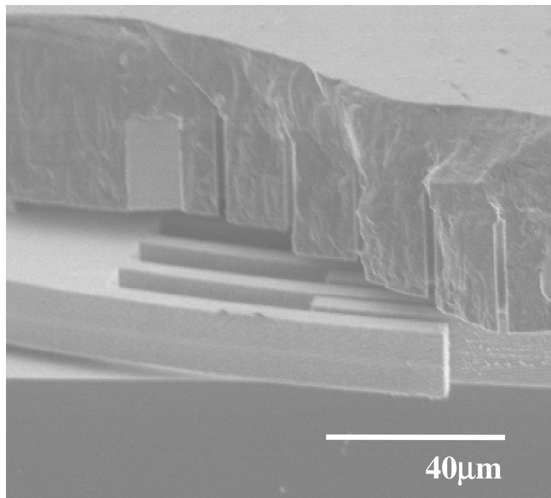

Figure 3: SEM cross-section of released and sealed interdigitated comb-drive fingers.

Though the intention of this new method was to allow the encapsulation of large deflection devices, it is still quite suitable for encapsulating the narrow trench devices found in other fabrication processes. Double-ended tuning fork resonators, similar to those previously encapsulated [4], were fabricated. Because the quality factor is limited by damping in such resonators, these structures were used to monitor pressure changes within the encapsulation by measuring their quality factor at various times during the hydrogen diffusion anneal, as shown in Fig. 4. The pressure is estimated to be well below 10mbar at room temperature based on the sealing pressure and temperature. *Candler et al* showed that the pressure can be reduced to less than 1mbar for a similar encapsulation process and demonstrated a method for determining pressure from quality factor [8].

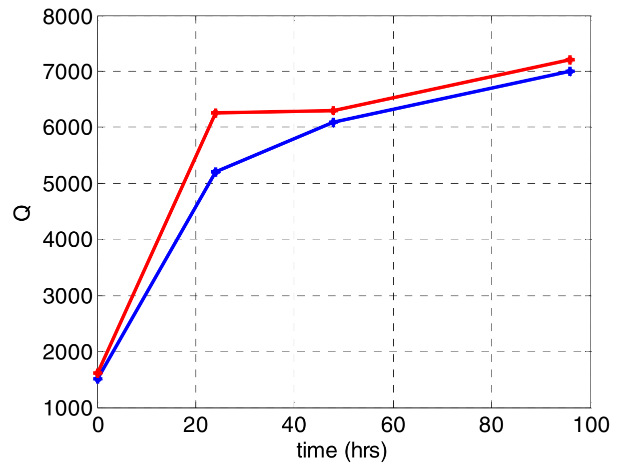

Figure 4: Plot of resonator quality factor, Q, increasing with anneal time in a 400℃ nitrogen ambient, corresponding to a decrease in the cavity pressure. Plot shows data for two different devices. Cavity pressure is estimated to be below 10mbar.

As it is the driving force of this work, large lateral deflection devices were also successfully encapsulated. Among these is a comb-driven, resonating fan structure for studying fatigue, shown in Fig. 5, that has been electrostatically actuated to achieve a displacement of 8.6μm and a stress of 1.6 GPa (calculated). The frequency response of this test structure is shown in Fig. 6. As frequency is sensitive to many environmental factors, the constant temperature frequency stability of ±3ppm over 700 hours of operation (at low amplitude) demonstrates the robustness of the encapsulation method, as seen in Fig. 7. More details on the testing of this structure are available elsewhere in these proceedings [9].

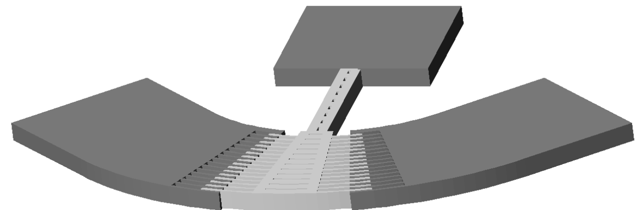

Figure 5: CAD drawing of a functioning comb-drive resonator encapsulated in this process.

It is often the case that wafer singulation and electrical contact to external circuitry are areas of concern for MEMS devices. The hermetic epitaxial silicon encapsulation presented here, however, is very robust and allows for dicing using a wafer saw and electrical contact via wire bonding without affecting the device integrity. For working devices, there was no loss in yield in going from completed wafers (tested using a probe station) to individual devices that were diced in a wafer saw, epoxied into packages, and wire bonded to those packages.

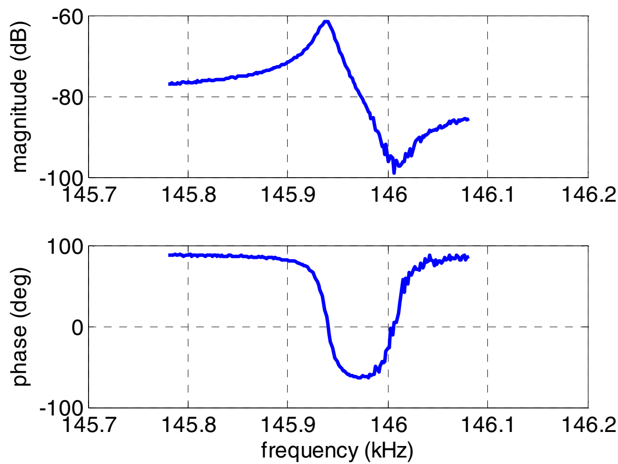

Figure 6: Plots of gain and phase versus frequency for a large deflection comb-drive resonator.

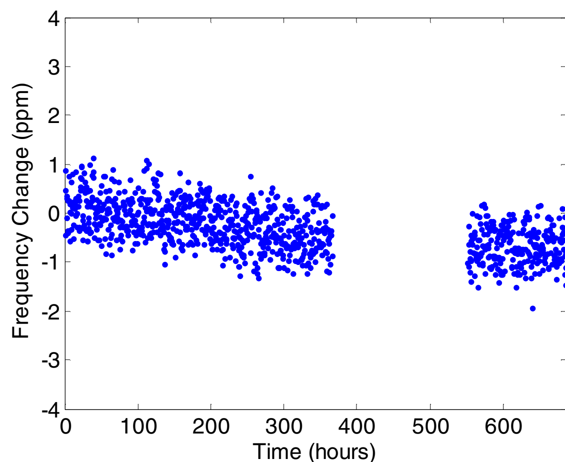

Figure 7: Plot of frequency change versus time for a large deflection comb-drive resonator operating at a nominal frequency of 137kHz. Temperature was maintained at 29°C±0.1°C. The loss of data between 400-600 hours is a result of a memory error during data acquisition, but the device was continuously operating during this time.

CONCLUSIONS

With this fabrication platform, devices with large lateral displacements can now be packaged at the wafer-scale into a stable, hermetic environment. The method of encapsulation has proven durable enough to withstand standard backend processing such as dicing and wire bonding, with no loss of performance. This has the potential to improve the reliability, performance and yield of common devices such as gyroscopes, accelerometers and comb-drive structures. In addition, the well-controlled environment can be used for fundamental studies of surface phenomenon such as fatigue, adhesion, and friction. Future work will focus on characterization of devices fabricated using this technique.

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