NOVEL TECHNOLOGY FOR CAPACITIVE PRESSURE SENSORS WITH MONOCRYSTALLINE SILICON MEMBRANES

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ABSTRACT

We report on a novel surface micromachining technology for the fabrication of capacitive absolute pressure sensors. The pressure sensitive membrane is formed by single crystal silicon enabling excellent long term stability. The membrane formation is based on the Advanced Porous Silicon Membrane (APSM) process [1], which is currently applied to piezoresistive transducers. Expanding this technology to capacitive transduction allows for a greater flexibility in tailoring the sensor properties to specific applications [2]. This expansion is implemented by adding a poly-Si counter electrode layer on top of the membrane in a surface micromachining step. Since only front side processing on standard silicon substrates is used, this method is very cost-efficient and fully CMOS-compatible, enabling monolithic integration of circuitry.

INTRODUCTION

A widely-used approach for the fabrication of capacitive MEMS pressure sensors is surface micromachining (SMM) [3]. Typically, on top of a silicon substrate a sacrificial silicon dioxide film is etched from underneath a polysilicon layer creating a cavity. SMM processes allow for fully CMOS compatible, low cost capacitive pressure sensors, since only front side processing is used. On the other hand, the formation of stress-free polysilicon is difficult [4]. Furthermore, the necessary subsequent sealing of the cavity typically done with dielectric layers is a possible weak spot regarding long term stability and leak tightness.

A second bulk micromachining approach uses continuous single crystal silicon membranes as pressure sensitive element leading to higher mechanical stability. The diaphragm is formed by a shallow KOH etch on the front surface and a deep etch from the backside. The surface side is then attached to a glass plate by electrostatic bonding. The latter is provided with a thin metal film serving as counter electrode [3]. Due to the backside processing, large required space and additional need of a glass wafer bulk micromachined pressure sensors are quite cost-intensive.

Recently, a concept for a capacitive pressure sensor with a boss membrane using the APSM technology was reported [5]. The APSM process enables fabrication of self-sealing single crystal membranes above a vacuum cavity. The novel concept presented in this paper combines the benefits of both approaches mentioned above. First, it provides a continuous single crystal pressure sensitive membrane taking advantage of its unique properties like high strength, high reliability and no mechanical hysteresis. Second, this membrane as well as the polycrystalline counter electrode added on top of it is formed by only using front side and fully CMOS-compatible process steps. Third, since the dimensions of the electrodes are confined by an etched trench instead of a *pn*-junction and the electrodes are isolated by a dielectric layer, the sensor is designed for stable temperature behaviour.

SENSOR CONCEPT

A schematic view of the sensor concept is displayed in Figure 1a). The sensing element consists of a single crystal silicon membrane covering a vacuum cavity which serves as pressure sensitive lower electrode. To realize the capacitive measuring principle a perforated polysilicon counter electrode is added on top of the membrane. A thin silicon oxide layer separates and electrically isolates the electrodes. To define the lateral confinement of the counter electrode and thereby reduce the parasitic capacitance of the sensor, an additional trench is etched around the membrane region. The vent-holes allow the applied pressure to penetrate the polysilicon electrode and deflect the single crystal membrane. With a proper design of the vent holes the perforated polysilicon electrode is not affected by the pressure. Therefore the deflection results in a variation of the electrode gap. This can be detected electrically as a change of capacitance ΔC.

To reduce temperature dependence and parasitic capacitances, an additional reference element is used [6]. This is identical to the sensing element except for the cavity (Figure 1b)). Hence, in case of the reference element

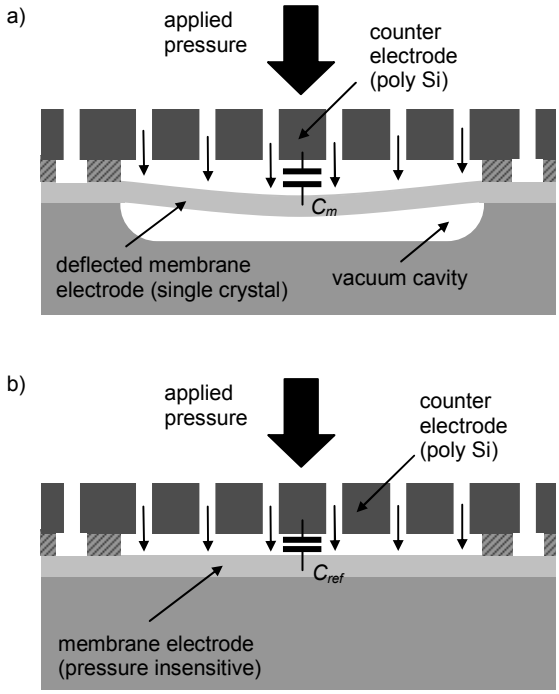

Figure 1: Functional principle of capacitive transducer: a) sensing element: applied pressure deflects single crystal membrane covering a vacuum cavity, b) reference element without cavity providing a pressure insensitive membrane electrode.

the single crystal lower electrode is pressure insensitive. Therefore, by taking the difference between the two capacitances, most temperature and parasitic effects can be eliminated.

FABRICATION

The fabrication process of the capacitive sensor is described by means of schematic cross-sectional illustrations (Figure 2)). It consists of the APSM process [1] for the single crystal membrane formation (Figure 2a)-c)) and some further SMM process steps for the implementation of the counter electrode (Figure 2d)-f)).

Process flow

The core of the APSM process is the so-called anodization, during which the silicon substrate is locally porosified by electrochemical etching in concentrated hydrofluoric acid (HF). Starting material is a moderately *p*-doped silicon substrate with (100)-orientation.

First, a deep n^+-doping and a shallow p^+-doping are implanted to the substrate. The n^+-doping, which is not porosified during the anodization [7], serves as lateral confinement of the membrane region into the bulk substrate. It is designed as quadratic frame enclosing a shallowly p^+-doped area (cf. Figure 2a)). The p^+-doping subsequently serves as single crystal seed layer for the epitaxial growth of silicon. Additionally, a silicon nitride layer is deposited onto the wafer to avoid porous etching of the substrate surface. The subsequent anodic etching in concentrated HF is performed in a two step process. First, the p^+-Si layer is etched using a low current density resulting in a mesoporous silicon layer. Second, the subjacent *p*-Si is anodized with an increased current density leading to a nanoporous silicon layer buried under the mesoporous layer (Figure 2a)). Afterwards, the silicon nitride layer is removed in HF solution. In a CVD reactor the substrate is then exposed to a hydrogen atmosphere. At temperatures between 900°C and 1100°C the hydrogen desorbs native oxide residuals from the porous silicon surface. As soon as the oxide is removed, both porous silicon layers start to rearrange driven by the minimization of the surface energy: the surface pores in the mesoporous layer are sealed, while the buried nanoprous silicon starts to merge into one single cavity (Figure 2b)).

In the same CVD reactor, an epitaxial Si-layer is grown, using the sealed mesoporous silicon as a seed layer. Simultaneously, any porous silicon has completely rearranged leaving one single cavity (Figure 2c)). The thickness of the epitaxial layer (~10 µm) defines the membrane thickness. The hydrogen enclosed inside the cavity diffuses through the silicon during subsequent high temperature processes leaving a vacuum.

This membrane constitutes the pressure sensitive first electrode of the capacitive transducer. The pressure insensitive counter electrode is implemented as follows.

First, a thin (~1 µm) silicon oxide film is deposited onto the Si-epitaxy. It serves as sacrificial layer and defines the electrode gap. In the contact area of the membrane the oxide is removed by wet etchig (Figure 2d)). In a CVD reactor, a second silicon layer of ~10 µm is subsequently deposited. In the etched area the Si-layer grows as a single crystal onto the substrate preparing the membrane contact. At the same time, the deposition on the sacrificial

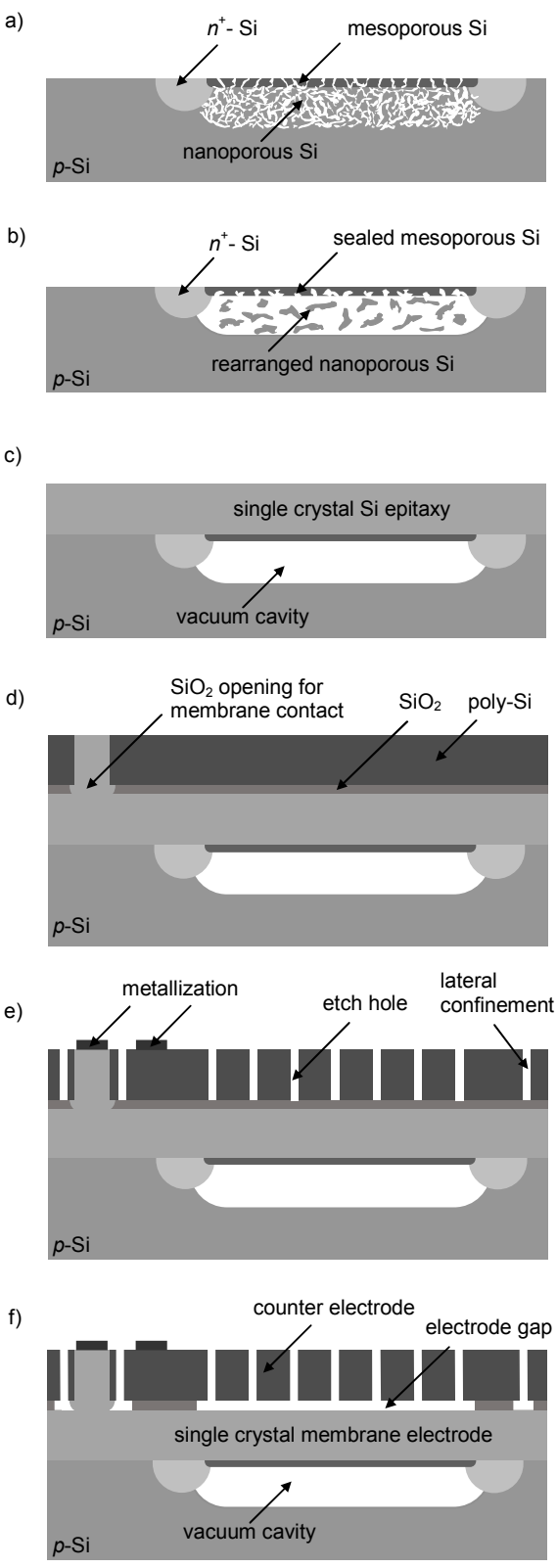

Figure 2: Schematic process flow: a) porous etching of mesoporous seed layer and nanoporous cavity layer, b) thermal rearrangement of porous silicon during hydrogen prebake, c) sealing of cavity by lateral overgrowth during Si epitaxy, d) deposition and structuring of sacrificial layer (SiO_2) and deposition of poly-Si (counter electrode), e) metallization and perforation of poly-Si by DRIE, f) removal of sacrificial layer by HF vapor etch and thereby releasing membrane from counter electrode.

oxide results in a polysilicon layer, which constitutes the pressure insensitive counter electrode (Figure 2d)).

After depositing and structuring an Al metallization layer for the electrical connection of the electrodes, the membrane region of the polysilicon layer is provided with access holes by DRIE (Deep Reactive Ion Etch) (Figure 2e)). The dimensions of the holes (2-3 µm diameter and 15-19 µm distance) result from the trade-off between maximizing the sensing capacitor area and minimizing the duration of the sacrificial layer etching. With the same DRIE step the trenches for separating the membrane contact from the poly-Si layer and confining the counter electrode are etched. By means of HF vapor etching through the vent holes the sacrificial silicon oxide is removed in the membrane region (Figure 2f)) and the electrodes are released.

Results

Figure 3 pictures cross-sectional SEM micrographs of the cavity and membrane region at certain process steps. Figure 3a) shows the cavity region after anodization. In the whole membrane region a double porous stack with an upper mesoporous layer and a buried nanoporous layer were generated.

Figure 3b) displays the cavity region after hydrogen prebake. Driven by the minimization of the free surface energy, both porous silicon layers start to rearrange. The buried nanoporous silicon shows a coarsened morphology, while the upper mesoporous layer is sealed providing the seed layer for the epitaxial growth. Since the rearrangement of porous silicon is solely thermally activated, it continues with each high temperature process, even in the sealed cavity, until a single cavity is formed.

Figure 3c) shows the membrane and cavity region after the deposition of an approximately 10 µm thick Si-membrane. The porous silicon has now completely rearranged creating a single vacuum cavity. The Si epitaxy is grown onto the sealed mesoporous silicon. Since the mesoporous silicon layer and thereby the Si growth is perfectly single crystalline, a high quality single crystal silicon layer is formed. The mesoporous layer is part of the membrane and has been completely smoothed by thermal rearrangement.

Figure 3d) shows the final membrane stack above a vacuum cavity after HF vapor etching. The silicon dioxide layer has been fully undercut and removed, resulting in two freestanding membranes: a continuous lower silicon membrane and a perforated upper membrane. The latter shows the typical polycrystalline structure, in contrast to the perfectly single crystal lower membrane. The cut through the vent-hole shows the characteristic periodic profile of the DRIE. The gap between the membranes corresponds to the sacrificial oxide thickness of 1 µm.

Top views of the sensing element are given in Figures 4. Figure 4a) shows the single crystal lower membrane before the sacrificial layer deposition. Membrane electrode and contact area are connected by an n^+-doped conductive path. A p^+-guard ring surrounds the whole membrane and contact region confining the lower electrode by a *pn*-junction. Due to the vacuum inside the cavity the single crystal membrane is slightly bent under atmospheric pressure. This is visualised as contrast given by a DIC (Differential Interference Contrast) microscope,

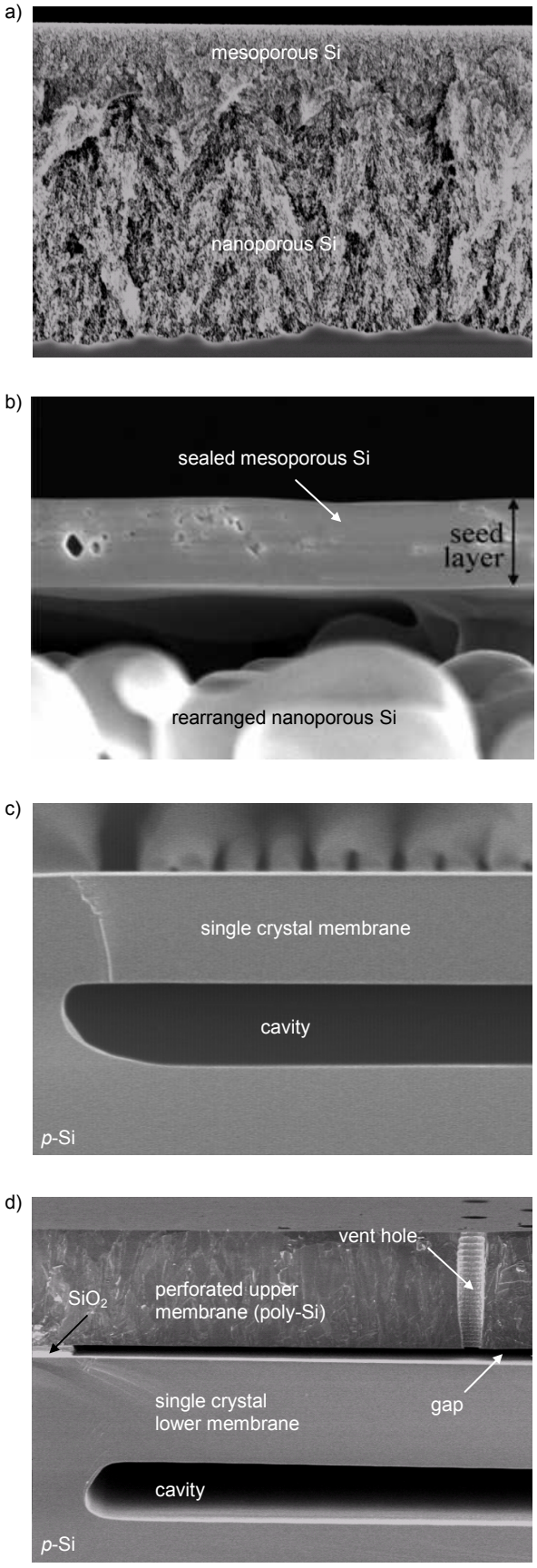

Figure 3: Cross-sectional SEM micrographs of the cavity and membrane region a) nanoporous and mesoporous layer after anodization, b) rearranged porous silicon layers after hydrogen prebake, c) single crystal membrane and cavity after epitaxial deposition, d) full membrane stack after etching the sacrificial layer.

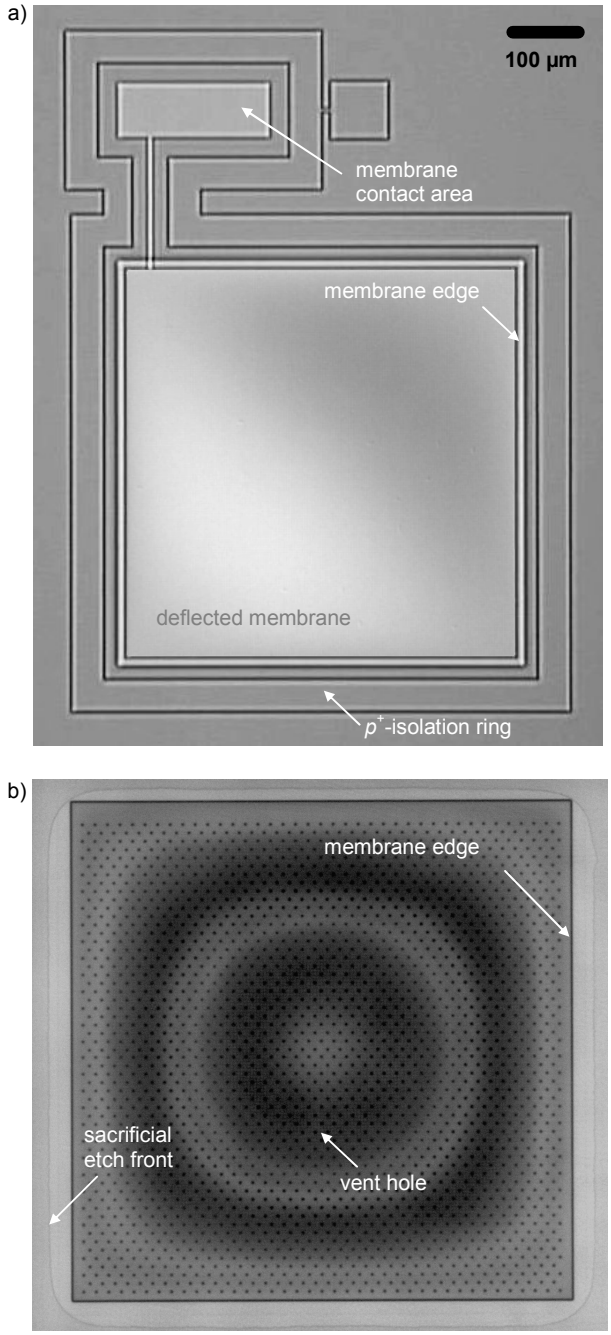

Figure 4: Top view of the sensing element: a) optical microscope view before sacrificial layer deposition, b) infrared microscope view after sacrificial layer etching.

which detects the optical path difference generated by the deflected membrane (Figure 4a)).

Figure 4b) shows an infrared microscope view of the membrane region after the full process demonstrating the relative position of the membrane stack. The polysilicon perforation is centered above the cavity region (indicated by the membrane edges). The etch front of the sacrifical oxide layer reaches the membrane edge releasing the whole single crystal membrane. The apparent Newton's Rings indicate that the capacitor plates are not coplanar. This is attributed to the deflection of the single crystal lower membrane.

CONCLUSIONS

This paper introduces a novel technology for the fabrication of capacitive absolute pressure sensors. Single crystal silicon serves as material for the pressure sensitive membrane electrode and a perforated polysilicon layer as pressure insensitive counter electrode. The single crystal membrane is formed using the APSM process. The main process steps are: (i) local anodic etching of porous silicon in concentrated hydrofluoric acid; (ii) sintering of the porosified areas in hydrogen atmosphere at elevated temperature; (iii) epitaxial growth of the monocrystalline membrane onto rearranged porous silicon [1]. The counter electrode is added on top by deposition of a thin oxide and a thick polysilicon layer. The sacrificial oxide layer separates and electrically isolates both membranes. The vent holes allow the applied pressure to reach and deflect the single crystal membrane.

By using a self-sealing continuous single crystal membrane as pressure sensitive electrode, the sensor elements exhibit high long term stability and leak tightness. Since the thickness of the sacrificial oxide layer defines the electrode gap, a considerably smaller and well-defined gap than previously [5] can be achieved leading to higher capacitance and sensitivity. Finally, by using only CMOS compatible, front side process steps on standard silicon substrates this method is very cost-efficient and allows for the integration of circuitry.

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