GOLD-INDIUM TRANSIENT LIQUID PHASE (TLP) WAFER BONDING FOR MEMS VACUUM PACKAGING

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ABSTRACT

This paper reports the first wafer-level vacuum packages created with gold-indium transient liquid phase (TLP) wafer bonding. The packages were bonded at 200 °C for 1 hour under a vacuum environment in a commercially available wafer bonder. After bonding, the integrated getters were activated for 1 hour resulting in internal pressures as low as 200 mTorr. The pressures have been stable for over 6 months as measured by integrated Pirani gauges. Although no leak rate trend has been observed, the worst case leak rate that fits within the error of the pressure measurement is 16 mTorr/year ($1 \cdot 10^{-16}$ atm.cc.s^{-1}).

1. INTRODUCTION

Some MEMS, such as resonant devices and thermal imagers, need a vacuum environment for maximum performance [1-2]. These devices take advantage of several advantageous effects that are provided by the reduced gaseous molecular density at vacuum pressures. A vacuum package will provide high quality factors for low-frequency resonant devices by reducing squeeze-film damping and high thermal isolation for infrared imagers by reducing gaseous thermal conduction. Creating wafer-level MEMS vacuum packages is a challenge because of their small scale. With internal volumes that can be smaller than 1 μL, only a high quality hermetic seal will provide the barrier necessary to maintain long-term vacuum. These high quality hermetic seals can only be provided by certain wafer bonding techniques.

Several different types of wafer bonding have been used to create wafer-level vacuum packages. Anodic, Fusion, and Eutectic bonding can all create the high-quality robust hermetic seals that are required for MEMS vacuum packaging [3]; however, they are all processed at temperatures that may preclude the use of some temperature sensitive materials. Typically temperatures of greater than 350 °C are required for reliable bonding with these techniques, which is too high for some materials such as the dielectrics used in next generation CMOS circuits [4].

Transient Liquid Phase (TLP) bonding is an advanced type of solder bond that can form high-quality hermetic seals at lower temperatures than other bonding techniques. Previously, TLP bonding has been reported as a low-temperature die attachment technique for high powered semiconductor die [5] and recently as a wafer-level vacuum packaging technique formed at 300 °C [6]. This paper reports a gold-indium TLP metallurgy that is created at 200 °C for very low temperature vacuum packaging.

2. DESIGN

A TLP bond is formed by sandwiching a low melting point interlayer between two parent metals. The bond proceeds through 4 stages during the formation process (see Fig. 1). In the first stage, the parent metals and interlayer are put into contact. Next, the assembly is heated to melt the interlayer. In stage 2 the molten interlayer flows over and seals wafer topography, such as lateral feedthroughs. During this stage the molten interlayer rapidly reacts with the parent metals to form higher melting point intermetallic compounds. In the third stage, the joint undergoes isothermal solidification as the last of the liquid interlayer is transformed into intermetallic compounds.

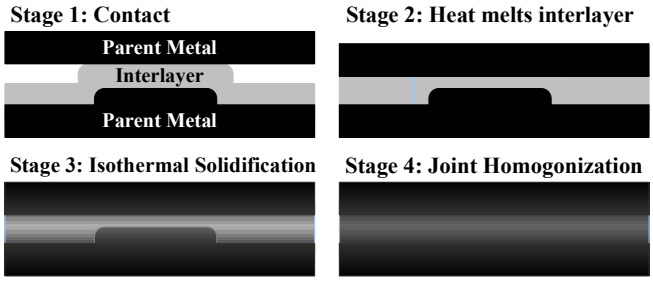

Figure 1: The 4 stages of TLP bonding.

After the transformation of the interlayer, the melting temperature of the joint is raised from the melting point of the interlayer (156 °C, see Fig. 2) to the melting point of the intermetallic compound (540.7 °C). In stage 4 further heating increases the quality of the bond as the intermetallic compounds diffuse away from the bond interface leaving behind a continuous pure parent metal.

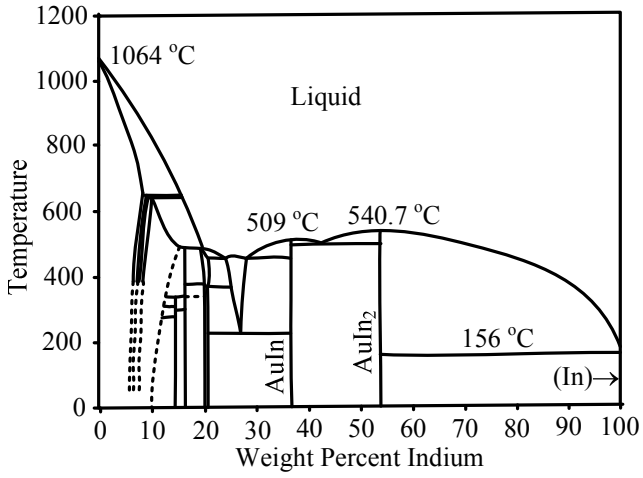

Figure 1: The gold-indium binary phase diagram [7].

Several factors need to be considered when designing a fluxless TLP bond. The material system, the thickness interlayer metal, and the heating rate, will determine the final quality of the bond.

Temperature Constraints

The materials used to create the TLP bond will determine the bonding temperature and the maximum temperature it can survive after completion. The formation temperature of the bond is just above the melting point of the interlayer and is thus dictated by its choice. Indium and tin are the most widely used interlayer metals because of their low melting points (156°C and 232°C, respectively). The choice of the parent metals will determine the final melting temperature of the joint. Material systems like silver-indium and silver-tin offer the greatest increase in re-melting temperature due to the high melting temperature of the silver intermetallics. Table 1 lists several TLP bonds reported in the literature.

Table 1: TLP Bond results reported in the literature. Adapted from [8]

Material System	Bonding Process	Remelt Temp.
Copper - Tin	4 min at 280 °C	> 415 °C
Silver -Tin	60 min at 250 °C	> 600 °C
Silver - Indium	120 min at 175 °C	> 880 °C
Gold - Tin	15 min at 260 °C	> 278 °C
Gold - Indium	0.5 min at 200 °C	> 495 °C
Nickel - Tin	6 min at 300 °C	> 400 °C

Void Formation

MEMS vacuum packaging requires high-quality void-free wafer bonds. For void-free TLP bonds, the thickness of the interlayer is the most critical design parameter [9]. As the joint is heated, even before the interlayer melts, it reacts with the parent metals and forms intermetallic compounds in the solid-state. If the heating rate is too slow, this interaction completely transforms the interlayer into intermetallics before its melting point can be reached. In this case, the interlayer never forms a liquid phase and won't fill any gaps in the joint between the parent metals, leaving voids in the final bond. A minimum interlayer thickness is required to ensure that there is still pure interlayer material left to melt when the assembly reaches the interlayer melting point. The minimum interlayer thickness that creates a voidless bond can be calculated from the heating rate used and the reaction rate between the parent metal and interlayer.

Fluxless Bonding

Fluxes are typically used in solder bonds to ensure good wetting by removing the native oxides from the metals involved in the bond. Good wetting is also required to produce good TLP bonds.

However, fluxes are not compatible with released MEMS devices; therefore the TLP bonding process must be fluxless. This can be accomplished by designing the bond so that the only metal oxides are those on the surface of the interlayer. The oxide on the interlayer will not prevent good wetting because with sufficient force during the bond, the force will break up the unsupported oxide covering the molten interlayer revealing clean interlayer underneath to wet the parent metals. The oxides on the parent metals, however, will prevent good wetting. Keeping the parent metals free from oxide can be accomplished by using a noble metal, such as gold, as the parent metal. Another way is to deposit interlayer material over the clean parent metal on both wafers. The interlayer covers both parent metals and prevents them from forming native oxides. A final technique for fluxless TLP bonding is to deposit a noble metal, such as gold, on top of the interlayer in-situ. Gold will form a skin of intermetallic compounds as it is deposited that will protect the interlayer from oxidation.

3. FABRICATION

The packages are created with a two wafer process. A device wafer containing Pirani gauges and a recessed cap wafer with getters are bonded together with gold indium TLP bonding.

Fabrication for the device wafer starts with a double side polished silicon wafer. The Pirani gauges are fabricated with a previously reported polysilicon surface micromachining process [10]. Next, a seed layer (1kÅ Cr – 2.5 kÅ Au) is sputtered over the Pirani gauge wafer. A photoresist mold masks the seed layer for the 300 μm wide, 5 μm thick gold bond rings that are electroplated around each Pirani gauge. After electroplating, the gold-chrome seed layer is etched. The Pirani gauges are released with a 40 minute buffered HF etch. During the seed layer and release etch steps, the electroplated gold bond rings are covered with photoresist for protection. After sacrificing the oxide, the photoresist is stripped in acetone, the wafer is rinsed in IPA and methanol, then the wafer is put into a critical point dryer (CPD) to prevent stiction of the gauges during final release. Finally, a 300 W oxygen plasma treatment removes the residue left by the CPD step.

The cap wafer process also starts with a double-sided silicon wafer. As with the device wafer, a seed layer of Cr/Au 1kÅ/2.5kÅ is sputtered onto the wafer, a photoresist mold is formed, and then a 5 μm thick 300 μm wide gold bond ring is electroplated onto the cap wafer. Next a 2 μm thick indium layer is evaporated onto the bond rings, followed in-situ by a 1 kÅ layer of gold that will form a protective layer of gold-indium intermetallics to prevent indium oxidation and enable fluxless TLP bonding. The indium-gold metal stack is patterned by a liftoff process. Similar to the device wafer, photoresist protects the bond rings during the seed layer etch and deep reactive ion etch thinning of the cap wafer. After thinning, Nanogetters™ from ISSYS are deposited on the cap wafer and patterned by liftoff. The cross section of the two wafers is shown in Fig. 2.

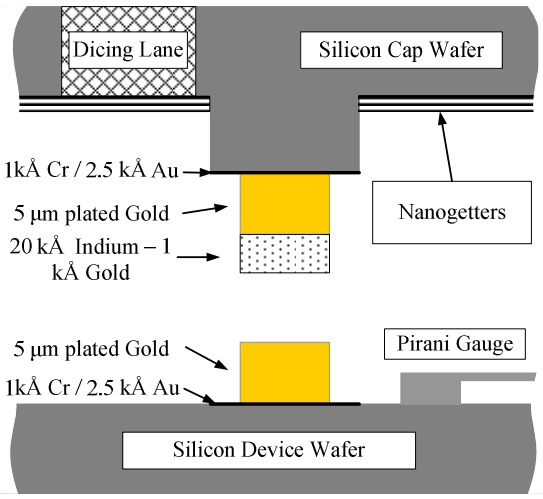

Figure 2: Cross section of the two wafers right before bonding.

The wafer pair is then aligned and bonded. Figure 3 shows the bond temperature profile and chamber pressure. It is critical to heat the wafers as fast as possible to ensure that the indium melts before it completely reacts with the gold parent metal to form higher melting point phases. The heating rate for this bond is ~ 60 °C/min. After heating to 200 °C the wafers are held for 1 hour to complete the bond. During the bond process, a force of 3000 N was applied to the wafer stack to make sure the thin gold-indium oxidation prevention layer is broken to reveal fresh molten indium during the bond. After completing the bond, the chamber is vented to atmosphere and the temperature is raised to 400 °C and held for 40 minutes to activate the Nanogetters and test the thermal robustness of the Au-In TLP bonds. After getter activation, the top wafer is diced to reveal the bond pads and the bottom wafer diced to singulate the packages.

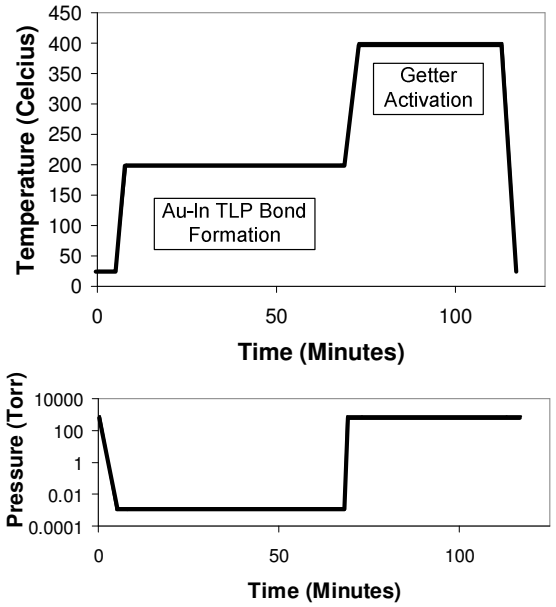

Figure 3: Temperature profile and chamber pressure during the bond cycle.

4. RESULTS

The gold-indium TLP bonding technique has been verified by bonding several different wafer pairs months apart with similar vacuum results each time. Figure 4 is a picture of a wafer with a magnified view of a de-capped die that shows the Pirani gauges and bond rings.

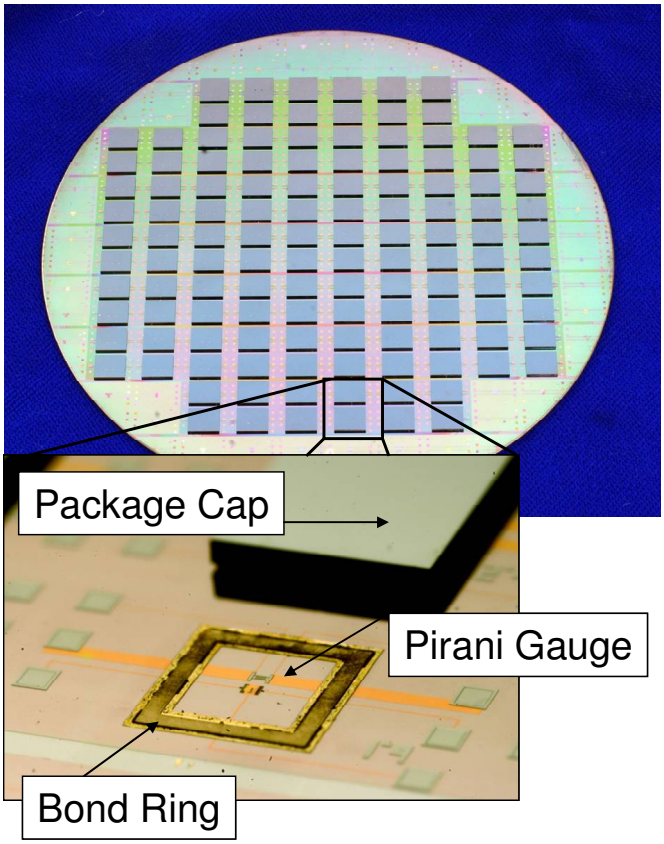

Figure 4: A completed wafer with a close-up of a de-capped die showcasing the Pirani gauge and bond ring.

Figure 5 shows a SEM image of the package cross section with magnified views of the gold-indium bond ring in the insets.

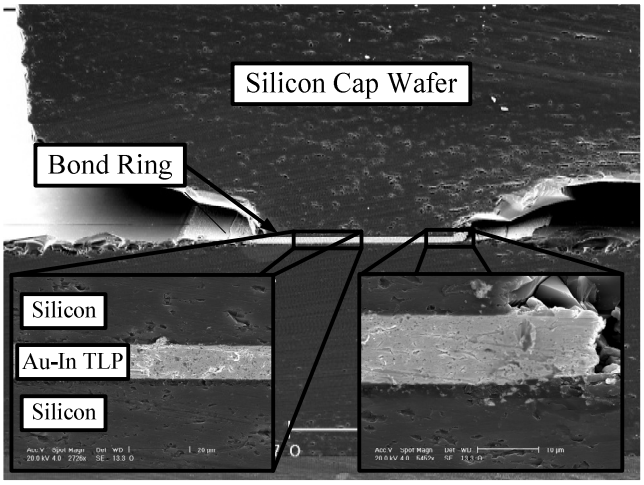

Figure 5: SEM of the bond cross section with magnified views of the bond ring.

The pressures inside the cavities were measured to determine a baseline, and have been periodically measured since. Figure 6 shows the long-term hermeticity data from the packages after bonding. The pressures inside the cavities ranged from 200 mTorr to 5 Torr and have remained stable for over 6 months without any obvious leaks. The wide range in pressures is likely due to differences in outgassing rates and getter pumping speed.

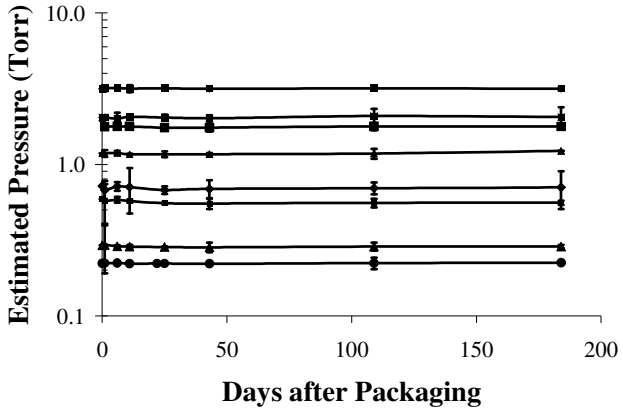

Figure 6: Long term cavity pressures measured by packaged Pirani gauges.

Looking closer at the long term pressure data of one package shows enough detail to estimate a leak rate (Fig. 7). There is no observable trend in the pressure data that indicates any leak in the package. However, the dotted line in the figure represents the worst case leak the fits within the error bars of pressure measurement by the Pirani gauges. The worst case pressure rise is 16 mTorr/year, which corresponds to a leak rate of $1 \cdot 10^{-16}$ atm.cc.s^{-1} for the package volume of 0.15 µL. This is the worst case leak rate based on the error in the pressure measurement; it is believed that the package is neither leaking nor the pressure actually going up. As more long term pressure measurement data is taken, the worst case leak rate will go down.

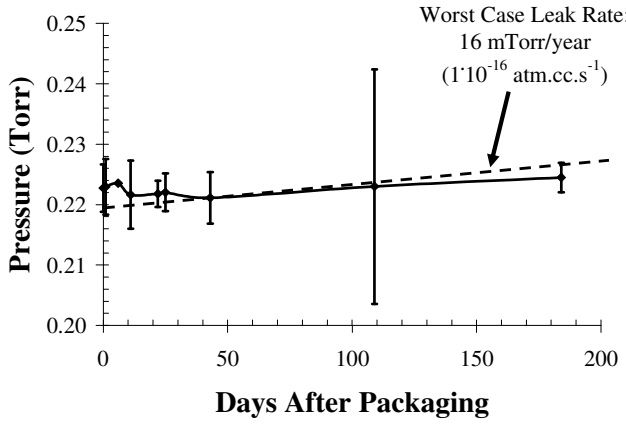

Figure 7: Zoomed in view of the pressure measurement of one of the die. The dotted line represents the worst case estimate pressure rise that fits within the error of the pressure measurement.

5. CONCLUSION

A gold indium TLP bonding technique was used to create low-temperature wafer-level MEMS vacuum packages. The bond is created in a commercially available wafer bonder with a maximum temperature of 200 °C and total process time of one hour. The package pressures varied from 200 mTorr to 5 Torr and have been stable for over 6 months. Despite no leak trend, a worst case pressure rise of 16 mTorr/year can be fit within the error of the Pirani gauge measurement data. This corresponds to a leak rate of $1 \cdot 10^{-16}$ atm.cc.s^{-1} for a volume of 0.15 µL.

This process does not take full advantage of the low-temperature nature of Au-In TLP bonding because the getters need to be activated at 400 °C. The maximum temperature of the process is dictated by this getter activation temperature, which can be reduced in several ways. One way would be to use getters with lower activation temperatures, such as TiVZr getters that can be activated at 300 °C. Another way would be to use localized heating to activate the getters, which would not heat the package at all. By combining one of these techniques with Au-In TLP bonding, a complete low temperature vacuum packaging technique is possible.

6. ACKNOWLEDGMENTS

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7. REFERENCES

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