Capacitive Accelerometer with High Aspect Ratio single crystalline Silicon Microstructure Using the SOI Structure with Polysilicon-Based Interconnect technique

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Abstract

We have developed a new processing technique for a capacitive mechanical sensor with a single crystalline silicon microstructure using the SOI structure which enables electrical isolation and interconnected wiring. This technique can make the sensor surface completely flat, allowing the formation of a cap for resin molding and a vacuum package for an angular rate sensor.

Introduction

In recent years, various types of sensors, such as capacitive accelerometers and angular rate sensors, based on surface micromachining technology have been reported. Of the piezo-resitive and capacitive type adapted in these accelerometers for detecting method, the capacitive is becoming mainstream due to its theoretical characteristics of high sensitivity and small temperature drift. However, since most surface micromachining-based capacitive sensors have a polycrystalline silicon film of only about 2 μ m thick in their structures, they are usually susceptible to cross-axis sensitivity and electrical noise, which poses an obstacle for performance improvement. So, to improve their performance, sensors need large sense capacitance and large mode separation. They are achieved by structures with high aspect-ratio and dielectric separation. Some processes which achieve these structure by using single crystalline silicon as its structure based on the SOI(Silicon on Insulator) substrate are suggested [1],[2]. The sensor needs to be capped during the mounting process so that it is resin-molded or, in the case of angular rate sensors, is packaged in a vacuum environment, and if possible the surface of the sensor substrate should be made flat as shown in Figure 1 and 2.

This paper discusses the SOI substrate structure, in

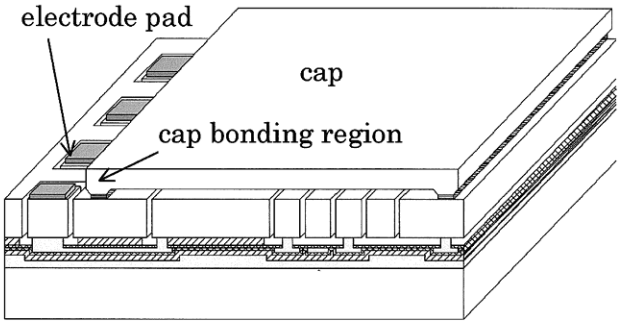

Fig 1. Sensor image with a cap viewed diagonally

which a cap for protecting the sensor surface at dicing

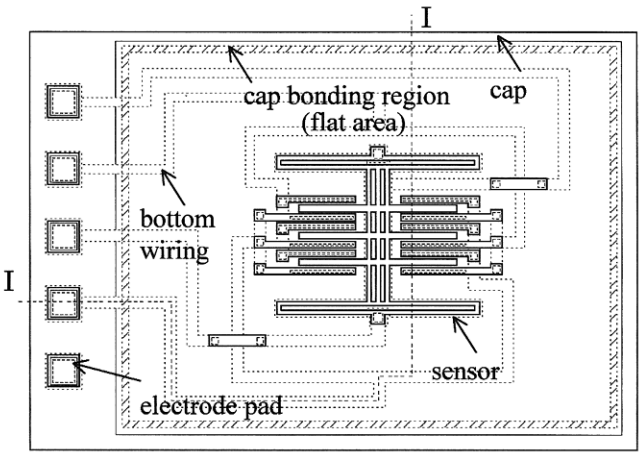

Fig 2. Accelerometer image with a cap viewed from above

or mounting can be created by embedding the polycrystalline silicon in the SOI substrate through the

interconnected wiring technique in which circuit wires do not appear on the surface. We have developed a prototype of this SOI-constructed substrate and examined its basic performance. A substrate with this structure can be freely modified in its thickness, and if the aspect ratio of dry etching, a ratio between the structure thickness and the electrode-to-electrode distance, can be made higher, the capacitive amount per unit area will increase, thereby minimizing the element size.

Process for embedding polysilicon-based interconnection in the SOI structure

As you see in Figure 2, two pairs of fixed electrodes are generally placed on both sides of a capacitive sensor to establish a comb-like structure, and this wiring arrangement is very effective for obtaining a large amount of capacity. Since these pairs of fixed electrodes are to be plugged into external units after having been connected respectively, their wires shall have the joints at which they cross over each other. However, forming a cross joint is difficult with standard SOI substrates. As a solution, we built wires made of polycrystalline silicon in the SOI substrate. The cross section shown in Figure 3 is the process flow of the prototype we made based on this theory. Its process flow is explained as follows.

1) Etch the single crystalline silicon substrate to form grooves using RIE(Reactive Ion Etching) and then fill with silicon dioxide, which is used as a sacrificial layer, by thermal oxidization and CVD. Note that both grooves and silicon dioxide are later used as guiding marks for mask alignment as well as a stopper for measuring the desired thickness when the substrate is polished with CMP (Chemical Mechanical Polish) after wafer direct bonding.
2) Using LP-CVD (Low Pressure Chemical Vapor Deposition), deposit a silicon nitride which acts as a stopper during sacrificial layer etching. After removing part of the silicon nitride and silicon dioxide by RIE, form a polycrystalline silicon thin film by LP-CVD and pattern it by RIE. This polycrystalline silicon film can be used as an electrode or inner wiring.
3) Repeat this operation to form silicon nitride and silicon dioxide films, and fabricate a polycrystalline silicon film with LP-CVD over these films. Polish them together with CMP until the surface becomes flat.
4) Then Contact another silicon substrate directly to the substrate that was flattened in Step 3. At this time, anneal this combined substrate at a temperature of 1,150℃ for approximately one hour.

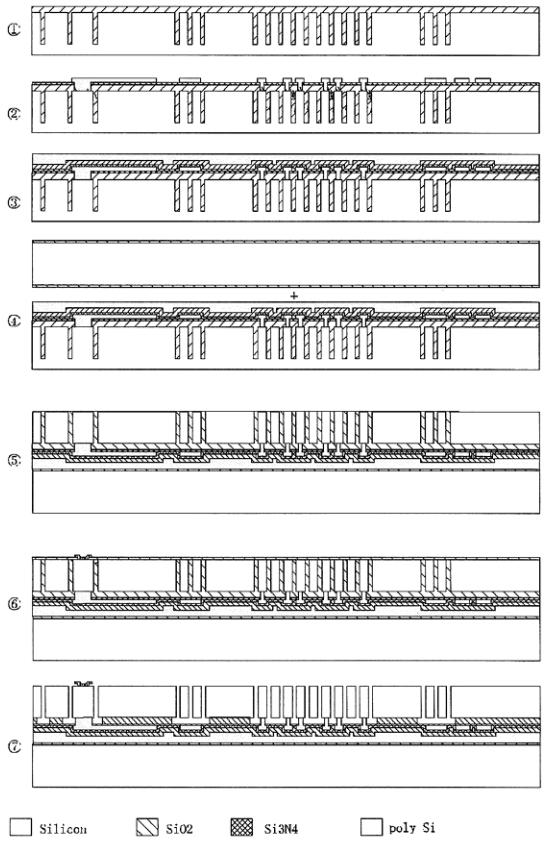

Figure 3. Process flow of the capacitive accelerometer embedding polysilicon-based interconnection in the SOI structure(Shown in cross section)

5) Polish the substrate until the desired structural thickness is achieved with CMP. The silicon dioxide embedded in the groove in Step 1 has a slower polish rate than silicon and this property is efficiently used as a stopper when etching.
6) Form an Al electrode which is used as a pad after fabricating silicon dioxide insulating layer.
7) Remove the sacrificial dioxide layer through HF etching to make the structure movable. In this process, no more caps were fixed on top of this structure.

Experimental Result

Unlike a simple direct wafer bonding in SOI, the wafer bonding technology presented here involves a more complicated structure in which each groove separating the structure is filled with silicon dioxide. In addition, bonding is realized in the structure composed of internally connected polycrystalline wires and the fixed electrodes (anchors), imposing some alternative method that can accept a difference in layers. This is particularly important for the SOI structure having polysilicon-based interconnection. For this purpose, we first flattened the substrate by leveling out the unevenness of the multi-layered polycrystalline silicon fabricated in Step 3 (see Figure 3) before bonding that substrate and another thermally oxidized substrate together.

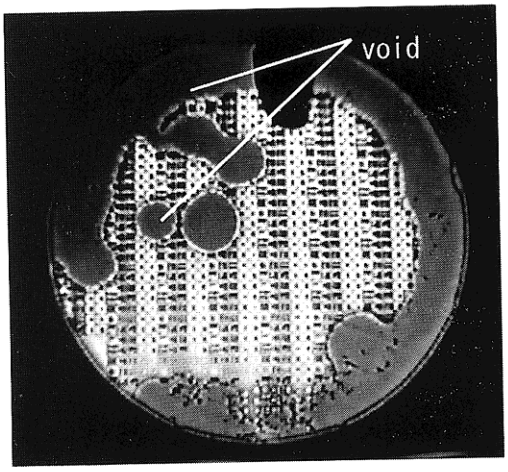

Figure 4. void after bonding and polishing (Magic mirror image)

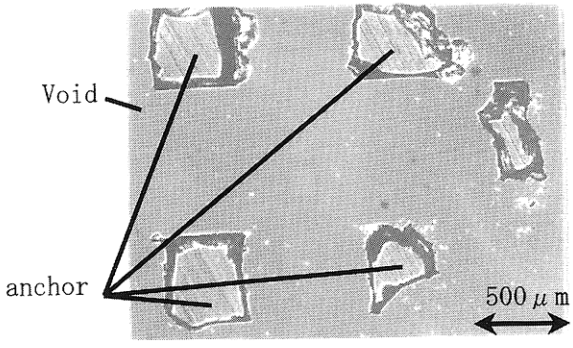

Figure 5. Enlarged photograph of void (Optical microscope image)

Our experiment detected a failure in the bonding as shown in Figure 4. Figure 5 is an enlarged photograph showing this defective bonding. As you see in this photograph, all areas other than the anchors are unbonded and removed by CMP polishing. Considering the process flows of bonding and polishing, it is assumed that the annealing process has caused a difference in layers between the anchors and the remaining areas. We compared the crystalline structure and the surface roughness of the anchors before and after annealing, the results of which are given in Figure 6. The photograph in Figure 6 is a cross-sectional TEM image representing the anchor's polycrystalline silicon, in which the polycrystalline silicon particles in the anchors have become larger after the anneal treatment. We believe that the silicon was

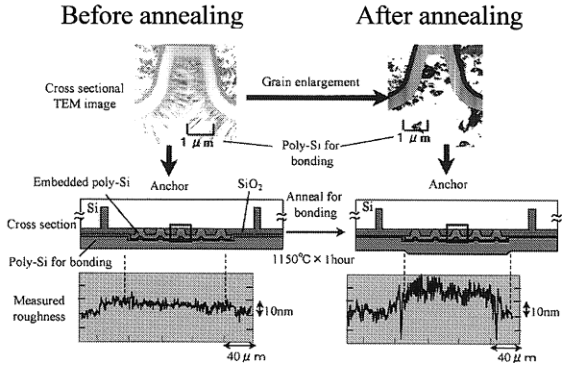

Figure 6. Changes in the polycrystalline silicon before and after annealing

mostly expanded vertically in volume or in the direction of the thickness, but not horizontally, because the expansion to sideways was blocked by the silicon dioxide. This manifestation is particularly obvious in the anchors compared with the remaining sections, and this inconsistency should be responsible for the unevenness of the polycrystalline silicon surface.

The solution we took for this problem was to pre-anneal the polycrystalline silicon substrate before it was passed to the bonding process. To eliminate a difference in layers, we annealed the polycrystalline silicon at a bonding temperature until its grain growth were saturated, and then flattened it by CMP. The time required for the grain growth saturation point was calculated, i.e., we measured the time until no differences were detected in the annealed silicon by both roughness measurement and a magic mirror observation (a test in which minor unevenness is made more apparent for observation). As a result, the difference was narrowed down to below the measurable resolution (5 nm) and unevenness was no longer observed by the magic mirror observation on the polycrystalline silicon if it had been annealed for more than 10 hours.

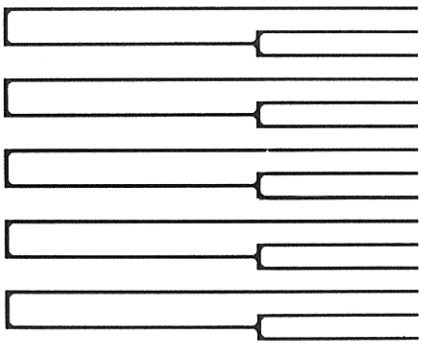

Figure 7: Cracks in the structure
(Optical microscope image)

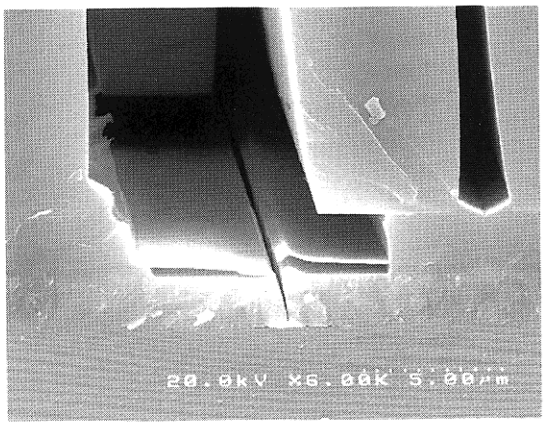

Figure 8. Cross-sectional SEM photograph showing cracks in the structure

Another problem was some chips found in the structure as shown in Figure 7. Figure 8 is the cross section of the structure with such a failure. A difference in the thermal expansion coefficient between the SiO2 filled in the partially formed grooves and the silicon used in the other areas could have induced stress when they were tied together at a high temperature, which in turn probably caused a crack in the structure. Having considered all these factors, we have changed the process flow so as to prevent such a stress from taking place at high temperatures at bonding. The altered process flow is illustrated in Figure 9. In this

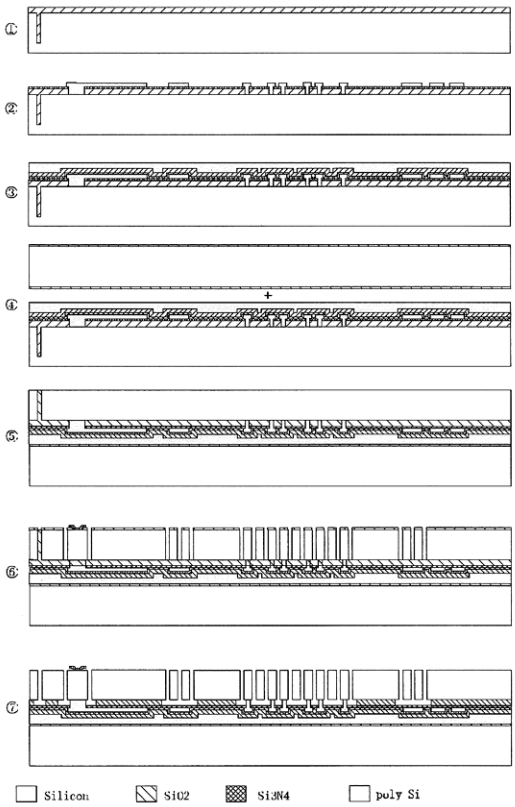

Figure 9. Improved process flow

new approach, filling the groove with silicon dioxide is eliminated and the generation of stress is prevented by forming the structure after the bonding.

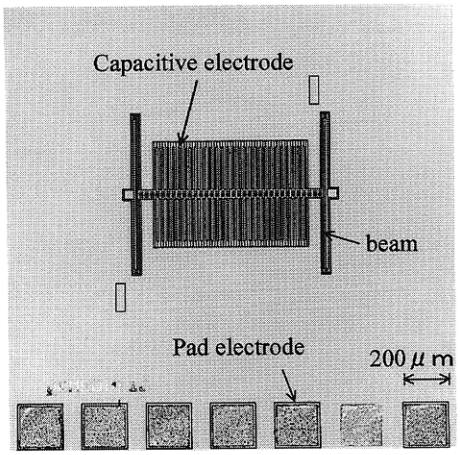

Figure 10. Photograph of sensor in plane view (Optical photomicrograph)

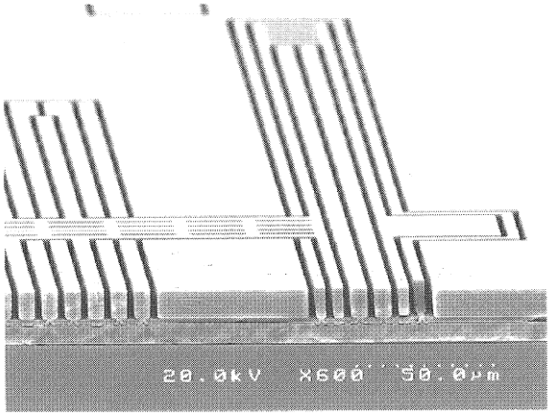

Figure 11. Cross-sectional SEM photograph of capacitive accelerometer with polysilicon based interconnection

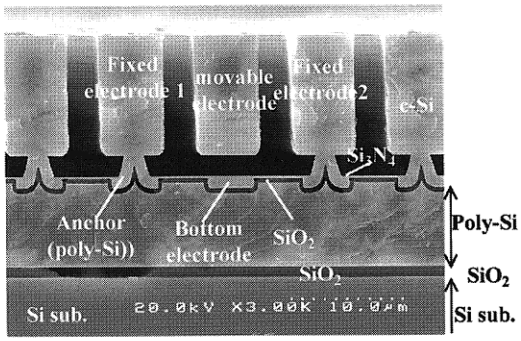

Figure 12. Enlarged SEM photograph showing the anchor

The microscopic picture in Figure 10 shows the surface of the capacitive accelerometer and the SEM photograph in Figure 11 shows its cross section. These two figures indicate that a wide, flat area is secured without causing unevenness between the sensor and the pad electrode, thus allowing the joint section to be reserved for the cap as illustrated in Figures 1 and 2.

In addition, as you can see in Figure 12, the anchor base for the structure is established by the embedded polycrystalline silicon and is firmly fixed to the substrate even after the sacrificial layer etching.

Acceleration Output Characteristics

We evaluated the capacitive accelerometer assembled by the above-mentioned process by applying acceleration using a vibrating exciter and examined its output against the acceleration ratio. Shown in Figure 13 is a block diagram of the circuit we used in our test. We applied a negative-phase pulse to each of the two pairs of fixed electrodes and conducted demodulator with a commercially available IC (AD630) on their C-V converted outputs generated from the movable electrodes. After that, we removed noise using LPF(Low Pass Filter) to take out the output. No servo control was performed in this procedure. Figure 14

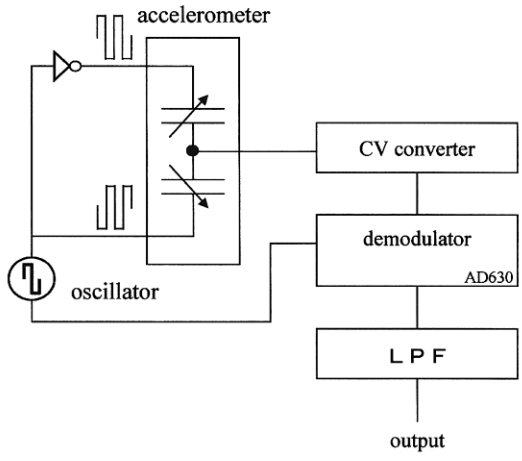

Figure 13. Block diagram of the circuit examined

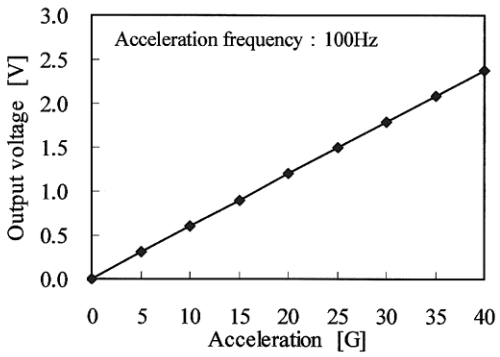

Figure 14. Acceleration output characteristics

describes the graphical characteristics of the output voltage when acceleration is increasingly applied to it. As you see from this figure, a good linearity is obtained between output and acceleration.

Conclusions

We prototyped and evaluated an SOI-structured capacitive accelerometer having interconnected polycrystalline silicon wiring. With our strategy, a complete area can be bonded when the SOI is formed by effectively handling a difference in layers which is accompanied in the built-in interconnected wiring structure. This was realized by annealing the polycrystalline silicon used for smoothing the surface in advance in order to prevent the silicon's expansion which is widely associated to bonding. We evaluated the acceleration property of the capacitive accelerometer prototyped in this approach and confirmed a liner characteristic.

References

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