A 1 mG LATERAL CMOS-MEMS ACCELEROMETER

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ABSTRACT

This paper reports a lateral CMOS-MEMS accelerometer with a measured noise floor of 1mG/$\sqrt{\text{Hz}}$ and a dynamic range larger than 13G. The accelerometer is fully compatible with conventional CMOS processes enabling the integration of most of the conditioning circuits. It is fabricated in a three metal layer 0.5μm CMOS process followed by a two-step dry etch release. An improved curl matching technique is utilized to solve the out-of-plane curl problem. A new differential amplifier is used for the capacitive sensing interface. The CMOS micromaching process used in this project is described. The design of accelerometer, system schematic applying force-balance feedback and experimental test results are presented.

INTRODUCTION

Microstructures based on CMOS processes were first reported ten years ago [1] and are currently being researched by several groups [2][3][4]. A high-aspect-ratio CMOS micromaching process [5][6] developed at Carnegie Mellon University has advantages of 100% compatibility with conventional CMOS IC processes and multi-layer wiring [5][6]. Using this process, one can make a fully differential CMOS accelerometer. The fully integrated sensors and circuits suffer less parasitic capacitance and electrical noise. This process enables relatively high sensitivity and wide freedom in design.

However, the multi-layer microstructures in CMOS-MEMS experience serious curling during release. Out-of-plane curling may significantly decrease lateral sensing capacitance. Special consideration of curling control is required for proper function.

The first lateral CMOS accelerometer was reported in [7]. And the polysilicon counterpart with force-balance feedback topology was presented in [9]. Challenges in this project include improving curl matching, designing a new sensing interface circuit for less parasitic capacitance, obtaining the closed loop signal, and increasing dynamic range by using the force-balance feedback topology.

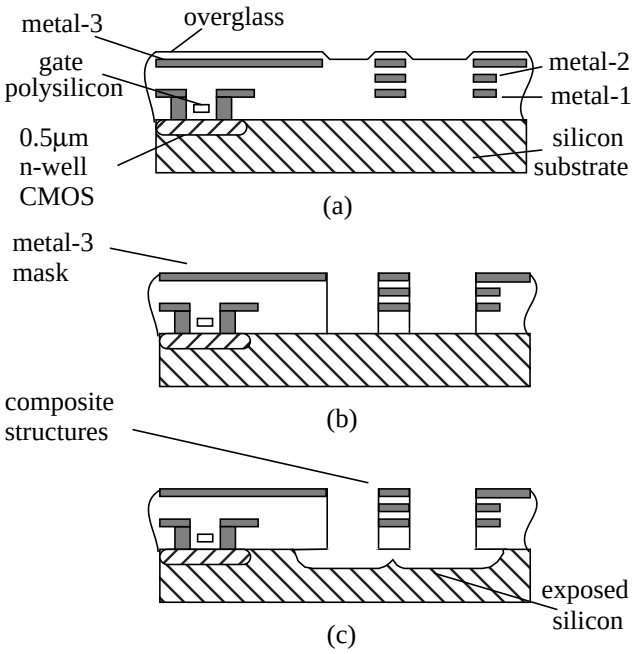

Figure 1: CMOS-MEMS process. (a) CMOS chip after fabrication (b) anisotropic RIE removes dielectric (c) isotropic RIE undercuts silicon substrate

CMOS MICROMACHING PROCESS

The accelerometer described in this paper uses high-aspect-ratio CMOS micromaching technology [5][6]. It is fabricated in a three metal 0.5μm n-well CMOS process. After the foundry fabrication, two dry etch steps, shown in Figure 1, are used to define and release the structure. Figure 1(a) shows the cross section of the chip after regular CMOS fabrication. In the first step of post processing (Figure 1(b)), dielectric layers are removed by an anisotropic CHF_3/O_2 reactive ion etch (RIE) with the top metal layer acting as an etch resistant mask. After the sidewall of the microstructure is precisely defined, an isotropic SF_6/O_2 RIE is performed to etch away the bulk silicon and release the structure (Figure 1(c)). Multi-layer conductors can be built in the composite structure, which enables more flexible designs than homogeneous conducting structures.

The undercut of silicon in the release step (Figure 1(c)) constrains the placement of sensing circuits to at least 40μm away from the microstructures. Compared to commercial polysilicon micromaching technology, the CMOS-MEMS

clearance is smaller and suffers less parasitic capacitance. Such parasitics are to be avoided when using capacitive sensing techniques.

ACCELEROMETER STRUCTURE DESIGN

The schematic view of the accelerometer is shown in Figure 2. It is a fully differential common-centroid accelerometer using the topology described in [7].

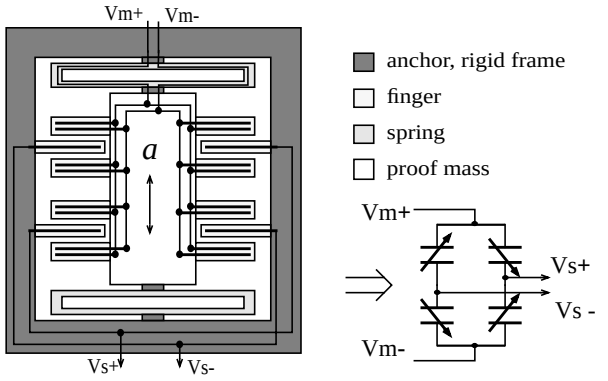

Figure 2: Schematic of accelerometer.

Sensing nodes are located at stators instead of rotors to minimize parasitic capacitance. Differential modulation signals are routed through the serpentine spring by the two metal layers under the top metal layer, which is grounded and acts as the RIE mask. Compared to a half bridge sensing interface, the differential topology has higher input common-mode rejection ratio (ICMMR) and larger dynamic range.

In the layout, each half-capacitive bridge is split into two parts and located at two cross-axis corners. This common-centroid layout topology cancels common-mode input noise such as substrate coupling, power supply coupling and cross-axis vibration.

The laminated structure experiences a larger vertical stress gradients than its polysilicon counterpart. Vertical residual

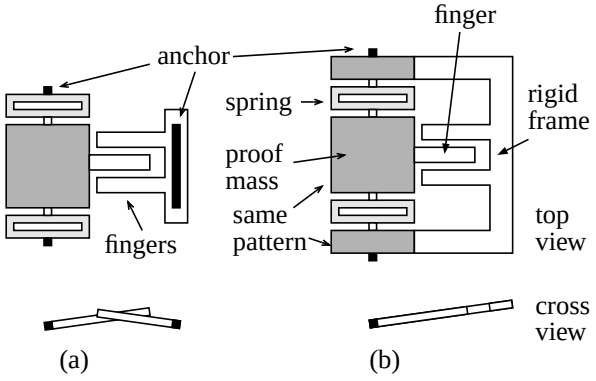

Figure 3: Local curl matching technique (a) Without curl matching. (b) With curl matching

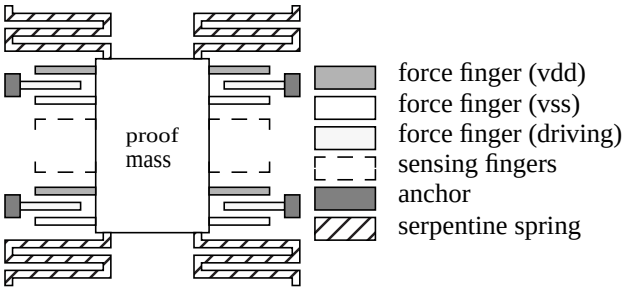

Figure 4: Feedback actuator

stress gradients in the CMOS structures can result in a radius of curvature of 1mm~5mm [8]. Out-of-plane curling can significantly reduce the sidewall capacitance which is critical to capacitive sensing. To solve this problem, fingers on the stator side are attached to a rigid frame (Figure 3) instead of to the substrate. The rigid frame is anchored along a common axis with the proof mass, and is subjected to the same stress gradient as the inner structure. Thus a first order curl matching can be achieved. To get optimal matching, a local matching technique has been developed. The middle part of the rigid frame has the same density of holes in its structure as the proof mass. The outer part of the rigid frame is composed of beams which are similar to the fingers. This design eliminates the pattern sensitive mismatch between the inner and outer structures.

The force-balance technique counters any impeding deflection due to acceleration and servos the device back to its null position using the electrical feedback force generated by the actuator [9]. To avoid cross-axis actuation, the actuator is partitioned into four parts and symmetrically located at each corner of the accelerometer (Figure 4). Differential force fingers are biased with the highest voltage in the system (power supply voltages, v_{dd} & v_{ss}) and are routed by two metal layers through the serpentine spring.

The accelerometer was simulated in Cadence SPECTRE™ using NODAS [10]. The simulation schematic is given in Figure 5. Some key parameters and simulation results are given in Table 1:

Table 1. Parameters of the accelerometer

device size	400 μm × 540 μm
comb finger length	54 μm
finger gap	1.5 μm
serpentine spring	2 turns, 2.1μm× 123 μm
sensing capacitance	16 fF × 4
spring constant	2.04 N/m
resonant frequency	6.1 kHz
sensor sensitivity	0.6 mV/G

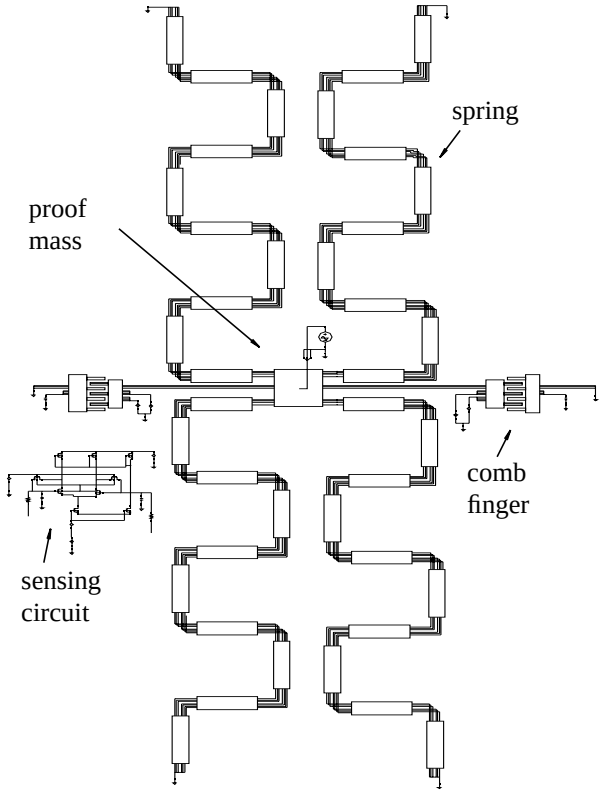

Figure 5: Sensor simulation schematic

CIRCUIT DESIGN

On-chip fully-differential sensing pre-amplifier and main amplifier (Figure 6) are used to detect the capacitance change due to deflection of comb fingers. The biasing problem of the capacitive sensing interface is solved by using two small transistors (W/L=2.4μm/2.1μm) working in the subthreshold range. These two transistors exhibit large resistance and no source to drain capacitance. This technique eliminates the requirement of large resistors which are not feasible in the CMOS process.

The integrated main amplifier is a differential amplifier with gain of 32dB and also acts as an output buffer. To avoid the damage caused by undercut of silicon in the RIE (see Figure 1 (c)), circuits are put 40μm away from the sensor. Except for the microstructure, the whole chip area is covered by the top metal layer.

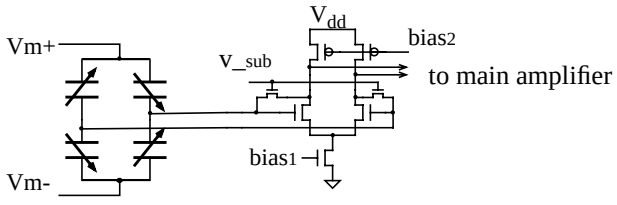

Figure 6: Capacitive sensing interface

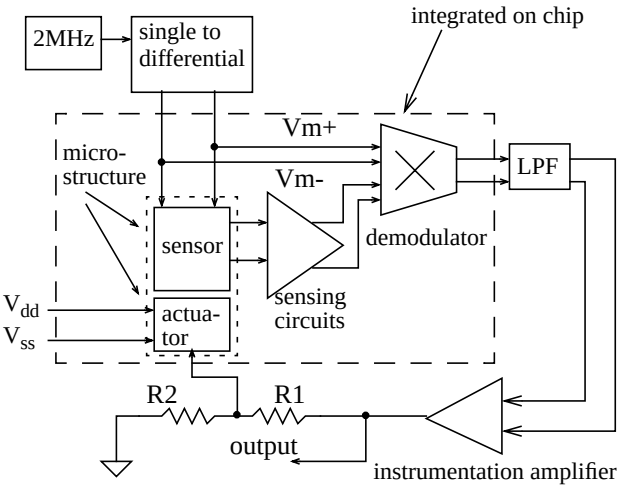

Figure 7: Schematic of force balance feedback loop.

A force-balance topology greatly increases the accelerometer dynamic range. Figure 7 shows a block diagram of the complete feedback loop. The output from the sensing finger is amplified and applied to a synchronous demodulator. The low-pass filter (LPF) eliminates the carrier and boosts loop phase margin. The output of the off-chip instrumentation amplifier is fed back to the actuator to keep the device in the null position.

EXPERIMENTS

The device was fabricated in the Hewlett-Packard three-metal 0.5μm n-well CMOS process. Figure 8 shows the SEM of the released CMOS-MEMS accelerometer. A side view with details at one corner of the accelerometer is shown in Figure 9.

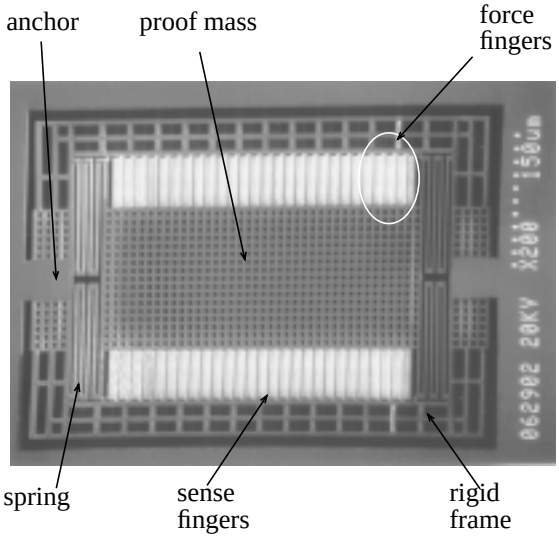

Figure 8: SEM of a released accelerometer.

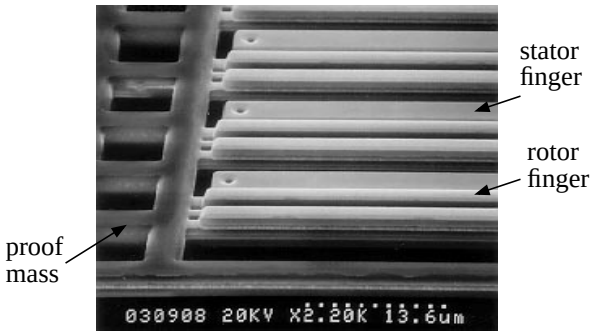

Figure 9: SEM of the side view with an angle of 45˚ at one corner of the accelerometer.

By using the local-matching technique, curling matching was improved by 50% over the first generation design [7]. The stator fingers are 1.2μm lower than the rotor fingers.

A test PCB (3 cm × 5 cm) including a differential modulation clock (2 MHz) generator and the complete force-balance feedback loop has been made. The measurement setup consists of a Brüel & Kjær 4808 vibration exciter, a HP 4395A spectrum analyzer, and a LeCroy 9354L digital oscilloscope. The accelerometer is shielded by a metal box to cancel external radio interference (Figure 10).

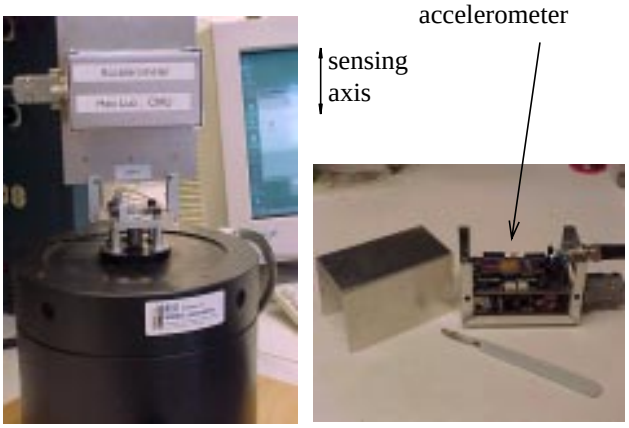

Figure 10: Test setup and accelerometer

Figure 11 shows the waveform of the accelerometer when excited by 50 Hz 14G(p-p) sinusoidal acceleration. Trace 1 is the output from the reference accelerometer on the vibration table. Trace 2 is the output from the CMOS-MEMS accelerometer under test.

Figure 12 shows the spectrum of the output from the accelerometer when excited by 100mG acceleration at 200Hz. As can be seen, the noise floor is 1mG/ $\sqrt{\text{Hz}}$. The system noise is Brownian noise and circuits noise combined with the test environment noise.

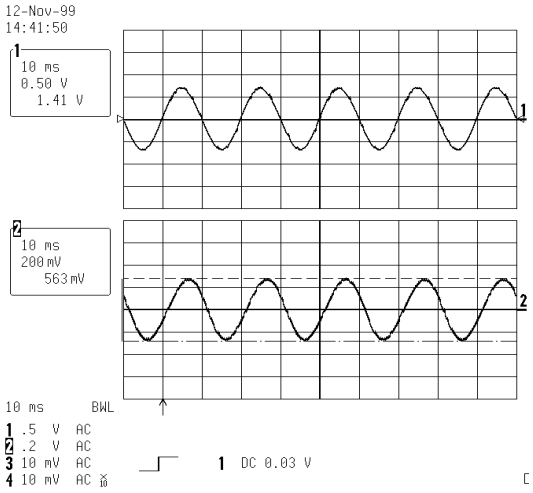

Figure 11: Waveform of accelerometer output

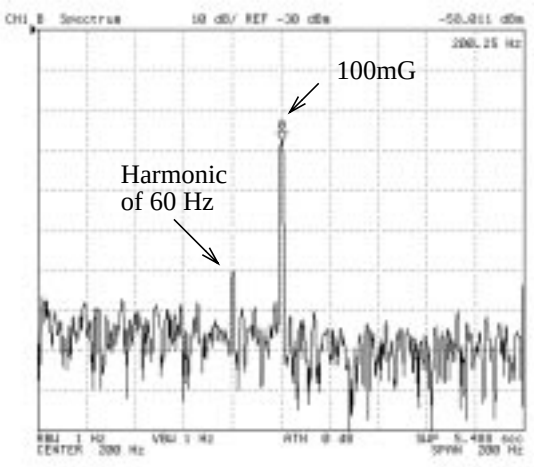

Figure 12: Spectrum of the output

The AC response of this system was obtained by applying 2G(p-p) sinusoidal acceleration from 20Hz to 860Hz. As shown in Figure 13, the frequency response is relatively flat at low frequency (lower than 300Hz), and it varies greatly at frequencies higher than 300Hz. The severe change is caused by multiple vibration modes of the test PCB and the mechanical supporting structure. This system is suitable for applications working lower than 300 Hz.

Dynamic linearity characteristics of the accelerometer is measured by applying sinusoidal acceleration at 200 Hz (Figure 14). The measured dynamic range of this accelerometer (±13G) is limited by the maximum output acceleration of the test equipment. Even when the accelerometer experiences a large shock acceleration (> 30G) during the crash test, saturation has not been observed.

Table 2 summarizes the design specifications given by NODAS simulation, MATLAB loop simulation and the test

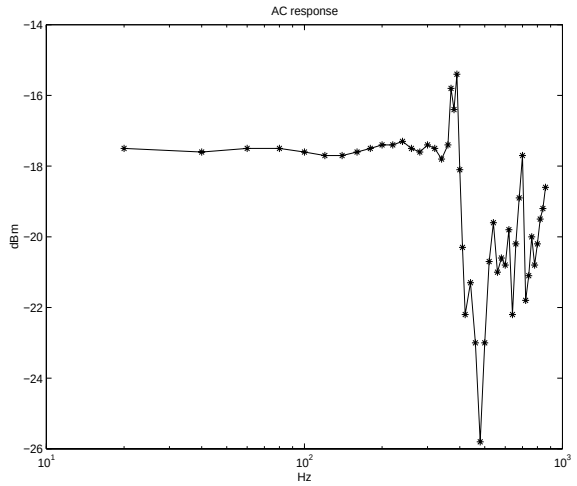

Figure 13: Accelerometer AC response

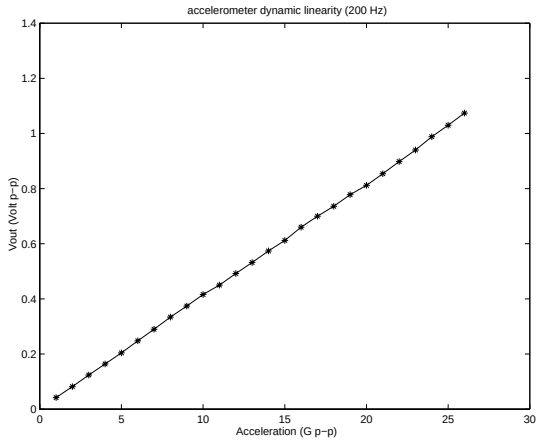

Figure 14: Dynamic linearity at 200 Hz.

results. As can be seen, the resonant frequency matches the simulation to within 5%. The measured noise floor (1mG/ $\sqrt{\text{Hz}}$) is larger than the composite of Brownian noise (28μG/ $\sqrt{\text{Hz}}$) and circuit noise (0.3mG/ $\sqrt{\text{Hz}}$). Significant noise comes from the testbed ambient. The sensitivity loss of 17% was caused by the capacitance loss due to beam curling.

CONCLUSION

We have reported a fully functional differential CMOS accelerometer and a complete force-balance feedback test system. The fabricated accelerometer shows 1mG/ $\sqrt{\text{Hz}}$ noise and 13G linear range. The finger mismatch and relatively large circuit noise require further research on device structure and circuit topology.

Table 2. Design specs and test result

	Designed	Tested
Resonant frequency	5.9 kHz	6.1 kHz
Noise	28μG/ $\sqrt{\text{Hz}}$ (Brownian only)	1mG/ $\sqrt{\text{Hz}}$ (total)
Sensor sensitivity	0.6 mV/G	0.5 mV/G
Closed loop sensitivity	22 mV/G	41 mV/G
Dynamic range	$\pm$ 5G	> $\pm$ 13G
Cross axis sensitivity	--------	-40 dB

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