A MONOLITHIC FULLY-INTEGRATED VACUUM-SEALED CMOS PRESSURE SENSOR

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Abstract: **This paper presents an integrated multi-transducer capacitive barometric pressure sensor that is vacuum-sealed at wafer level. The interface circuitry is integrated directly within the sealed reference cavity, making the device immune to parasitic environmental effects. The overall device process merges BiCMOS circuitry with a dissolved-wafer transducer process, is compatible with bulk- and surface-micromachining, and employs chemical-mechanical polishing (CMP), anodic bonding, and hermetic lead transfers. The sensor achieves 15b resolution and is suitable for low-cost packaging. The device is composed of a programmable switched-capacitor readout circuit, five segmented-range pressure transducers, and a reference capacitor, all integrated on a 7.5x6.5mm^2 die using 3µm features.**

INTRODUCTION

The development of integrated sensors containing on-chip interface circuitry has become a primary focus in MEMS in order to achieve improved performance, reduced cost, and realization of the system-on-chip concept. Such sensors reduce the effects of parasitics and external interference because the signal is amplified in close proximity to the transducer; however, they also pose interesting challenges in merging transducer and circuit processes, maintaining testability, and achieving reliable vacuum encapsulation. Vacuum encapsulation is required in many devices to eliminate problems relating to temperature-induced gas expansion, squeeze film damping, and stiction during final release of the device. In addition the availability of an assembly-ready device can significantly reduce packaging costs associated with hermetic sealing and permit injection-molded plastic packaging to be used. The die area required for a sensor having embedded readout circuitry is typically smaller than for two separate dies as used in hybrid integration, and any reliability problems associated with inter-chip interconnects are eliminated.

Any yield model for integrated sensors containing on-chip circuitry is highly process dependent. In the past decade, process equipment has become highly automated, providing improved control to support processes having high numbers of masking steps. The impact of this improved process control is seen in the success of deep-submicron process technology, which has many more masking steps than standard 1µm CMOS and yet achieves high yield. Thus, the prospect of fabricating sensors using higher mask counts to achieve high performance while still maintaining high yield is promising and has resulted in growing interest from many large-volume sensor manufacturers [1-3].

STRUCTURAL DESIGN

The integrated barometric pressure sensor reported in this paper is a significant extension of earlier work on multi-segment transducers [4] and readout circuitry [5] and complements other previous work in this general area [6-8]. It was developed for use in precision altitude measurements and microweatherstations. The device structure is shown in Fig. 1 and is formed by anodically-bonding a <100> silicon wafer to a 7740 glass substrate after the fabrication of the CMOS circuitry. The glass is thermally matched to silicon, reducing structural stresses. The transducers and circuits are located in recessed cavities in the silicon. By recessing the circuitry, the bonding anchors form the highest topological features on the silicon wafer. This allows the use of CMP at a later stage in the process to obtain a surface roughness of

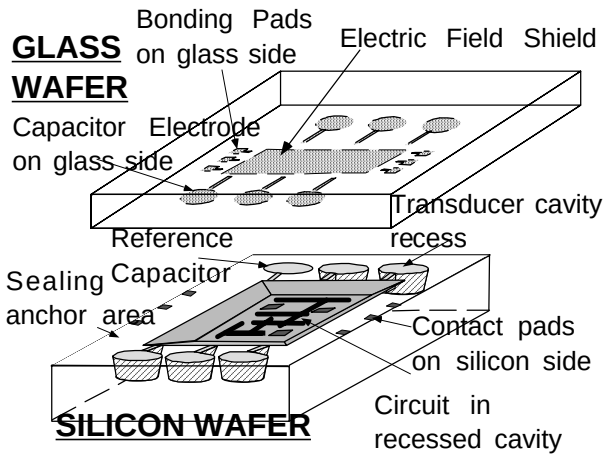

Fig. 1: Exploded three-dimensional diagram of the capacitive barometric pressure sensor.

<50nm on the bonding polysilicon. This is crucial for a high-yield vacuum seal. Electrical signals are transferred from the sealed cavity to the outside world using dielectric isolated doped polysilicon leads. A selective backside anisotropic etch in EDP is performed to release the pressure transducers. Bonding pads are located on the glass to allow the die to be directly mounted on a PCB or MCM module. Semiconductor sensing devices cannot always be placed in standard packages and most package designs have some effect on sensor performance due to externally-induced stresses and trapped-gas effects. This is especially true when the transducer measures an ambient physical quantity (such as pressure or humidity) that requires one side of the die to be directly exposed to the ambient. In this device, software programmability is provided to overcome any environmentally-induced shifts in the system behavior. Partial dicing of the glass wafer before anodic bonding simplifies die separation prior to packaging.

SYSTEM ARCHITECTURE

While the system reported here was specifically designed for a capacitive pressure sensor, sufficient flexibility was included to permit its use with other micromachined capacitive sensors as well (e.g., such as accelerometers). This required the use of a modular process compatible with bulk- and/or surface-micromachined devices on the same wafer. The complete device cross-section is shown in Fig 2. The on-chip readout circuitry can interface with five different transducers and employs programmable offset and gain adjustments, a buffered DC analog output, an on-chip sampling clock generator, and a serial microcontroller bus interface. There are three I/O, one control, one CLK and two power lines. Vin+ and Vin- (Fig. 3) are typically referenced to Vdd but can be referenced to other voltage levels if required. The prototype chip has additional access pins provided for debugging and also allows use of an optional external

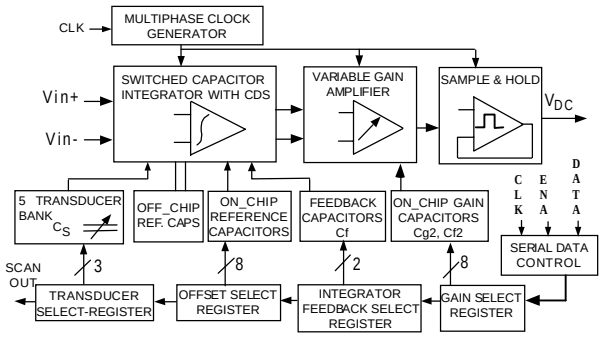

Fig. 3: Block-level schematic of the integrated readout circuitry for the sensor

reference capacitor.

Device parasitics, which may be introduced in the wafer bonding/sealing step, are a particular issue in the case of on-chip CMOS circuitry; because of these parasitics, it is not possible to perform final trims on the system prior to vacuum sealing. However, after vacuum encapsulation, laser trimming is no longer an option because the circuit is no longer accessible optically. Thus, electronic trimming is required in such devices. To enable these adjustments, analog offset/gain blocks, RAM registers, switches, and capacitor/resistor arrays are included on-chip. In addition, the circuitry needs to have control functionality to switch between calibration mode and operational mode. Provision for wafer probe level testing is made to avoid packaging of non-functional dies.

TRANSDUCER DESIGN

The sensor array consists of five different transducers, which cover the 300Torr dynamic range of the device. One of the transducers covers the entire range at lower sensitivity while the remaining four cover segments of the range at higher sensitivity [4]. Range differentiation is achieved by varying the diaphragm diameters from 1000µm to 1100µm for the various transducers. In

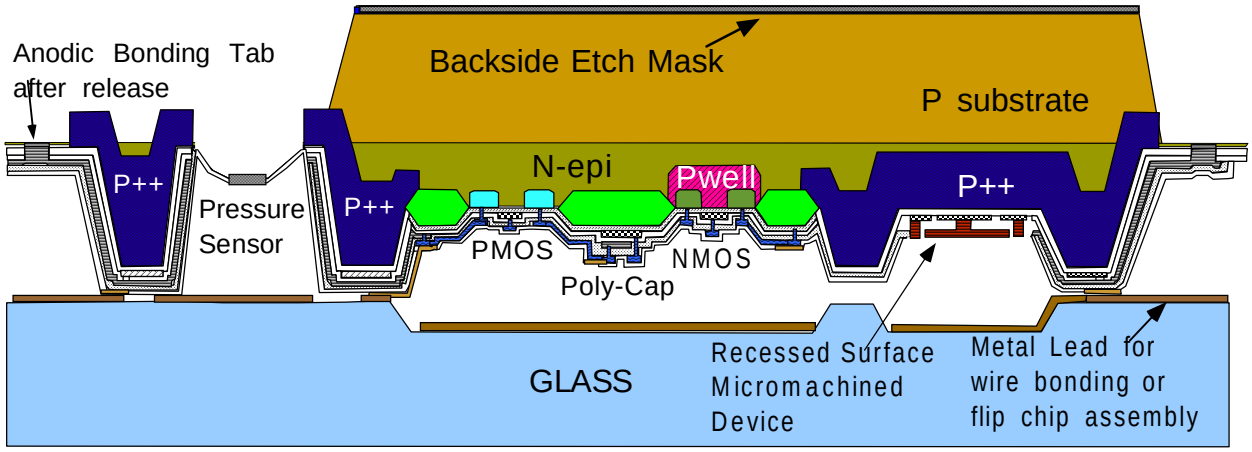

Fig. 2: Cross-section of the overall sensor, showing the transducer and its associated readout circuitry. A surface-micromachined vacuum encapsulated ring-gyro is shown in an adjacent cavity to illustrate the modular process.

operation, the global transducer is first read out to determine the approximate applied pressure, and the appropriate segment transducer is then used at higher sensitivity to determine that pressure with higher resolution. A reference capacitor is included for use with the differential switched-capacitor readout circuit.

The transducers consist of 4µm-thick (3.7/0.3µm Si/SiO_2) membranes with a rigid bossed center. The transducers are formed in 10.2µm-deep cavities recessed in the silicon. After the vacuum sealing and release in EDP, the bosses deflect about 9.8µm due to atmospheric pressure, operating with a gap of about 0.5µm. The resultant capacitance is in the 8-10pF range. The rigid boss does a first order linearization of the sensor capacitance change. A metal (Ti/TiN/Al) electrode on the moving diaphragm forms one plate of the capacitor and another metal electrode (Ti/Pt/Au) on the glass substrate forms the other plate. The diaphragm design is done using the ANSYS finite-element analysis tool. The center deflection y for a circular diaphragm with a rigid center boss (without residual stress) can be obtained to a first order as [9]

$$P = \frac{Et^3}{A_p a^4} y + \frac{B_p Eh}{a^4} y^3$$

Here, P is pressure, E is the Young's modulus, t is the diaphragm thickness, a is diaphragm radius and y is the center deflection. A_p and B_p are diaphragm/boss diameter and Poisson's ratio dependent constants, which for a representative case (Fig. 4) evaluate to 0.1135 and 12.4059, respectively. For heavily boron-doped membranes compensated by a thin layer of oxide, a residual stress of about 25–30MPa is present in the diaphragm, resulting in a proportionate decrease in deflection. Fig. 4 shows the center deflection predicted using FEA with all the stress factors present for this diaphragm.

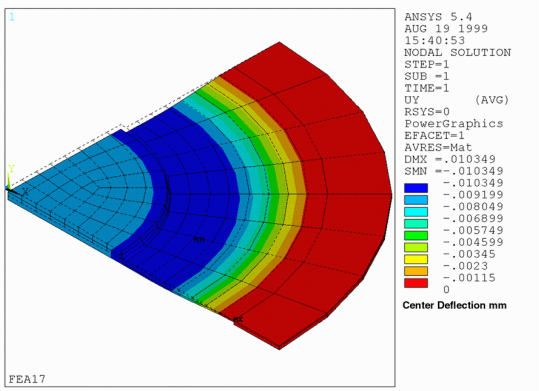

Fig. 4: Finite-element analysis results for a quarter of one diaphragm (2r=1040µm, boss_r=280µm), showing 10.3µm center deflection for an applied pressure of 101kPa.

CIRCUIT DESIGN

The chip contains a three-stage programmable switched-capacitor (SC) circuit (Fig. 5) that can multiplex up to five sensor elements at its input. SC circuit operation depends on the ratio of capacitances, allowing for greater process tolerance. The circuit gain can be adjusted by external programming. The programming data is input via a simple serial data interface. Programmable capacitor arrays are used for calibrating gain (0.1-1.25mV/fF) and offset over a wide range of transducer base capacitances (1 to 30pF) and sensitivities. The analog front-end consists of a fully-differential charge integrator with a self-biased folded-cascode amplifier, which uses continuous-time current-summing common-mode feedback for DC stabilization. The clocking scheme uses correlated double sampling to suppress 1/f noise and amplifier offset effects. The output of the first stage feeds a differential gain stage with single-ended output conversion. The charge transfer of the first integrator stage (Fig. 5) can be represented in discrete time by the difference equation

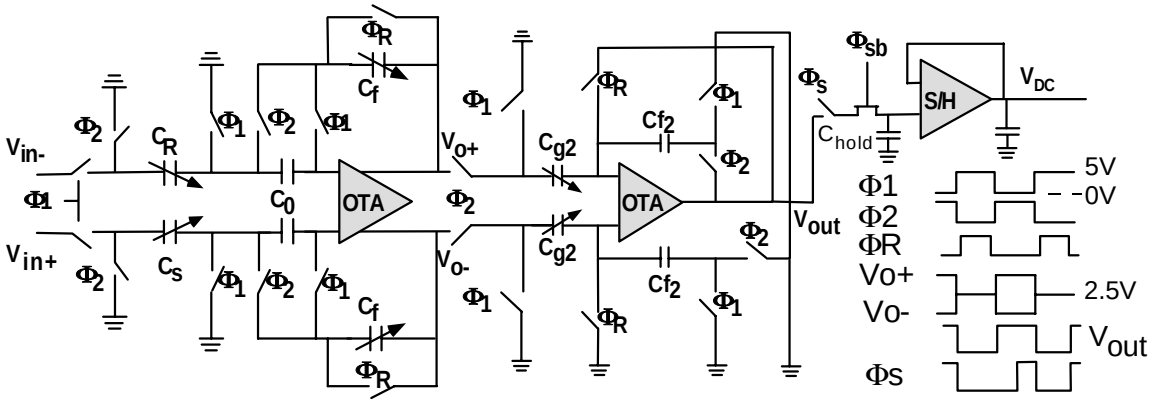

Fig. 5: Three stage switched capacitor readout circuit with fully-differential front-end.

$$C_f V_{o+}(n)T - C_f V_{o-}(n)T =$$
$$\{C_f V_{o+}[(n-1)T] + C_S V_{in+}[(n-\tfrac{1}{2})T]$$
$$-[C_f V_{o-}[(n-1)T] + C_R V_{in-}[(n-\tfrac{1}{2})T]\}$$

Using this, the overall capacitance to voltage conversion is given as

$$V_{DC} = \frac{C_{g2}}{C_{f2}}\left(\frac{C_S}{C_f}V_{in+} - \frac{C_R}{C_f}V_{in-}\right) + 2.5$$

The layout was done in the Michigan in-house 3µm BiCMOS p-well process, resulting in an overall die size for the sensor of 6.5 x 7.5 mm^2.

The additional thermal processing steps and application of the electric bonding field during post-processing requires the circuit to be tolerant to transistor parameter variations and process-dependent parasitics. In the case of vacuum-sealed devices, there is a parasitic resistance (20-50Ω) and capacitance (1-2pF) associated with the signal-transfer leads from inside the sealed cavity to the outside world. These parasitic elements can change as much as 20% due to process variations. For digital signals, the output buffers must be large enough to maintain output rise/fall times within required specifications. For analog signals, buffering using source followers is advisable. OTAs with a second output stage should be used to drive the output signals. One source of parasitic capacitance is that between the lead transfers and rest of the silicon bulk. The other major source is between the metal electrode on silicon and the silicon bulk with an O/N/O-poly-O/N/O stack acting as an intermediate dielectric. This manifests itself as a fixed capacitor in parallel with the internal sense and reference capacitors with a value of 1-1.5pF. In the physical layout, the silicon side should be connected to the input of the front-end charge integrator to avoid charge sharing with this parasitic capacitance. In general, there can exist many parasitic capacitances in monolithic devices, which must be extracted using customized LVS files and whose effect on circuit functionality must be carefully analyzed using back-annotated simulations.

PROCESS DESCRIPTION

The process uses 20 masks: 15 for the 2P/2M p-well circuitry, three additional masks for the transducers, and two for the glass processing. The process first etches recesses in a <100> p-type silicon wafer, subsequently growing a thick n-type epi layer in which the circuitry will be formed. The transducers are formed in recessed cavities 8µm deep, while the circuitry is fabricated in separate 2.5µm-deep cavities (Fig. 2). Thus, the anchors used for anodic bonding form the highest topological features on the silicon wafers. Figure 6 shows the silicon die before anodic bonding. The bonding anchor areas

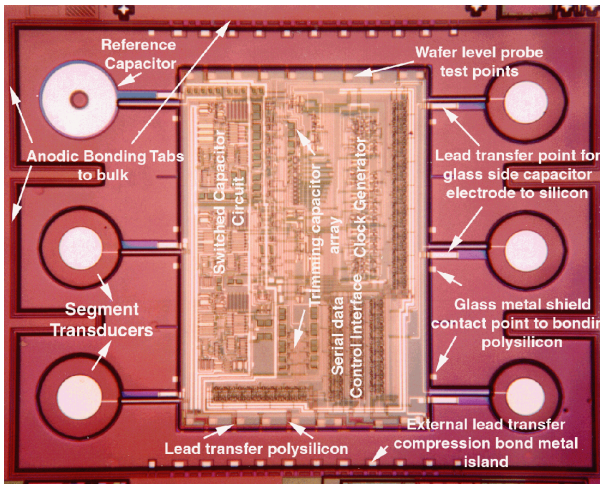

Fig. 6: Top view of the silicon die, showing the circuitry (center) with electrodes for five transducers and a reference capacitor.

also contain polysilicon lead transfers (Fig. 7) from the vacuum-sealed cavity to the outside world. The second-level polysilicon is 2µm thick; colloidal-silica-based CMP [9] is used to remove any surface imperfections and allow vacuum sealing. Ti/Pt/Au metallization is used on the glass to getter outdiffusing oxygen from the glass, and TiN is used in the circuit contacts to prevent junction spiking during anodic bonding. Back-side masking with corner compensation [10] is used over the circuit area while the remaining portions of the wafer are selectively etched to realize the final device.

The transducers are formed using two diffused-boron etch-stops: one for the rims/bosses and one for the diaphragms. Metal islands on both wafers provide compression-bonded low-resistance contacts to bring the leads out to pads on the upper glass surface. The process gives careful consideration to step coverage in the recessed areas and to the CMOS thermal budget,

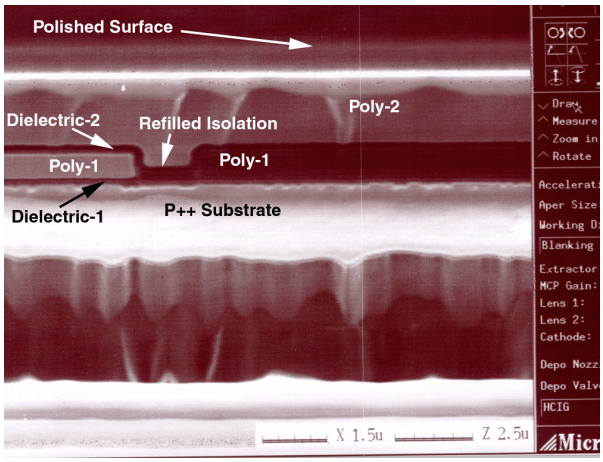

Fig. 7: Focused ion-beam cross-section of an isolation refilled polysilicon lead transfer.

achieving high yield. With three additional masks, the process can also be used to form vacuum-encapsulated surface micromachined devices on the same die. The second-level polysilicon is then common to the circuitry (poly-poly capacitors), the lead transfers, and the surface-micromachined devices. The surface micromachined devices are released in HF or BHF just prior to the anodic bonding step. Resonators, gyros, and accelerometers have been successfully fabricated on test dies included on the pressure sensor mask set.

One of the important considerations during design was the protection of the active devices from any damage due to anodic bonding. A special metal mask is included on the glass to block the electric field from the circuit area. This is accomplished by providing metal-2 contacts on the bonding polysilicon, which are in contact with the glass metal mask during bonding. The location of the tabs on the silicon side can be seen in Figs. 2 and 6. The connection requirement on the signal lines during fabrication is summarized in Table 1.

	Fabrication/ Test sequence step	*Desired condition for the signal lines*
1	Wafer probe test	Signal lines isolated from bulk
2	Anodic Bonding	Signal lines shorted to bulk
3	Final device	Signal lines isolated from bulk

Table 1: Various conditions for the signal lines during processing.

A metal-2 jumper deposited after wafer probe testing is used to connect the internal wafer probe pads to the poly-1 line, which forms the lead transfer. The signal comes out on poly-2 lines, which are shorted to the substrate to form the bonding tab. This satisfies the requirement during bonding. For normal operation of the final device, the signal lines are isolated when the lightly-doped silicon, where the bonding tabs have made contact, is dissolved during the EDP etch.

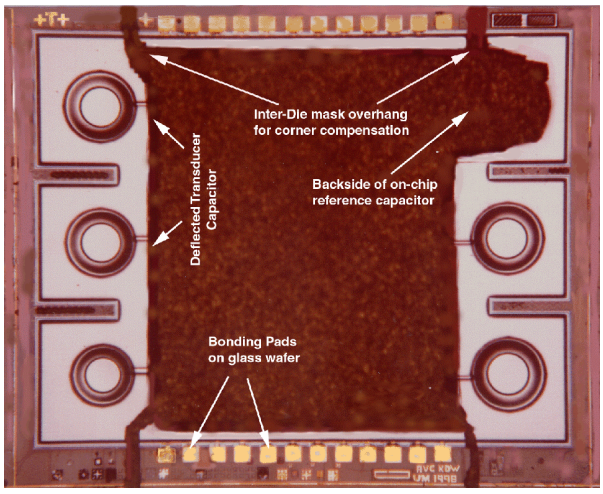

Fig. 8: A completed sensor, seen from the silicon side after release of the transducers in EDP.

FABRICATION AND TEST RESULTS

The final device as seen from the silicon side is shown in Fig. 8. It consists of five heavily-deflected diaphragms and one reference capacitor. Table 2 shows the effects of anodic bonding on various device parameters with the special metal shield used on the glass.

Device Name	*Size/Type*	*Effect of Anodic Bonding**
PMOS	W/L=3.3 Peri=120μm^2	ΔVt = ~-5mV
PMOS	W/L=1 Peri=1600μm^2	ΔVt = ~-50mV
NMOS	W/L=3.3 Peri=120μm^2	ΔVt = ~4mV
NMOS	W/L=1 Peri=1600μm^2	ΔVt = ~2mV
OTA	Folded Cascode	Δgain = ~-6dB Δoffset=-12mV

**370°C 10 minutes at 10-5mmHg; voltage stepped to 1000V*

Table 2: Effects of anodic bonding on device characteristics in a 2M/2P p-well CMOS process.

The devices which were directly fabricated in the lightly-doped bulk had the maximum shift in threshold voltages. The larger devices showed a greater amount of shift. The overall shift was still within tolerable limits for all analog circuits on the chip. The folded cascode OTAs have an open-loop gain of 50dB after bonding. The final DC output and the clock phases can be seen in Fig. 9a, while

(a)

(b)

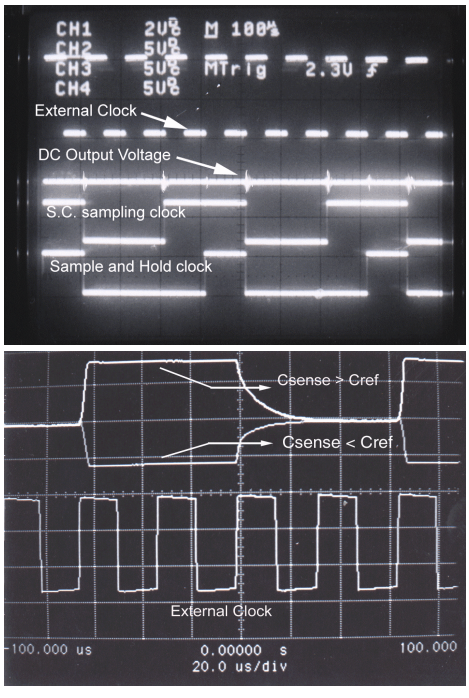

Fig. 9: a) Multi-phase readout clock generated on-chip; b) output of the gain stage for two different ratios of transducer to reference capacitance.

the output of the gain stage for two different pressure readings is shown in Fig. 9b. The maximum output sensitivity for a segment transducer is 48.8mV/Torr. Figure 10 shows the output voltage as a function of pressure for two segment transducers and a global transducer. The resolution is 25.6mTorr (15b) with a dynamic range from 500 to 800Torr. The NMOS devices, which were located within the more highly-doped p-well, had negligible threshold shift. The cavity

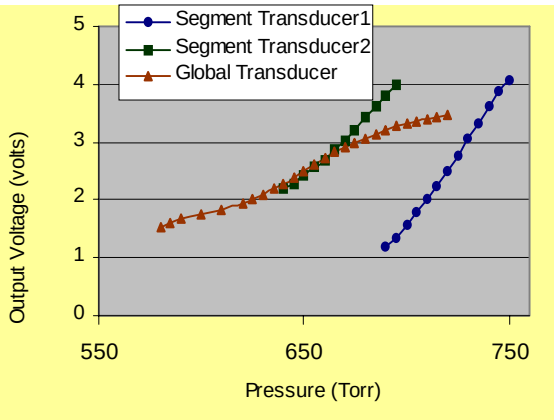

Fig. 10: Output voltage as a function of pressure for the global transducer and two segment transducers.

pressure after anodic bonding was in the range of 0.5-5Torr, resulting in an acceptable trapped gas TCO. In-cavity active getters and autocalibrating readout circuitry [5,9] is being developed to reduce and compensate for this residual gas. Use of DRIE instead of masked wet etching on the back-side can reduce the area of the device by up to 25%. Figure 11 shows a silicon-side view of a completed batch-processed monolithic pressure sensor wafer.

CONCLUSION

A monolithically integrated vacuum-sealed active pressure sensor was successfully fabricated using a monolithic CMOS micromachining process. The test results show that noise interference levels from external factors can be substantially reduced using this technique, giving a resolution of 25.6mTorr over a dynamic range of 500-800Torr. The device makes use of vacuum encapsulation at wafer level, thereby significantly reducing the packaging challenges. The process lends itself to batch fabrication with minimal modification to a simple 3µm CMOS process. Using the modular capability of the process, vacuum encapsulated surface-micromachined devices can also be fabricated in the same flow.

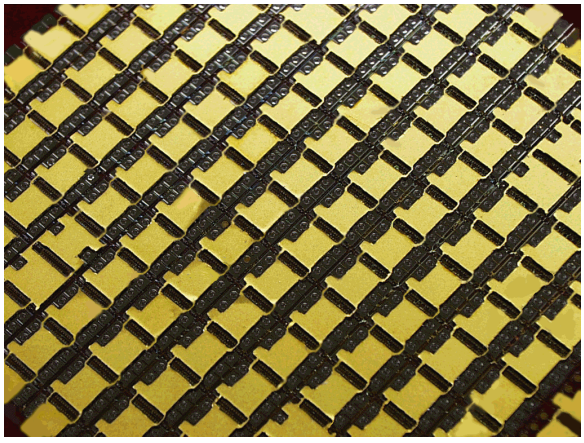

Fig. 11: View of a processed sensor wafer as seen from the silicon side.

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