Embedded-Mask-Methods for mm-scale multi-layer vertical/slanted Si structures

Yoshio MITA, Makoto MITA*, Agnès TIXIER, Jean-Philippe GOUY and Hiroyuki FUJITA*
All the authors are with LIMMS, CNRS-IIS, the University of TOKYO, JAPAN
*Also with CREST, JST

SUMMARY

Complicated deep-etched structures having multiple heights and vertical/slanted walls have realized by fully-silicon-based **batch** fabrication process, which only needs lithography on a flat surface. Arbitrary numbers of mask layers were laminated on the initial surface of a substrate and deep-RIE, LOCOS or anisotropic wet etching were performed to make microstructures using each mask layer subsequently.

I. INTRODUCTION

'2.7-D technologies' of Si deep-etching are proposed in this paper: Al-DMP and LOCOS-Al-DMP. As shown in fig.1, deep-etched multiple height structure, deep-etched structure with vertical and slanted wall, or multiple height structure with thin layer at the center are fabricated by these technologies. These technologies are quite compatible with CMOS-based surface micromachined structures.

Si micromachining technology began from surface (2-dimensional)[1] and it has been evolved toward 3-dimensional micromachining. At the early stage of micromachining, all the structures were fabricated on one plane: in the thickness less than 10 μ m. The 3D structure which can be obtained were anisotropically etched hole or mechanically drilled hole. In the end of 80s, two important technologies have arisen: LIGA and ICP-RIE anisotropic etching technology. Both two technologies were applied to obtain thicker structures (i.e. more than 10 μ m, up to mm-scale). These technologies sometimes are called 2.5-D technologies, since the shape of structure is the same from the top to the bottom.

The authors proposed a 'Delay - Masking - Process (DMP)[2]' to obtain multi-level structure of Si; by putting several different mask materials on a surface and perform deep-RIE by using the mask one after another. The pattern which was put on the surface can create multi-level Si structure. This method can be classified as '2.6-D technology', since multi-level structure can be obtained but the number of level is limited by the number of different kind of masking material, and the depth of each layer is decided by the etching selectivity of masking material to ICP-RIE.

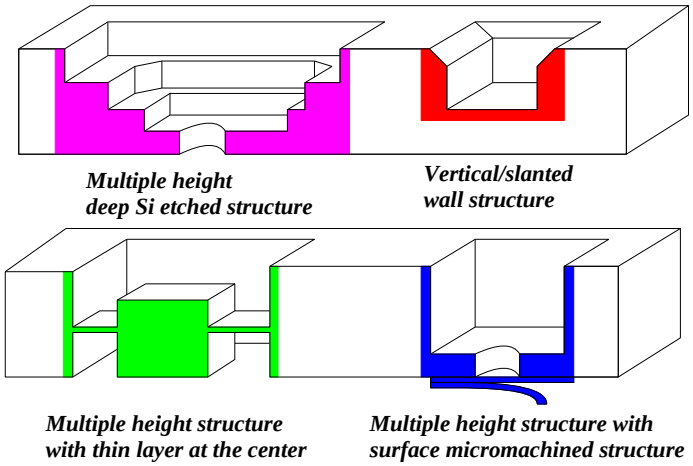


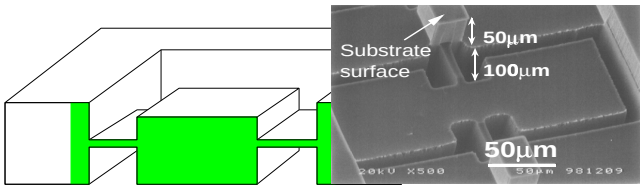
Figure 1: Obtainable 2.7-D structures by Al-DMP/LOCOS-Al-DMP.

The DMP tells us the fact; embedding the masking material and using them one after another make it possible to obtain the precise and multiple layer structure. Based on this principle, we propose '2.7-D technologies' of Si deep-etching: Al-DMP and LOCOS-Al-DMP. By Al-DMP, number of masking layers becomes unlimited, and the depth of each level is up to the limit of ICP-RIE apparatus. Moreover, by applying LOCOS-DMP, both dry deep-etching and wet anisotropic etching technologies can be combined.

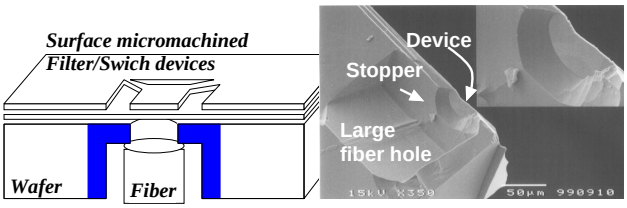
The "toward the 3D-micromachining technology" have been developed not only for cutting the edge of micromachining, but also for the specific applications. Obtainable structures and those applications are illustrated in fig.2: (a) Obtaining a thin layer in the middle of Si wafer as well as a thicker structure, (b) Making a through hole with 'stopper' structure for optical filter device, in having the active device on the other surface, (c) Micro Si mother board with well-aligned micro connector and micro socket, and (d) Making a shadow mask with suspended boss structure and mechanical alignment mark[3].

II. AL-DMP: ALMINUM BASED DELAY MASKING PROCESS

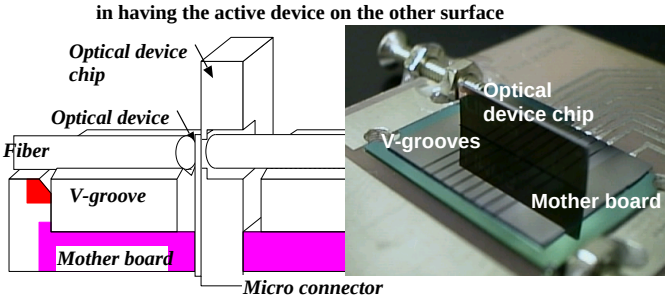
Many materials have been reported as a mask of ICP-RIE such as photoresist, SiO_2 and aluminum. Among these materials,



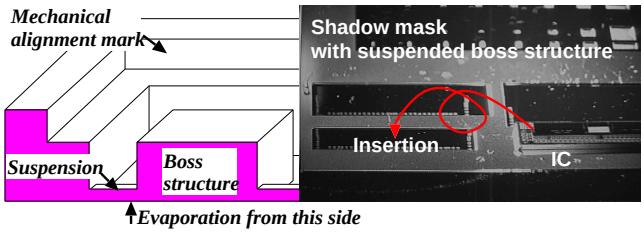
(a) Thin layer in the middle of structure (which works as spring), as well as thicker structure (which works as structure), for several optical scanner and resonator applications.



(b)Making a through hole with 'stopper' structure for optical filter, in having the active device on the other surface



(c) Micro Si mother board with well-aligned micro connector and micro socket



(d) Making a shadow mask with suspended boss structure and mechanical alignment mark

Figure 2: Applications of 2.7-D structures

aluminum has the best performance in terms of etching selectivity with Si. The nominal etching selectivity of these materials toward Si are, 1:100, 1:300, and 1:13000+, for photoresist, SiO_2, and Al, respectively. It shows that the thickness of each layer of DMP can effectively infinite when multi layer of Al can be obtained. We have succeeded to obtain the 3-layer Al mask by putting the exposed and hard-baked thin negative resist between each Al layers.

The process step is shown in fig.3. Process is composed of two phases: (I) Deposition and lithography of masking material and (II) Subsequent ICP-RIE and etching of each layer.

Phase-I: Deposition and lithography of masking material.

1. Evaporation of 0.2um aluminum.

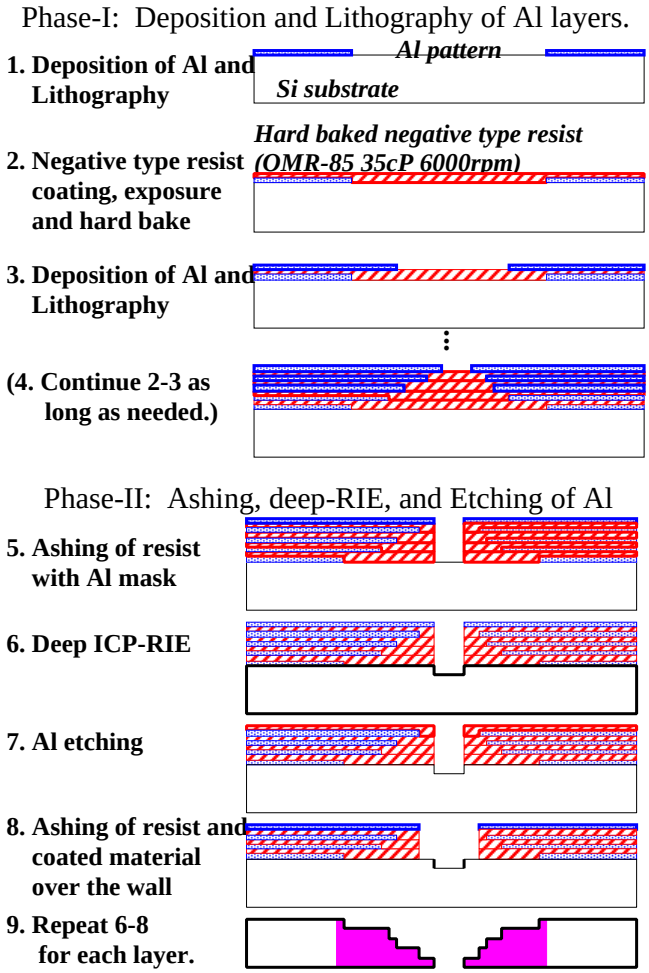


Figure 3: Al-DMP consists of two phase: deposition of Al layer phase and etching phase.

2. Photolithography of Al.
3. Prebake at 200℃, then deposition of negative type resist (OMR-85 35cP 4000rpm: 0.6um in this case).
4. Exposure and hard baking (200℃ 1hour).
5. Evaporation of 0.2um aluminum.
6. Photolithography of Al. (3-6 can be repeated when multi layer is needed.)

Phase-II: ICP and etching of each layer.

7. O2 ashing of negative photoresist by ICP-RIE.
8. ICP-RIE anisotropic Si etching (Bosch process for example.).
9. Al removal.
10. Repeat 7-9 for required multiple hights.

III. STRATEGY FOR MULTI-LAYER ETCHING DEPTH CONTROL

For multi-level depth structure, it is important to obtain precise etching depth of each layer as it is defined by specification. In this

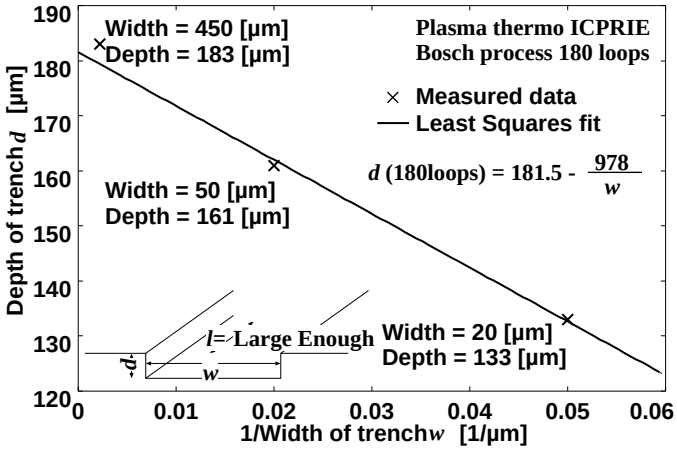


Figure 4: An example of etching depth dependency on pattern size. The narrower the width of trench is, the slower the trench is etched by ICP-RIE.

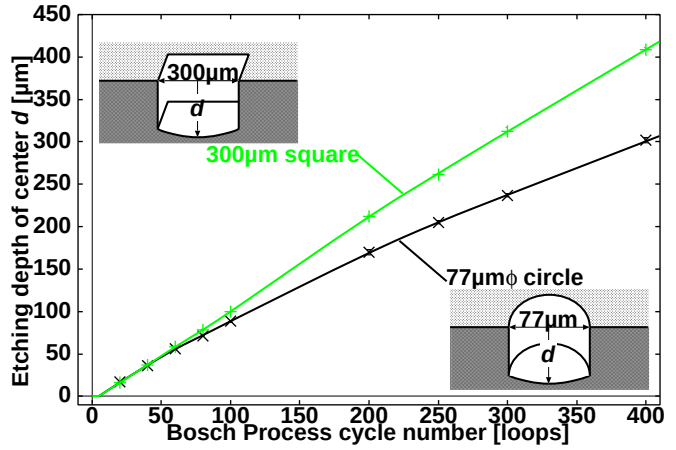


Figure 5: An example of the etching depth dependency on etching time for two different size of pattern. The deeper the trench is, the slower the etching speed becomes. Loop number in X axis stands for number of cycles of Bosch process.

section the strategy for controlling etching depth is described.

A. Key issues: etching speed and offset time.

In deep etching process using ICP-RIE, etching speed is dependent on the shape to be etched and total surface to be etched. The smaller the opening of mask is, the slower the etching speed becomes (fig.4); this phenomenon is known as a micro loading effect. Etching speed gets slower when the total etching surface in a wafer is larger. Etching speed is also dependent on the already etched depth: the deeper the trench is, the slower the trench is etched (fig.5). It is therefore necessary to measure the dependency of etching depth on the etching time and on the size of pattern, then calculate back the time for beginning of next layer etching.

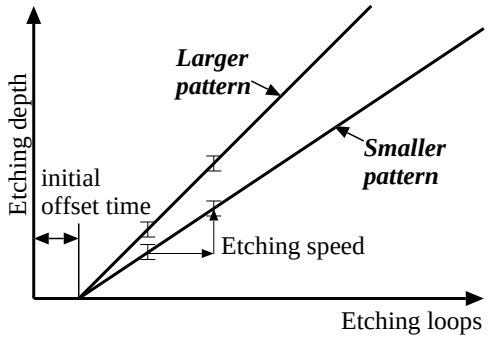


Figure 6: Deep etching begins with some offsets. Etching speed is faster when etching width is larger.

Another issue is the offset time of etching speed stabilization. The etching speed is slow at the beginning of deep-etching, typically several cycles of bosch process, then the etching speed is converged to a certain value as shown in fig.6. In authors' experiences, this offset time varies process by process. Hence, the etching depth must be measured some time after beginning of etching to measure offset time.

B. Estimation of n^{th} layer etching beginning time.

Once etching depth dependency on etching time is measured by simple structure, etching depth estimation curve for multi-level Si structure can be composed. The important thing is that etching speed is dependent mainly on the local size of etched pattern, even for multi-level structures.

Suppose an example in which two-layer of small (77 μ m circle) and large(300 μ m square) holes are being etched. Thickness of the wafer is 300 μ m. Etching time – etching depth curves for each shape are measured as shown in fig.5. As for a specification, small hole must be etched through the wafer (= 300 μ m) and stop by SiO_2 layer covered with Si on the other surface of wafer. Large hole must be etched down to 280 μ m (=20 μ m less than the thickness of the wafer). The procedure is as follows:

1. Perform 20 loop of bosch process with a mask for small hole.
2. Measure the etching depth of the small hole.
3. Perform another 20 loop etching and measure the etching depth.
4. Superpose the etching curve for small hole over the measured points.
5. Necessary loop count for first layer to reach to another end of wafer is calculated by the curve.
6. Plot final etching depth for the large square at the calculated etching-end time in step 5.
7. By superposing etching curve for the large square, calculate back the etching beginning time for next layer.

8. Perform etching until the back calculated time, then proceed the second layer with mask for large square.

Figure 7 shows a real procedure of etching time back-calculation with real data. The experiment was performed with ICP-RIE apparatus SLR-720ICP from Plasma-Therm co. The precision of depth using this back-calculation method is roughly $\pm$ 15 μ m. This error can be attributed first to depth measuring error with optical microscope (the last digit of micrometer is 1 μ m.), then to the other factors such as total etching surface.

IV. LOCOS-AL-DMP: OBTAINING DIAGONAL CUT OVER DEEP RIE STRUCTURE.

LOCOS-Al-DMP is also based on the same principle as Al-DMP: 'Embedding masks before deep-etching'. In this case, silicon nitride layer is deposited beneath the Al multi layers. As shown in fig.8, Si_3N_4 remains after DMP. The wafer is then oxidized. Oxidation with silicon nitride layer is well known as LOCOS; all the surface of the wafer except the area covered with Si_3N_4 is oxidized. After removing Si_3N_4 selectively, the wafer is immersed into TMAH. The wafer is anisotropically etched; the vertical wall in the wafer remains protected by SiO_2, hence both vertical and slanted etched structure can be obtained. The idea of combining wet/dry anistropic technology and LOCOS has also been proposed by many other institutes[4], [5].

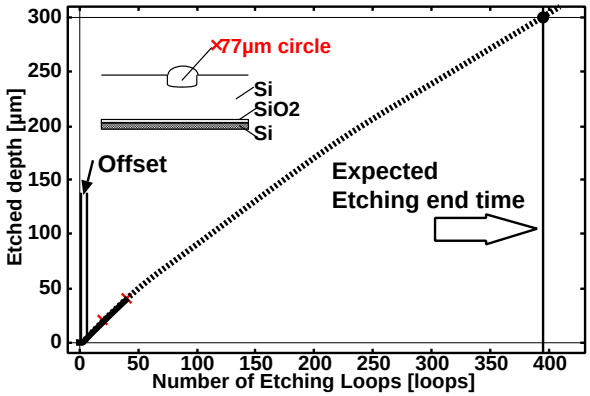
V. FABRICATION EXAMPLES

A. Al-DMP result

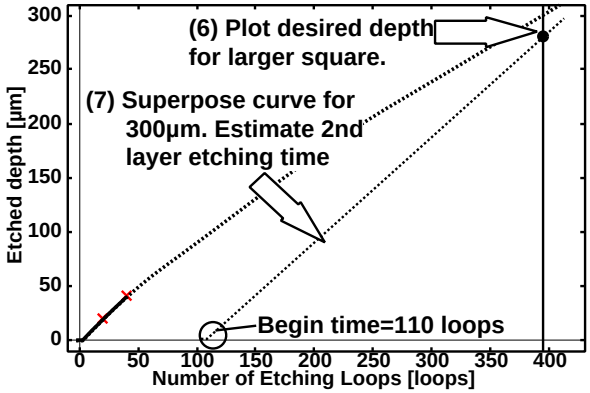
The photograph of a Si piece processed by 3-layers Al-DMP is shown in fig. 9. The surface remains smooth at all the process step. The important thing to obtain this smooth surface of Al mask is baking temperature of photoresist for intermediate layer. When using positive type resist and with post-baking of 130℃ 1hour, many ripples found on the resist after ICP-RIE. Therefore the photoresist as intermediate layer must be baked in high temperature (200℃). Negative type photoresist is chosen for this purpose because negative type photoresist can generally be baked at higher temperature then positive type and is not damaged by acetone in cleaning. The fabricated Si piece is used as a micro mother board on which the two pieces of optical filter chip are put on as shown in fig.2(c)[6]. Depth of each layer were 170 μ m, 230 μ m, and 400 μ m.

B. LOCOS-Al-DMP result

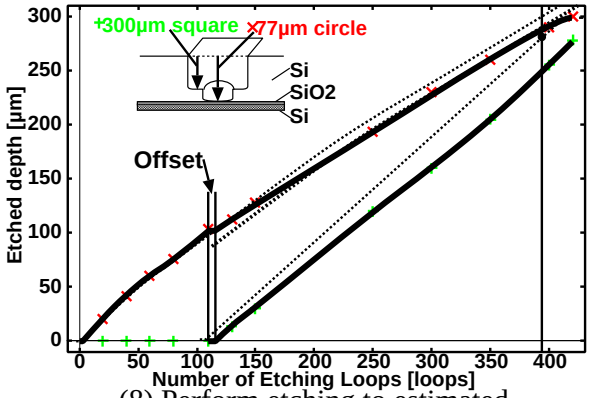
Figure 10 shows a silicon micro socket with a guide slope at the mouth of it. Wet anistropic etching was performed with TMAH solution at 80℃. The etching started from V-shape crosssection. However, after 2 hours of TMAH etching, the $<111>$ plane on the side of vertical wall was etched faster



(1-5) Etching of first 40 loops, superpose etching curve for 77μm



(6,7) Pointing out the desired etching depth, back calculation



(8) Perform etching to estimated loops, begin second layer etching

Figure 7: Procedure of DMP with precise control of etching depth of layers.

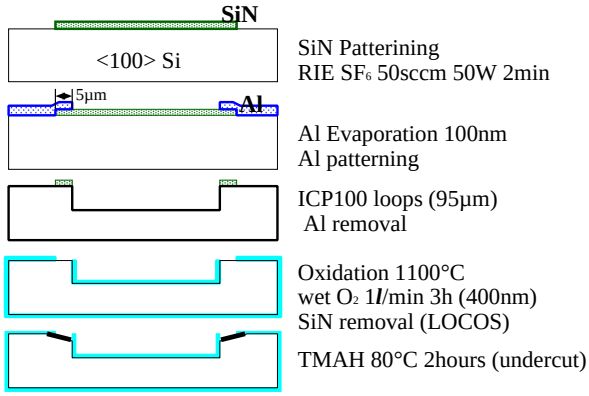
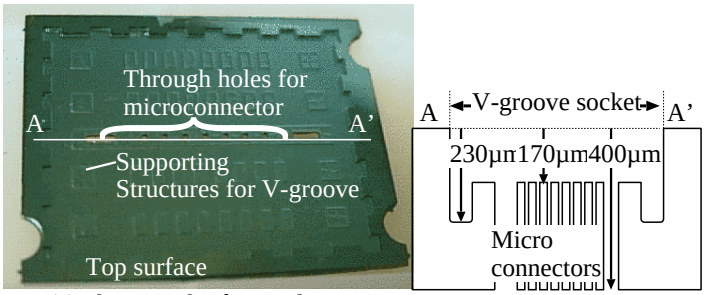


Figure 8: LOCOS-Al-DMP process chart.



(a) Photograph of optical system mother board by Al-DMP.

(b) Crossectional view

Figure 9: An example of 3-layers Si bulk micromachined structure.

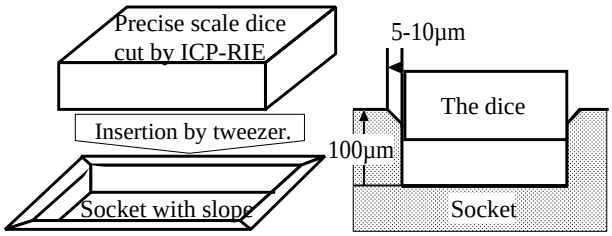
and disappeared, thus forming the slanted wall at the mouth of vertical wall. Thanks to this slanted wall, the tweezer-insertion of Si piece whose size is 5 μ m smaller than the socket was performed with no difficulty.

VI. REMARKS FOR A STABLER PROCESS WITH AL AND ICP

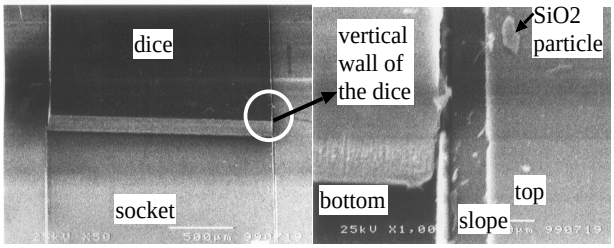
In this section some remarks for a stabler single/multi Al mask ICP-RIE process are discussed: (1) Aluminum mask contains submicron pin holes in many cases so that supplemental SiO_2 layer helps protecting the structure from damage through pin holes. (2) Prebake and postbake must be well performed before/after deposition of negative resist for Al-DMP.

A. Avoiding Surface damage by Al pin holes

Despite its superior selectivity of aluminum to ICP, Al mask in many cases contains pin holes randomly. The size of pinhole is sub-micron level so that it is hardly observed. The etching plasma, however, does pass through the pinhole so that the structure underneath can be damaged. This damage can simply be avoided by putting some passivation layer such as SiO_2 underneath Al. As shown in fig.11 (a), the 2-layer poly-



(a) Principal of microsocket with guide slope.



(b) Successful insertion of 1.9mm-wide Si piece

(c) Guide slope magnification.

Figure 10: Example of Al-LOCOS-DMP as a guide slope of silicon micro socket.

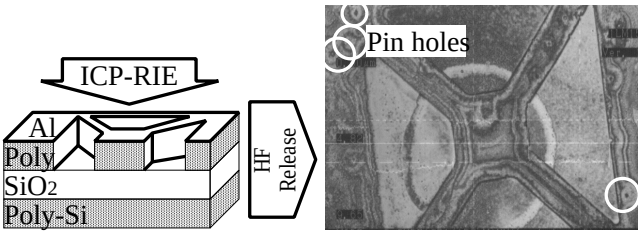
Si structure was damaged everywhere because of pin holes. Sacrificial layer etching is not successful since undercut is performed also from pin holes of Si invoked by Al pin holes. By putting an 1.2 μ m of SiO_2 passivation layer by LPCVD as shown in fig.11 (b), the surface micromachined structure is not at all damaged after ICP-RIE. This emphasizes the importance of passivation of surface micromachined devices to ICP-RIE with Al mask.

B. Prebake/Postbake of intermediate negative resist

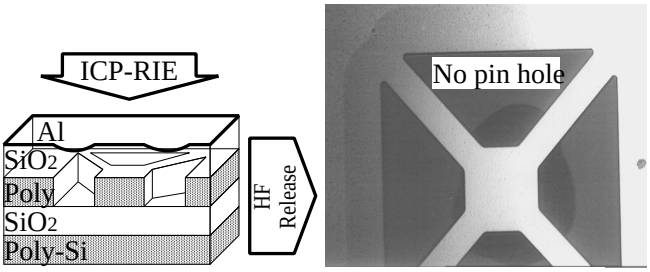
Baking is one of the key issues of Al-DMP. There are two typical pitfaults concerning baking: (1) Not sufficient post-baking causes rippled surface of resist, and (2) Not sufficient pre-baking causes bubbles of gas from residuals. Pre- and Post-baking are therefore very important and the authors perform baking for a long time at 200℃.

B.1 Rippled surface

While ICP-RIE or evaporation of Al, the surface temperature of wafer can rise up to 140℃ –150℃. The photoresists which are baked less than 130℃ can be well affected by the temperature and cause the ripple. Once ripple occurs on the surface it causes many severe cracks over photoresist, resulting damages over underlaying Al layer while Al etching (see fig.12). To avoid this problem, the authors perform 1 hour of baking at 200℃ after deposition of each intermediate layer.

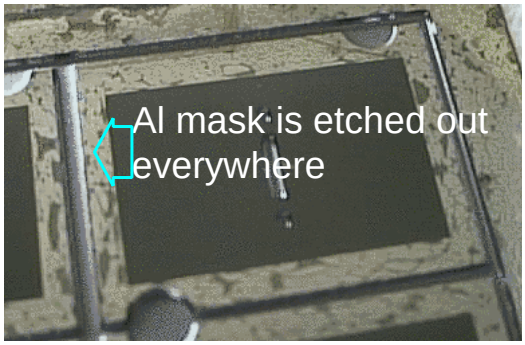


(a) ICP-RIE without passivation of surface structure.

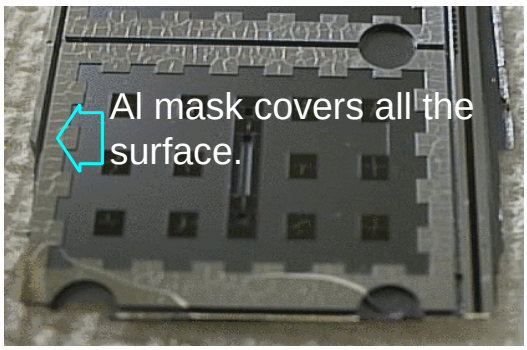


(b) ICP-RIE WITH passivation of surface structure.

Figure 11: Pinholes in aluminum can be the cause of surface damage (a). 1.3 μ m of SiO_2 well protected the surface(b).



(a) 130°C baked negative resist created many cracks after ICP-RIE then Al mask beneath have been etched.



(b) 200°C baked negative resist did not have severe cracks.

Figure 12: Insufficient baking can create rough surface of resist, then cracking everywhere for Al enchant to pass through.

B.2 Vapors from residuals

Before coating the surface with photoresist, it is extremely important to bake well the substrate. The authors performs pre-baking before resist coating at the temperature of post-baking (200℃). By this pre-baking, majority of the molecule on the the surface which might be able to evaporate while post-baking can be evaporated in advance.

VII. CONCLUSION

In this paper we have presented a 2.7-dimensional Si micromachining methods; Al-DMP and LOCOS-Al-DMP. Silicon structures having arbitrary numbers of thicknesses can be obtained. Wet anisotropic etching technology and dry high-aspect-ratio-technology are combined by means of LOCOS. The generic idea is to embed masking layers on one plane and use them one after another. Surface micromachined structures can also be embedded, thus providing 2+2.7-dimensional structures.

ACKNOWLEDGEMENTS

The authors would like to thank the Members of Fujita Laboratory for discussion and support. The authors also thank VLSI Design and Education Center (VDEC) to allow them to use electron beam chromium mask fabrication facility.

References

[1] for example: M.Madou, “Fundamentals of MICROFABRICATION”, *CPC Press* NY, ISBN0-8493-9451-1

[2] M. Mita, H. Toshiyoshi, T. Oba, Y. Mita and H. Fujita, “Multi-height HARMS by Planar Photolithography of Initial Surface”, *In Proceedings of High Aspect Ratio MicroStructure Technology (HARMST ’99)*, pp. 28–29, June 13–15, Chiba Japan.

[3] A.Tixier, Y. Mita, J.-P. Gouy and H.Fujita, “A silicon shadow mask for deposition of isolated areas”, *In Proceedings of Micromechanics Europe (MME ’99)*, pp. 195–198, Sep. 27–28, Orsay, France.

[4] V.Ianev and N. Schwesinger, “Multistep Deep Structuring of Silicon Using Wet Anisotropic Etching and Dry Etching Processes for MicroMechanical Purposes (part 2)”, *In Proceedings of Micromechanics Europe (MME ’99)*, pp. 160–163, Sep. 27–28, Orsay Orsay, France.

[5] J.-J Choi, R. Toda, K. Minami and M. Esashi, “Silicon Angular Resonance Gyroscope by Deep ICPRIE and XeF_2 Gas Etching”, *In Technical Digest of 11th IEEE International Workshop on Micro Electro Mechanical Systems (MEMS ’98)*, pp. 322–327, Jan. 25–29, Heiderberg, Germany.

[6] A. Tixier, Y. Mita, S. Oshima, J.-P. Gouy and H. Fujita, “3-D Microsystem Packaging for Interconnecting Electrical, Optical and Mechanical Microdevices to the External World”, *In Technical Digest of 13th IEEE International Conference on Micro Electro Mechanical Systems (MEMS 2000)*, Miyazaki, Japan.