A METHOD TO EVADE MICROLOADING EFFECT IN DEEP REACTIVE ION ETCHING FOR ANODICALLY BONDED GLASS-SILICON STRUCTURES

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ABSTRACT

Due to the microloading effect, an overetch in through-wafer etchings by DRIE has to be taken into account in the fabrication of glass-silicon structures, which results in damages of the silicon surfaces exposed to an ion bombardment. This paper reports on a method, in which a metal layer located on the glass surface and electrically connected with the silicon substrate is used. Even though structures are overetched for a long time, the silicon surfaces remain intact. The results show interdependency between the position of the metal layer on the glass surface and the gap separating the silicon and glass surfaces.

INTRODUCTION

The fabrication of Micro Electro Mechanical Systems (MEMS) usually requires at least one silicon etching step in the entire process. Especially for bulk micromachined devices, silicon etchings with high etch rates, high aspect ratios and high selectivities to mask materials are required for a through-wafer etching. Nowadays, etchings with such specifications are mainly achieved by Deep Reactive Ion Etching (DRIE) using high density plasma sources.

In plasma etching, the well-known microloading effect [1] is an important phenomenon to be considered for the design of the devices. This effect can be described as the interdependency between the etch rate and the aspect ratio, in other words wide trenches etch more fastly than narrow trenches. In the case of through-wafer etchings, it is necessary to take into account an overetch time in order to compensate this difference of etch rate. Therefore, undesirable effects occur in the wide trenches overetched for a long time. For example, a notching effect defined as a lateral etching at the silicon/oxide interface has been observed. This effect is quite important in DRIE systems in reason of their high density plasmas [2-3].

In this paper, we reports on a new method which enables the achievement of DRIE etchings for anodically bonded glass-silicon structures without taking into account the microloading effect. The solution proposed here, is to use a metal layer deposited on the glass surface and electrically connected with the silicon substrate, which enables a long overetching without significant damages on the silicon surface located above the glass surface. We also describe the effects for the following parameters: the position of this metal film on the glass surface and the gap between the silicon and glass surfaces.

EXPERIMENTAL

The DRIE behaviour for glass-silicon structures and the consequences of a metal layer on the glass surface have been studied through a test structure. The schematic process flow for the fabrication of this structure is shown in Figure 1. Two 3 inch wafers, one 380 μm thick p-type silicon wafer (resistivity: 1-10 Ωcm) and the other one a 600 μm thick Pyrex #7740 glass wafer have been used in the experiment. The silicon wafer is etched to a depth of 230 μm using DRIE technology and standard photoresist as a masking layer, resulting in a 150 μm thick silicon diaphragm. The preparation of the glass wafer consists of patterning first and then etching with HF a 20μm deep cavity. Then, a 2000Å thick Chromium (Cr) layer is deposited on this glass surface by sputtering, patterned and etched with a Cr etchant. Next, the glass wafer is anodically bonded with the processed silicon wafer. Finally, the front side of the silicon wafer is patterned and etched through the 150 μm thick diaphragm by DRIE. In order to compensate the microloading effect, an overetch time has been taken into account during this final DRIE step.

The DRIE steps have been carried out in a Plasma-Therm Shuttle Lock etch tool equipped with an Inductively Coupled Plasma (ICP) source operating at 2 MHz. This etch system is also equipped with a mechanical wafer clamp and helium backside cooling to improve the evacuation of heat from the wafer and thus providing an accurate temperature control. This etcher uses the recently developed High Aspect Ratio Si Etch (HARSE) process [4] ensuring the achievement of features with high depth-to-width aspect ratios,

anisotropic profiles, high Si etch rates and good dimensional control at room temperature. The HARSE process relies on the sidewall passivation technique. This technique is achieved with a cyclic method consisting of deposition and etch phases for each cycle, which requires the use of a high density plasma source such as ICP. Fluorine-based chemistry is used to etch silicon by producing volatile etch products. Since this etching actually has an intrinsically isotropic behaviour, the deposition step enables a maximum reduction of the lateral silicon etching. Thus, the desired silicon etching anisotropy is obtained.

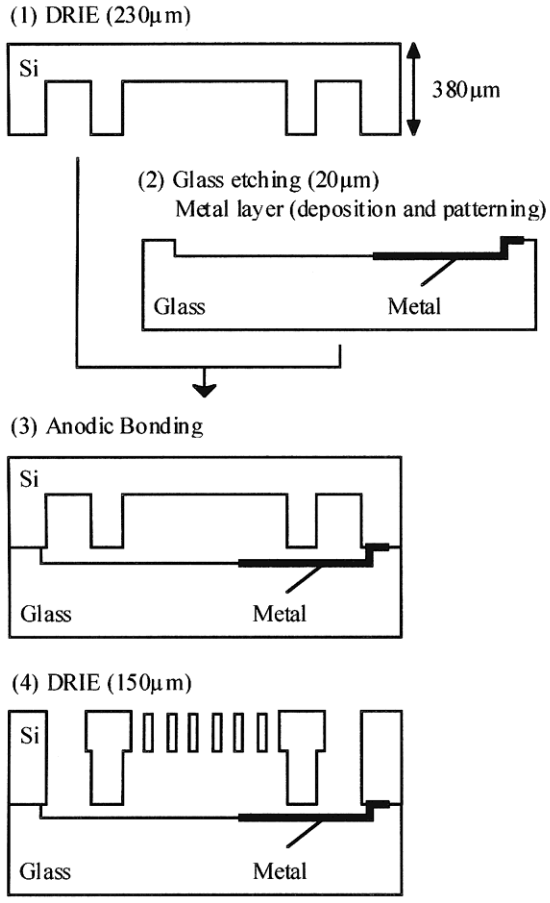

Figure 1: Process flow of the test structure

RESULTS AND DISCUSSION

Using the process described in the previous section, different test structures have been fabricated changing the position of the metal layer on the glass surface. The effects of this metal layer have been observed after the through-wafer etching by DRIE. The results below describe, firstly the importance of an electric connection between the metal layer and the silicon substrate and secondly the interdependency between the position of the metal film under the silicon surfaces and the gap between the silicon and glass surfaces.

Metal layer and electric connection

This section describes the advantages of using a metal layer deposited on the glass surface to avoid some undesirable effects occuring for standard glass-silicon structures during through-wafer etchings by DRIE. These results highlight the necessity of electrically connecting this metal layer with the silicon substrate.

Figure 2 shows the results after the final DRIE etching for a structure with a metal layer deposited on the 20 μm deep cavity etched in the glass wafer. This layer is at a floating potential compared to the silicon substrate. The silicon surfaces located 20 μm above this Cr layer are seriously damaged as shown in Figure 2. Similar damages have also been observed for a structure without metal film on the glass surface.

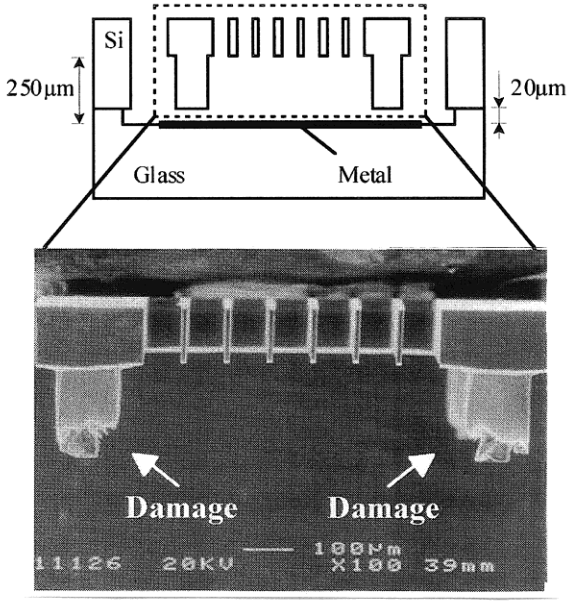

Figure 2: SEM micrograph showing the damages of the silicon surfaces after the through-wafer etching for a structure with a floating metal layer on the glass surface

In other experiment, the patterning of the metal layer has been carried out in order to obtain an electric connection between the Cr film and the silicon substrate after the anodic bonding. The etching results are shown in Figure 3. Though significant damages occur in the silicon area located above the glass surface, the silicon surface located above the Cr film remains perfectly intact after the final DRIE step.

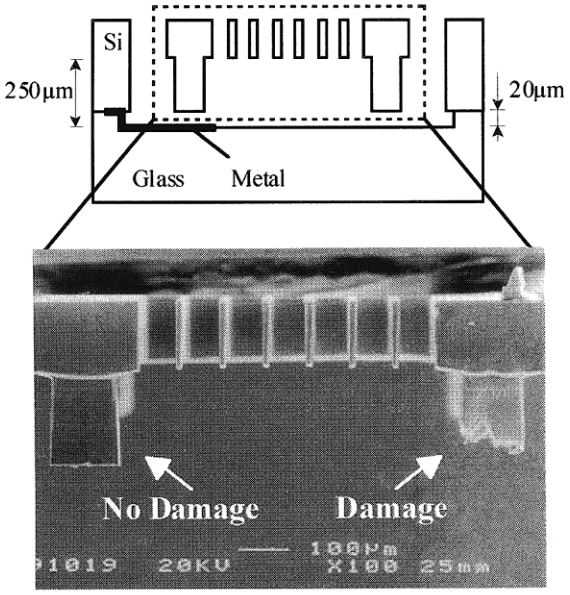

Figure 3: SEM micrograph showing an intact silicon surface above the Cr film after the through-wafer etching by DRIE for a structure with a metal layer electrically connected with the silicon substrate

Silicon surfaces, located above a glass surface or a floating metal layer deposited on the glass surface, are damaged during the overetch of the final DRIE. Once the etching is done through the 150 μm thick silicon diaphragm, the glass surface is exposed to an ion bombardment resulting in an accumulation of charges. Since the ions are strongly peaked about normal (highly anisotropic), the initially bombarded glass surfaces are the ones located underneath the trenches etched through the diaphragm. Once the potential is built up, these incident ions undergo an electrostatic deflection. Because of this charge-induced trajectory bending of ions, the initially unaffected glass surfaces located 20 μm under the silicon surfaces are exposed to an ion bombardment. The probable mechanism occuring in this region is schematically illustrated in Figure 4(a). The incident deflected-ions colliding with the glass surface are reflected in direction of the silicon surface. This glass area underneath the silicon surface also undergoes charging due to the bombardment of the forward deflected-ions. This charging effect can sufficiently deflect the ion trajectory in direction of the silicon surface. Both phenomena induce the damages of the silicon surface shown in Figure 2 and in the right part of Figure 3. However, with a metal layer electrically connected with the silicon substrate, the silicon surfaces located above this metal layer remain intact after DRIE, irrespective of the overetching time. Figure 4(b) shows the mechanism that takes place in the region of a glass surface located 20 μm under a silicon surface and covered by a metal layer electrically connected with the silicon substrate. The incident deflected-ions bombard the Cr film resulting in a charge accumulation. However, these charges can be evacuated from this area to the silicon substrate due to the electric connection. Therefore, the potential distribution in this region is not modified and no ion trajectory bending can occur in direction of the silicon surface.

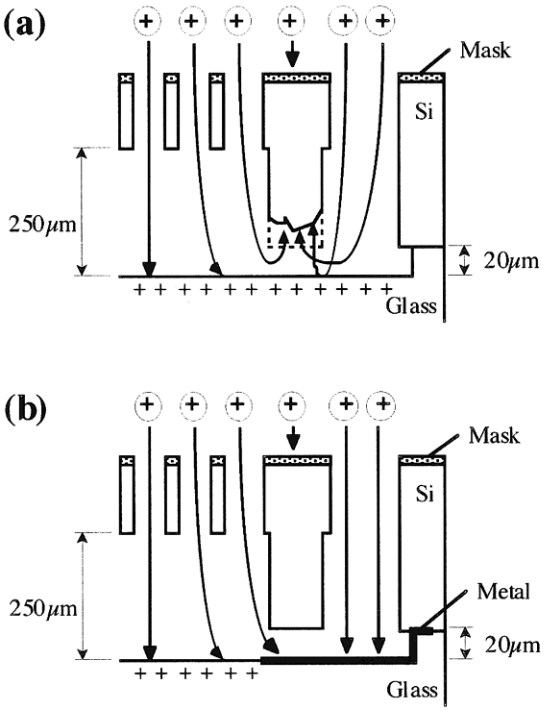

Figure 4: Schemes illustrating the mechanism of through-wafer etchings by DRIE (a) without metal layer and (b) with electrically connected metal layer

Interdependency: position of metal layer on glass - gap between glass and silicon surfaces

The following experiments have been carried out to investigate the importance of the position of the metal layer on the glass surface as a function of the gap separating the silicon surface from the cavity etched in the glass wafer. In these experiments, the metal layer has always been electrically connected with the silicon substrate.

Figure 5 shows the etching results for a structure in which there is no metal layer on the glass surface located under the silicon diaphragm. The silicon surface of the lower part of this silicon diaphragm is damaged during the final DRIE step along its entire surface as shown in Figure 5(a).

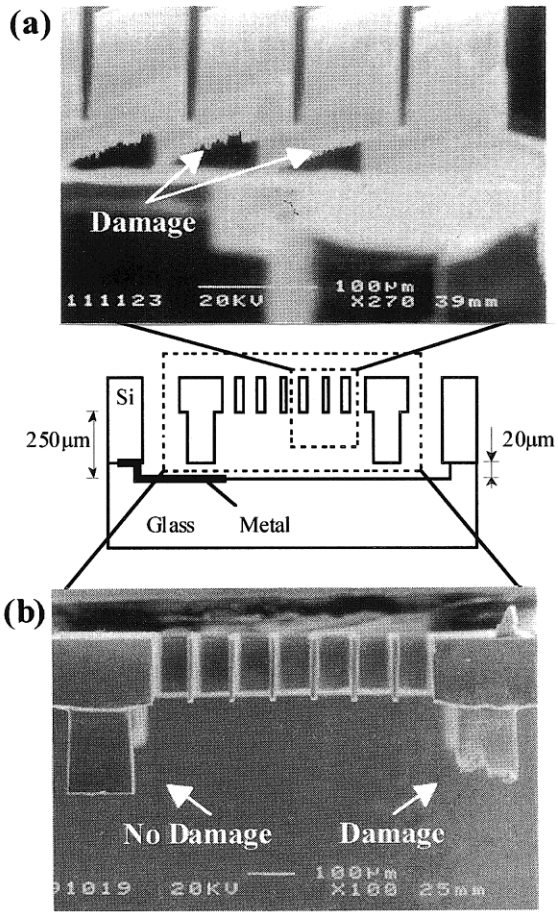

Figure 5: SEM micrographs showing the etching results for a structure without metal layer under the diaphragm region (a) Damage in the lower part of the diaphragm (b) Cross-sectional view

Figure 6 shows the etching results for a structure in which a metal layer has been patterned to cover only the half part of the cavity etched in the glass wafer. The silicon part located 250 μm above the glass surface (lower part of the silicon diaphragm) shows no apparent damages along its entire surface, even though half of the corresponding glass surface is not covered by the Cr film.

The mechanism taking place in the region under the silicon diaphragm seems to be governed by the potential variation of the microstructure. Once the etching is performed through the diaphragm, the glass surface is exposed to an ion bombardment, which gradually modifies the potential distribution of the microstructure. For a glass surface under the diaphragm without any metal layer, the variation of the potential distribution is sufficient enough to alter the ion dynamics as soon as they enter in the windows etched through the diaphragm. This ion trajectory bending leads to the damages in the lower part of the silicon diaphragm as shown in Figure 5(a). When only half of the glass surface is exposed to an ion bombardment, less charge accumulation occurs on this glass surface, which results in a smaller variation of the potential distribution of the microstructure. This smaller variation alters the bending of the ion trajectory in a region closer to the glass surface. Therefore, the lower part of the silicon diaphragm remains intact as shown in Figure 6(a).

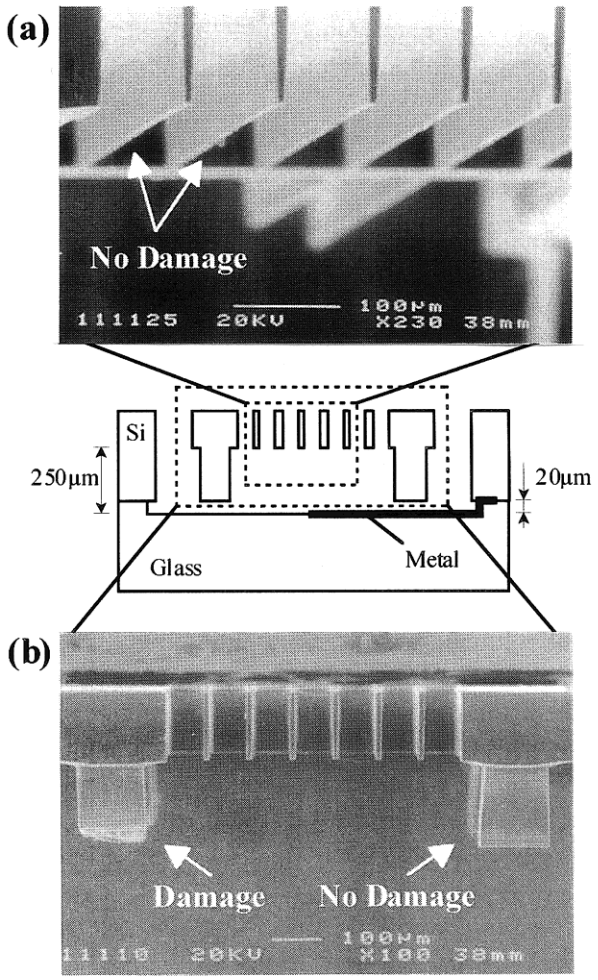

Figure 6: SEM micrographs showing the etching results for a structure with a metal layer covering half of the cavity etched in the glass wafer (a) Intact surface in the lower part of the diaphragm (b) Cross-sectional view

As shown in Figures 5(b) and 6(b), the silicon surface located 20 μm above the glass surface is more significantly damaged in the case of a structure without metal layer on the glass surface located under the silicon diaphragm. The variation of potential distribution, which depends on the size of the glass area exposed to the ion bombardment, is probably at the origin of this difference of damages. This observation can be taken as an additional evidence to support the above proposed mechanism.

CONCLUSION

A method has been presented to evade the damages due to the microloading effect as a result of overetching time in DRIE for anodically bonded glass-silicon structures. This method requires a metal layer on the glass surface electrically connected with the silicon substrate. Due to this electric connection which avoids a charge accumulation by the evacuation of these charges to the silicon substrate, the silicon surfaces remain intact irrespective of the overetching time in DRIE. The results show interdependency between the position of the metal layer on the glass surface and the gap separating the silicon and glass surfaces. Unlike small gaps (20 μm) for which the metal layer has to be located under the silicon surface, the position of the metal layer is not so critical for big gaps (250 μm). Further experiments are required to investigate this interdependency. Because no damage of the silicon surfaces occurs during the through-wafer etching by DRIE, the performance of glass-silicon devices can be significantly improved using this method.

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